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Measurement of Integrated PA-to-LNA Isolation on Si CMOS Chip

Ryo Minami[#1], JeeYoung Hong[*2], Daisuke Imanishi[*3], Kenichi Okada[*4], and Akira Matsuzawa[*5]

[#*]*Department of Electrical and Electronic Engineering, Tokyo Institute of Technology*
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552 Japan
[1]minami@ssc.pe.titech.ac.jp
[*]*Department of Physical Electronics, Tokyo Institute of Technology*
[2]hong@ssc.pe.titech.ac.jp
[3]imanishi@ssc.pe.titech.ac.jp
[4]okada@ssc.pe.titech.ac.jp
[5]matsu@ssc.pe.titech.ac.jp

***Abstract* — This paper shows measurement results of on-chip coupling between PA and LNA integrated on Si CMOS substrate, which is caused by substrate coupling, magnetic coupling, wire coupling, *etc.* These components are decomposed by measurements using diced chips. The result reveals that the substrate coupling is most dominant in CMOS chips and the total isolation becomes less than -50 dB with more than 0.4 mm PA-to-LNA distance.**

***Index Terms* — CMOS amplifiers, Duplexers, electromagnetic coupling, Mutual coupling, substrate coupling, Tx leakage**

I. Introduction

A low noise amplifier (LNA) is one of the key building blocks in RF transceivers. The LNA is used at receiver to amplify a weak signal from an antenna. There are many metrics to evaluate the LNA such as PG (Power Gain), NF (Noise Figure), IIP3 (3rd order Input Intercept Point), power consumption. Above all, the LNA is required to amplify the weak signal even if strong interferes exist.

A power amplifier (PA) is also the key building block in RF transceivers. It amplifies a signal in a transmitter so that the signal can be transmitted to a receiver far from the transmitter. To transmit the signal far away, the conventional power amplifier has been implemented by compound semiconductors such as GaAs, which has a superb high-frequency characteristic and high supply voltage. However, it causes the increase of die area and cost, because the power amplifier has to be designed as an external block. The PA is desired to be integrated in a single-chip transceiver which integrates all functional blocks for wireless communications in the view of cost, die occupancy, and so on. Therefore, the PA is preferable to be implemented by CMOS process. The miniaturization of the recent CMOS transistors can provide a sufficient ability for power amplifier and realize high frequency operation for RF circuits [1].

As compared with TDD systems, FDD systems have several design issues. One of the most critical issues for one-chip transceivers is Tx leakage. In the FDD systems, a transmitter and a receiver simultaneously work, and a duplexer is utilized to share a single antenna. However, duplexers have leakage between every ports, which is referred as isolation. Tx output power is very large as compared with received signal, so it

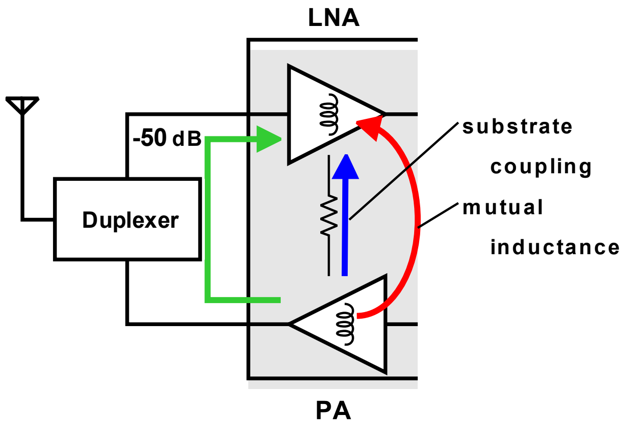

Fig. 1. Tx leakage path.

becomes considerably large interferer at Rx input even if the leakage is very small. This is called as Tx leakage. Tx leakage causes intermodulation and degrades demodulation quality.

Moreover, the integration of the PA with other blocks increases many coupling paths such as substrate coupling, magnetic coupling of inductors, and wire coupling (V_{DD}, GND, *etc*). As the result, the level of Tx leakage also increases [3].

To investigate the increased Tx leakage, a PA and some LNAs are placed on the same chip. Moreover, the chip is diced between PA and LNA for measuring an influence of each coupling, especially substrate coupling and magnetic coupling. The isolations of each PA-LNA is measured and compared to the simulated results.

Section II describes the coupling mechanisms. Section III discusses the simulation and measurement results. Section IV reveals the conclusion about the dominant coupling mechanisms based on measurements.

II. Evaluation of Tx-Leakage

Integration of PA with other blocks on the same chip causes various coupling paths like Fig. 1. There are a substrate coupling, magnetic coupling of inductors, and wire couplings (V_{DD}, GND). Thus, a PA and multiple LNAs are implemented on the same chip to investigate an influence of the couplings.

The wire couplings through V_{DD} and GND lines are considered as a negligible quantity. In the case of V_{DD} wire coupling, the each supply voltage is different. Moreover, GND wire is connected with a substrate, so that it is very difficult to distinguish the GND wire coupling from the substrate coupling. Thus, the GND wire coupling is included into the substrate coupling in this paper.

Consequently, the substrate coupling and magnetic coupling by inductors are considered an impact factor to Tx leak age. Thus, a PA and multiple LNAs are placed on the same chip and measured and simulated.

A. Measurement method.

Fig. 2 shows the measurement setup. To measure the influence of substrate couplings and magnetic coupling of inductors individually, the chip is diced [4]. Fig. 3 shows the chip which is diced. On this chip, there is a PA and several LNAs. After dicing, the distance between the PA and each LNA is 0.74 mm, 1.55 mm, 2.37 mm and 3.20 mm. As a result, the substrate couplings are blocked by physically separating the PA and LNA. Thus only magnetic coupling of inductors can be measured by using a Network Analyzer. Concretely, the input is configured as the PA and the output as the LNA. The isolation is calculated by subtracting the sum of power gain (PA and LNA) from S_{21} as the following equation.

$$isolation\ [\mathrm{dB}] = S_{21} - (G_{PA} + G_{LNA}) \qquad (1)$$

To separate the substrate coupling from the total coupling, the following equation is used with the measured isolations before and after dicing.

$$coupling_{substrate} = dicing_{before} - dicing_{after} \qquad (2)$$

Furthermore, thermal noise which is generated by resistance of LNA's input side is calculated by Eq. (3) and compared with S_{21}. In Eq. (3), the bandwidth (B), temperature (T), and cable loss (LOSS) are assumed 10 Hz, 300 K, and 2 dB, relatively. Measured NF_{LNA} and G_{LNA} are used.

$$Noise_{thermal}[\mathrm{dBm}] = 10\log(\mathrm{k}TB) + NF_{LNA} + G_{LNA} - Loss_{cable} \quad (3)$$

$$Noise_{thermal}[\mathrm{dB}] = Noise_{thermal}[\mathrm{dBm}] - (NA_{out})[\mathrm{dBm}] \qquad (4)$$

In addition, the noise floor of network analyzer and probe coupling should be considered, which influence on the coupling measurement. The probe coupling is assumed to be caused by the electromagnetic radiation between probes. These effects are evaluated by the open measurement without chips. The open measurement is done with 0.3mm distance between probes and stage of probe station, and distance between probes is varied from 0.74 mm to 3.2 cm. The noise floor is measured as S_{21} with 3 cm probe distance and 2 cm distance between probe and stage of probe station. Moreover the probe coupling is measured depending on the probe distance. In this case, the measured probe coupling is considered as the worst case one, because probes behave as monopole antennas and have larger coupling. In case of actual measurement, the probe tip is terminated by DUT, so the coupling will become smaller practically. If the measurement data such as before dicing is smaller than probe coupling, the measurement accuracy will be degraded

This thermal noise is the value which is measured at the point of (a) in Fig. 2.

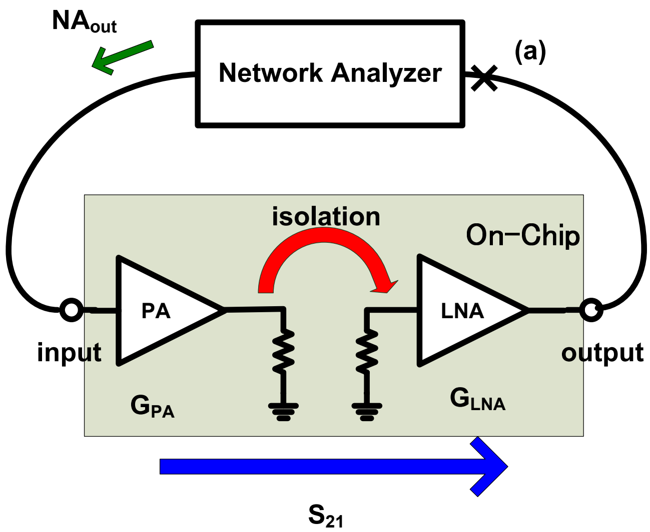

Fig. 2. Measurement setup.

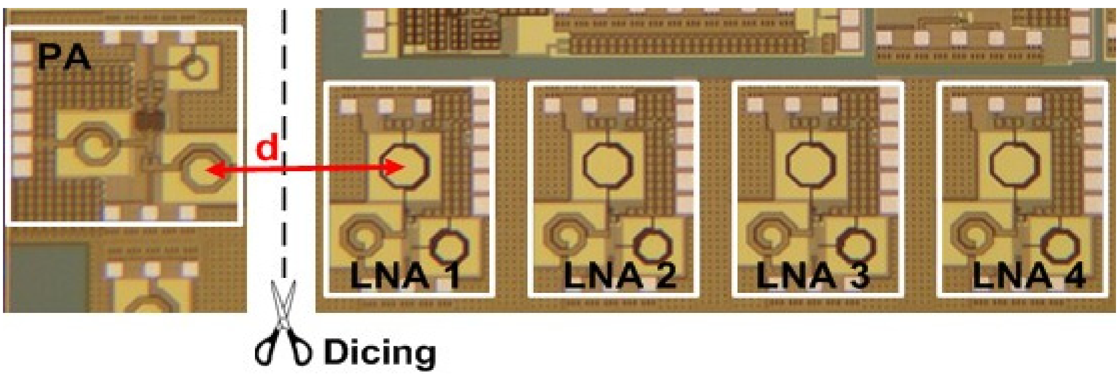

Fig. 3. Chipmicrograph

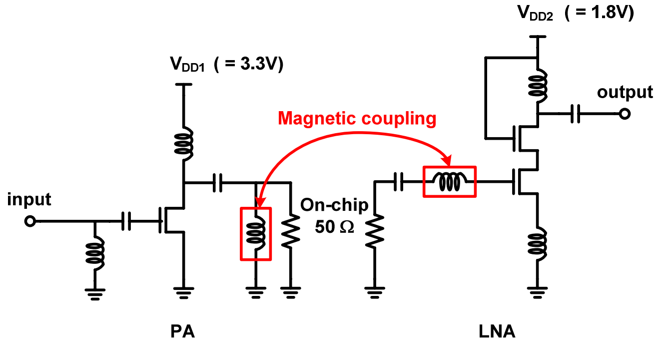

Fig. 4. Schematic of the PA and LNA

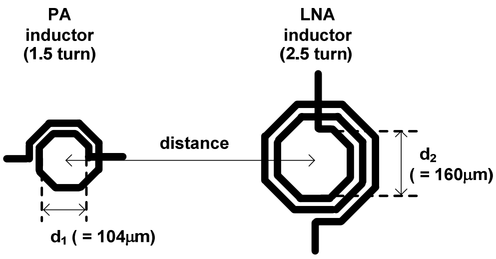

Fig. 5. The simulated inductor model.

B. Simulation method.

Fig. 4 shows the schematic of the PA and LNA. The inductor at PA output side and the inductor at LNA input side are thought the most impact on magnetic coupling. Thus, the inductors are simulated by an electromagnetic field simulator (Ansoft HFSS) to simulate magnetic coupling between PA and LNA. The distance between these inductors is set to the same distance as the chip measured. Fig. 5 shows the inductor model.

Moreover, a circuit simulator (Agilent simulator ADS) is used to calculate the S-parameter from the electromagnetic field simulation results of magnetic coupling of inductors, and S_{21} can be calculated.

III. Measurement Result

Fig. 3 shows the chip micrograph of the diced PA and LNAs. The distances between a PA and LNAs are configured as 0.74 mm, 1.55 mm, 2.37 mm, and 3.2 mm, respectively. The used PA and LNAs are implemented by 0.18 μm CMOS process and are designed for 5 GHz. The specification of the PA and LNA are summarized in Table I.

The chip is measured by using RF probes with external DC blocks at input and output nodes. The S-parameters are measured using Agilent E8361A Network Analyzer. The output power of network analyzer is -5 dBm.

Fig. 6 shows the measured S_{21} for each distance with simulation results. The dotted lines are simulation results and the solid lines are measurement results. The simulation results and the measurement results agree with each other except the case of 3.2 mm, and both of results have the peak at 5 GHz, because the amplifiers have the peak gain at 5GHz.

TABLE I
Specification of the Designed PA and LNA

	PA	LNA
Technology	0.18 μm CMOS process	
Frequency	5 GHz	
V_{DD}	3.3 V	1.8 V
Gain at 5 GHz	5.5 dB	15.1 dB
NF at 5 GHz		2.7 dB

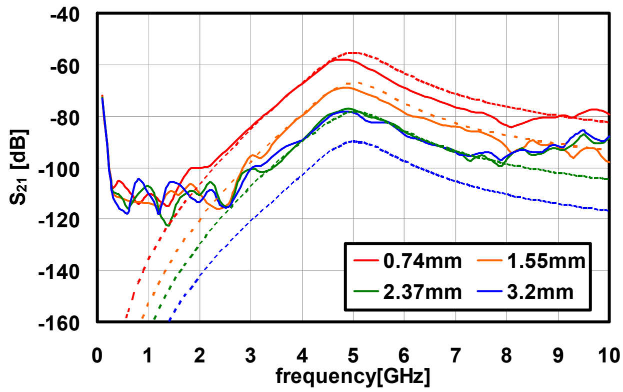

Fig. 6. Measured S_{21} versus frequency.

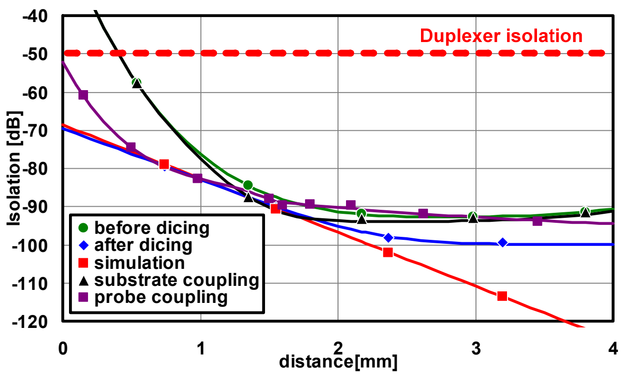

Fig. 7. Comparison of isolation at 5GHz.

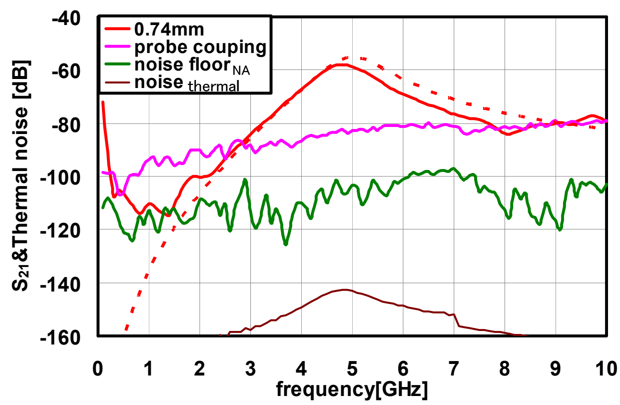

Fig. 8. Thermal noise, noise floor of network analyzer, and probe coupling versus frequency.

The simulated S_{21} is shifted to low value according to the distance. It means that the isolation between the PA and LNA depends on distance. The measured S_{21} is also shifted to low value, but the trend is stopped at 2.37 mm because of the influence of noise. The detailed analysis of various noises is described at the end of section III.

Fig. 7 shows the comparison of isolation at 5 GHz. The isolation value is calculated by Eq. (1). Moreover the probe coupling and the substrate coupling are also shown in this figure. The substrate coupling is calculated by Eq. (2) and others are the measurement data.

The green line, which is measured before dicing the chip, means the all of the Tx leakage from PA to LNA. Compared with the duplexer isolation, it is a lower value than the duplexer isolation from near 0.4 mm. On the average the distance between a PA and a LNA is more than 0.4 mm. Thus when the PA is integrated with other blocks, the increased Tx leakage is not a serious issue if it is placed with more than 0.4 mm distance.

The blue line, which is measured after dicing the chip, means the magnetic coupling of inductors. It is roughly in accordance with simulation results under 1.8 mm, and some errors are shown in the distance over 1.8 mm. The source of the error is the noise floor of the network analyzer. The detailed content is also provided at the latter part of section III.

The black line, which is calculated by Eq. (2), means the substrate coupling. Compared to the results of magnetic coupling, it is a bigger than the magnetic coupling all over the distance. Thus, substrate coupling is the most dominant factor.

The purple line is a measured probe coupling. It is measured on a probe station without anything related to the chip. When the chip is measured, the signal is generally carried through the chip. However, the chip does not exist in this time, so this probe coupling is the worst case. The probe coupling affects the measurement errors with the noise floor of network analyzer.

Fig. 8 shows the measured result in the case of 0.74 mm with several possible noise sources such as thermal noise, the noise floor of network analyzer, the probe coupling. The dotted line is the simulation result. The thermal noise is calculated by Eq. (3), (4) and the other noise sources are measured.

As shown in Fig. 6, there are some errors in the low frequency and the high frequency. In low frequency, the error is influenced by the noise floor of network analyzer. Thus, S_{21} does not decrease under the -110 dB. The probe coupling is larger than S_{21}, but it has to be considered that the measured probe coupling is the worst case. The reason why the magnetic coupling does not decrease under the -100 dB in Fig. 7 is the same which is affected by the noise floor of network analyzer. In high frequency, the error is influenced by the probe coupling, because the electromagnetic coupling between probes becomes larger at the high frequency. Thus, the measured S_{21} gets closer to the largest result of the probe coupling.

The calculated thermal noise is very small. Thus, the thermal noise is not a major error source in this measurement.

IV. Conclusion

On-chip Tx leakage is one of the most important issues for integrated power amplifiers, which is caused by substrate coupling, magnetic coupling, wire coupling, *etc*. In this work, the isolation between PA and LNA is measured, and the result reveals that the substrate coupling is most dominant in CMOS chips and the total isolation becomes smaller than duplexer isolation with more than 0.4 mm distance. Error in measurement is also analyzed, and the influence of probe coupling and noise floor of network analyzer is discussed.

Acknowledgement

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