A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply

Kenichi Okada, You Nomiyama, Rui Murakami, and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-28, Ookayama, Meguro-ku, Tokyo 152-8552 Japan
Tel.: +81-3-5734-2258, Fax: +81-3-5734-3764, E-mail: okada@ssc.pe.titech.ac.jp

Abstract

This paper proposes a dual-conduction class-C CMOS VCO for ultra-low supply voltages. Two cross-coupled NMOS pairs with different bias points are employed, which realize impulse-like current waveform to improve the phase noise in the low supply conditions. The proposed VCO was implemented in a standard 0.18 μm CMOS technology, which oscillates at a carrier frequency of 4.5GHz with a 0.2-V supply voltage. The measured phase noise is -104 dBc/Hz@1MHz-offset with a power consumption of 114 μW, and FoM is -187 dBc/Hz.

Keywords: *VCO, class-C, CMOS, low supply voltage, and impulse sensitivity function (ISF)*

Introduction

Recent wireless application, *e.g.*, wireless sensor network, requires low-power and low-voltage oscillators. The low supply voltage has a possibility to save power consumption even if it limits the signal amplitude. The transformer-feedback VCO has been proposed for a low-phase-noise and low-power operation, which performs with the comparable figure-of-merit to the state-of-art VCOs even at a supply voltage below the threshold voltage [1].

For further improvement of phase noise, the class-C VCO is significantly promising in terms of the effective ISF (impulse sensitivity function) [2]. However, the present class-C VCO cannot reduce the conduction angle with the limited supply voltage due to a start-up issue. Therefore, this paper proposes a dual-conduction class-C VCO to realize the reduced conduction angle by two cross-coupled NMOS pairs with different bias conditions as shown in Fig. 1. It will be shown that the proposed VCO can achieve a pseudo class-C operation at ultra-low supply voltages.

Dual-Conduction Class-C VCO

The class-C VCO can improve the phase noise by the concentrated current conduction at the small ISF region [2]. To keep the class-C operation, the following condition has to be satisfied.

$$V_{\rm DD} - A_{\rm t} > V_{{\rm gbias}n} - V_{\rm th} + A_{\rm t} > 0 \qquad (1)$$

where $A_{\rm t}$ is the voltage amplitude at drain nodes, $V_{{\rm gbias}n}$ is the gate bias of cross-coupled pairs, $V_{\rm th}$ is the threshold voltage, and $V_{\rm DD}$ is the supply voltage. Under the condition of Eq. (1), the phase noise of class-C VCOs can be expressed by the following equation [2, 3].

$$\begin{aligned}\mathcal{L}(\Delta\omega) &= 10\log\left[N\cdot\frac{1}{2q_{\max}^2\Delta\omega^2}\left(\Gamma_{R_{\rm t},{\rm rms}}^2\overline{i_{R_{\rm t}^2}}/\Delta f\right.\right. \\ &\quad \left.\left.+\Gamma_{i_{\rm ds1},{\rm rms}}^2\overline{i_{\rm ds1}^2}/\Delta f+\Gamma_{i_{\rm ds2},{\rm rms}}^2\overline{i_{\rm ds2}^2}/\Delta f\right)\right] \qquad (2)\\ &= 10\log\left[\frac{k_{\rm B}T(1+\gamma)R_{\rm t}}{NQ^2A_{\rm t}^2}\frac{\omega^2}{\Delta\omega^2}\right] \qquad (3)\end{aligned}$$

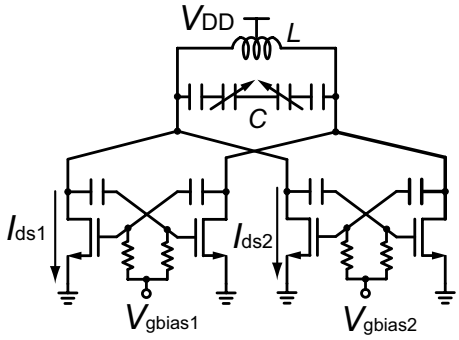

Fig. 1. Schematic of a dual-conduction CMOS class-C VCO.

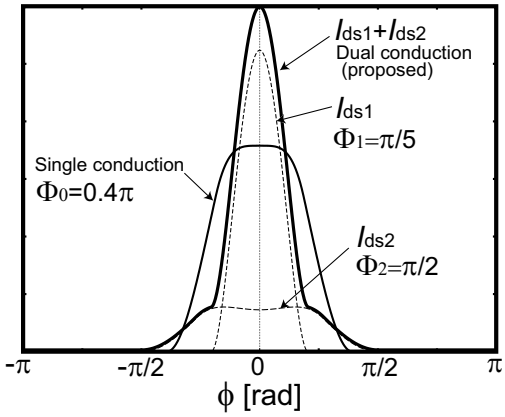

Fig. 2. MOS current waveform of single- and dual-conduction class-C VCOs under the same signal amplitude ($A_{\rm t} = 3/4 * V_{\rm DD}$, and $V_{\rm th} = 5/2 * V_{\rm DD}$).

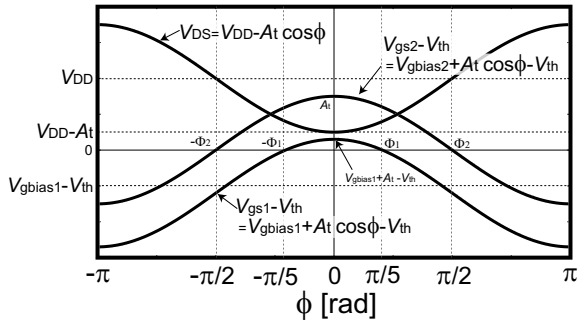

Fig. 3. Voltage waveform of the proposed VCO for drain and both gate voltages.

where N is the number of resonators (2 for differential VCOs), where $k_{\rm B}$ is Boltzmann's constant, T is the absolute temperature, γ is the MOS channel noise factor, and $R_{\rm t}$ is the tank impedance. Note that the phase noise of the proposed dual-conduction class-C VCO can also be expressed by Eq. (3).

According to Eq. (3), the methods to improve the phase noise are (1) increase of $A_{\rm t}$, (2) improvement of Q, and (3) reduction of $R_{\rm t}$ under the complete class-C operation. Moreover, the con-

duction angle should be reduced to improve the figure-of-merit [2, 3]. Fig. 2 shows current waveforms of the conventional single-conduction and the proposed dual-conduction VCOs. Here, the conduction angle $2\Phi_n$ is defined as $\cos(\Phi_n) = (-V_{\mathrm{gbias}n} + V_{\mathrm{th}})/A_{\mathrm{t}}$. Tank amplitude in voltage A_{t} should be less than V_{DD} for the class-C operation according to Eq. (1), which is severe especially at the low supply voltage. The overdrive voltage ($V_{\mathrm{th}} - V_{\mathrm{gs}}$) cannot also be reduced for the robustness of oscillation start-up.

Therefore, the proposed dual-conduction class-C VCO has two cross-coupled NMOS pairs with different conduction angles $2\Phi_1$ and $2\Phi_2$ as shown in Fig. 1. Fig. 3 shows voltage waveforms at drain and both gate nodes, which also explain the condition of class-C operation. In the proposed VCO, Φ_2 is designed as near $\pi/2$ for the robust start-up, and corresponding transconductance(β_2) is kept small to reduce total current consumption. Φ_1 can be kept small independently of the start-up robustness to improve the figure-of-merit, so the proposed VCO can achieve small conduction angles equivalently as shown in Fig. 2.

For example, in case of Figs. 2 and 3, Φ_1 and Φ_2 are $\pi/5$ and $\pi/2$, respectively, for the proposed dual-conduction VCO. Φ_0 is 0.4π for the conventional single-conduction VCO. V_{dd} is 0.2 V, Q is 10, and R_{t} is 400. The signal amplitudes A_{t} is kept equal by adjusting the transconductance. The phase noise, power consumption and FoM of the dual-conduction one are calculated as -109 dBc/Hz@1MHz at 5 GHz, 0.162 μW, and 191 dBc/Hz, respectively, -106 dBc/Hz@1MHz, 0.168 μW, and 188 dBc/Hz for the single-conduction one. 3 dB improvement in FoM can be confirmed in this condition, which is caused by the larger conduction angle of the single-conduction one under the low supply voltage condition.

Measurement Results

Fig. 4 shows a chip micrograph of test circuit. The chip size was 0.29 mm^2, excluding the pad and output-buffer area. The phase noise shown in Fig. 5 was measured at 0.2-V and 0.3-V supply voltages. The measured phase noise at the 0.2-V operation is -104 dBc/Hz@1MHz-offset with a power consumption of 114 μW. V_{gbias1} and V_{gbias2} are 0.45 and 0.55, respectively. The oscillation frequency is 4.5 GHz, and the phase noise corner is 200 kHz$\sim$300 kHz. The figure-of-merit(FoM) is 187 dBc/Hz. Table 1 summarizes performances of the conventional and the proposed VCOs, and the proposed VCO can perform at the 0.2-V power supply with the comparable FoM to the state-of-art VCOs.

Conclusion

The present paper has proposed and demonstrated a dual-conduction class-C VCO, which realizes impulse-shape current conduction even at the low supply voltage. The implemented VCO can operate at a 0.2-V power supply with the figure-of-merit of 187 dBc/Hz.

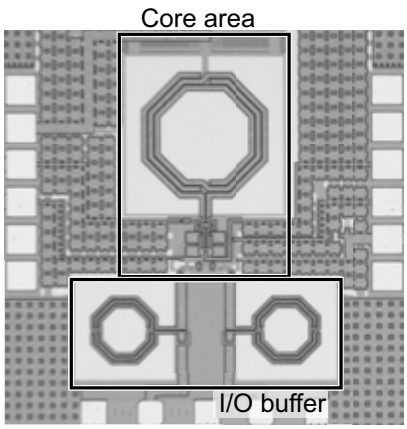

Fig. 4. Chip micrograph.

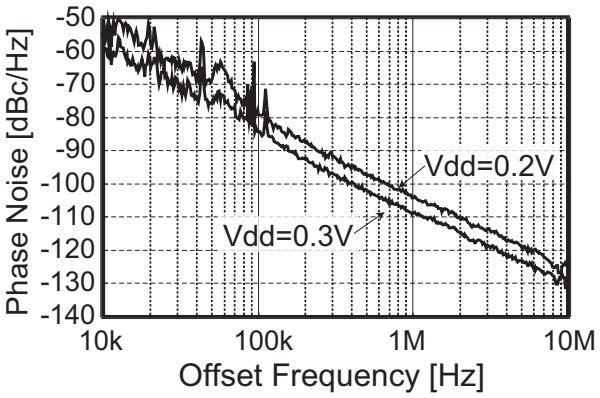

Fig. 5. Measured phase noise at the 4.5-GHz oscillation frequency.

Acknowledgements

This work was partially supported by MIC, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

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TABLE 1. Performance summary.

	[2]	[1]	[1]	**This work**	
Technology	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	
Supply voltage	1.0 V	0.5 V	0.35 V	0.3 V	**0.2** V
Power consumption	1.3 mW	0.57 mW	1.46 mW	0.159 mW	**0.114 mW**
Oscillation frequency	4.9 GHz	3.8 GHz	1.4 GHz	4.5 GHz	4.5 GHz
Phase noise	-130 dBc/Hz @3MHz-offset	-119 dBc/Hz @1MHz-offset	-129 dBc/Hz @1MHz-offset	-109 dBc/Hz @1MHz-offset	-104 dBc/Hz @1MHz-offset
FoM	196 dBc/Hz	193 dBc/Hz	190 dBc/Hz	190 dBc/Hz	187 dBc/Hz
Chip area	0.50 mm^2	0.23 mm^2	0.76 mm^2	0.29 mm^2	
Topology	Class-C (single)	TF	TF	Class-C (dual)	