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A 10-bit, 290fJ/conv. steps, 0.13mm², Zero-Static Power, Self-Timed Capacitance to Digital Converter

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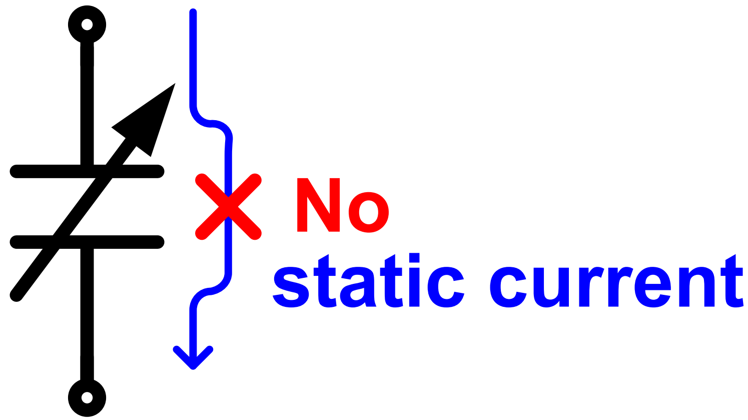
Contents

- Background
- Proposed Circuit Architecture
- Simulated and Experimental Results
- Conclusions

Background

- Increasing of researches in in-vivo medical system utilizing capacitive pressure sensor
  - Small size
  - High sensitivity
  - Robust structure



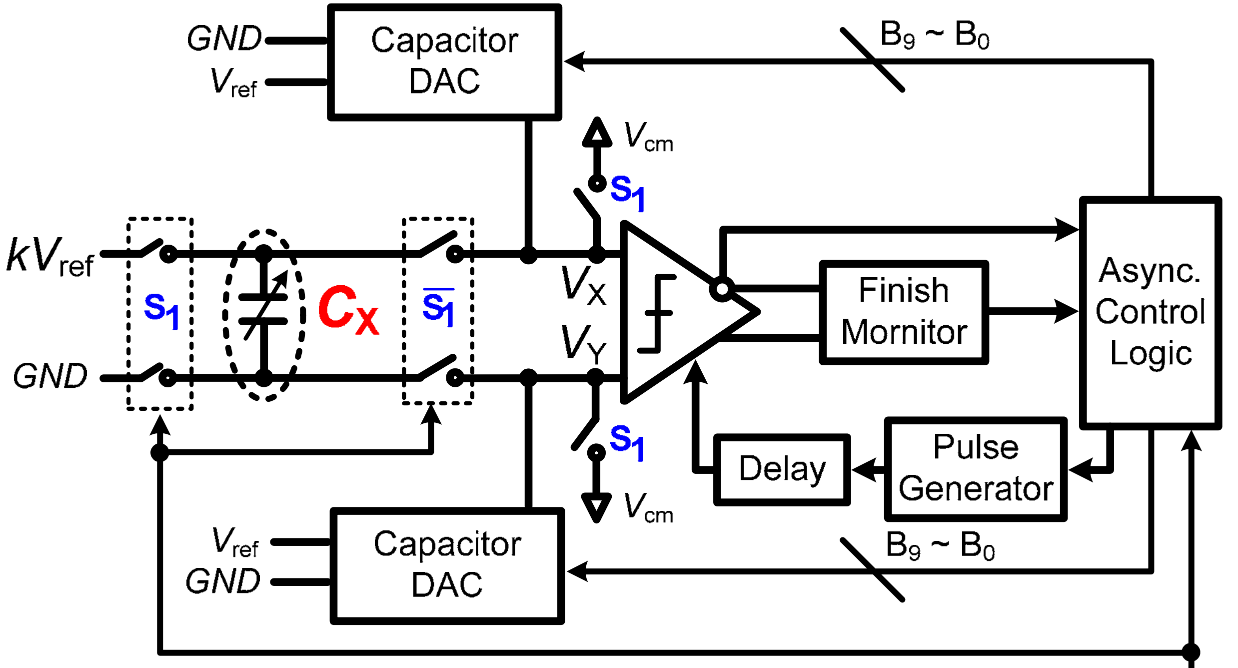
- A sensor interface to convert sensor capacitance to digital is indispensable

Capacitance to digital convert method

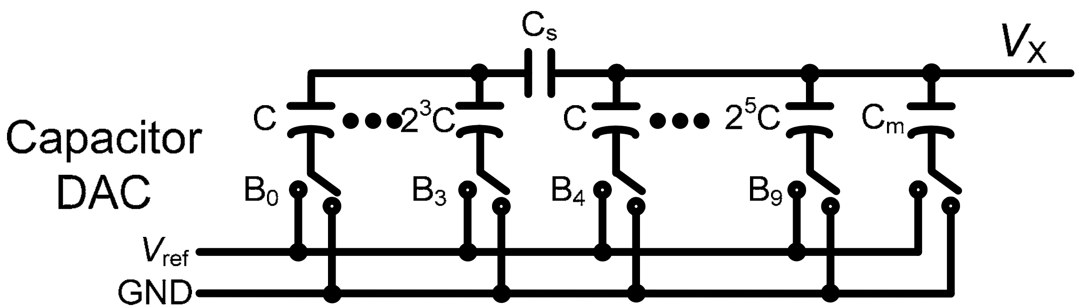
- Conventional method
  - Semi digital method [1,2]
    - ☹ Power, area of ADC
  - Direct convert method utilizing ΣΔ ADC [3]
    - ☹ Power of Opamp
  - Direct convert method utilizing single-ended SAR ADC [4]
    - ☹ Sensor capacitance variation
- Proposed a direct Capacitance to Digital Converter having differential architecture

[1] P. Bruschi, N. Nizza, and M. Piotto, *JSSC*, 2007 [2] X. Xu, X. Zou, L. Yao, and Y. Lian, *VLSI Circuits*, 2008
[3] J. O'Dowd, A. Callanan, G. Banarie, and E. C. Bosch, *Sensors*, 2005 [4] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, and A. Matsuzawa, *ASSCC*, 2007

Proposed Circuit Architecture



C_X : Capacitive Pressure Sensor



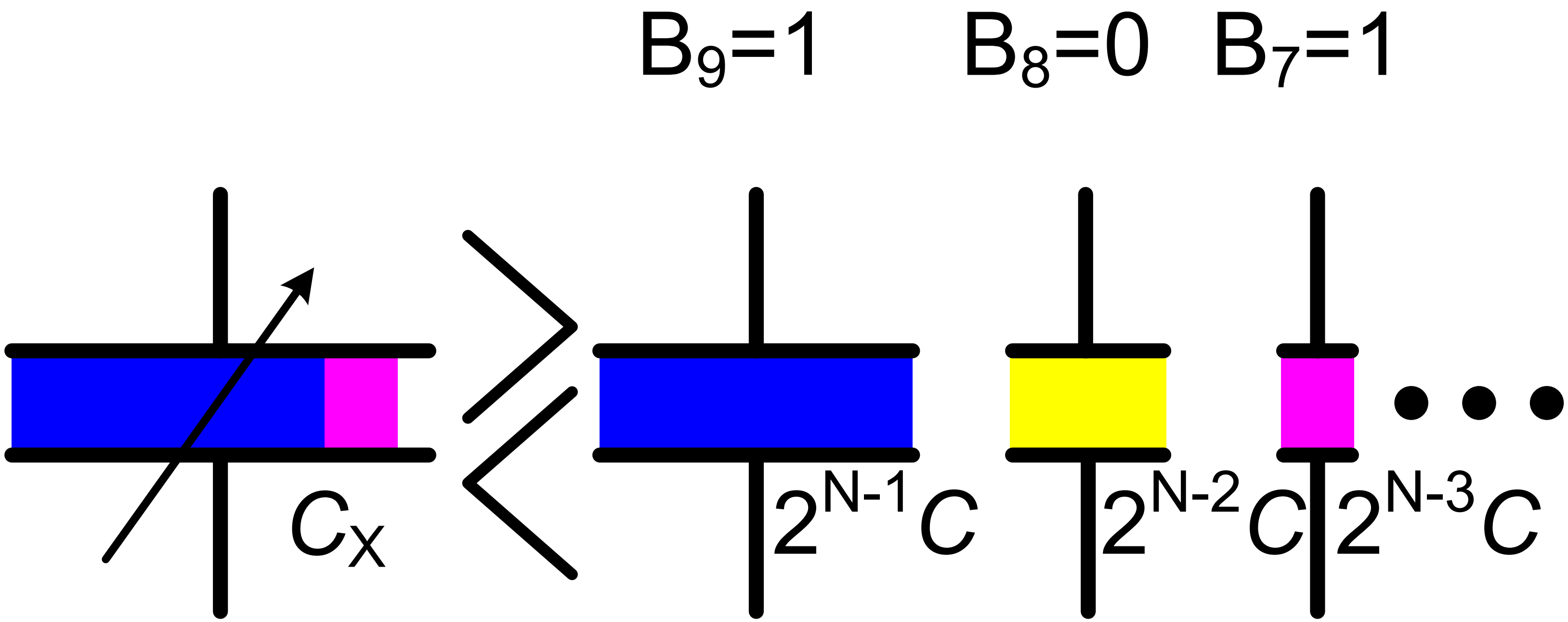
- Single-ended input but differential operation
- Asynchronous processing [5]
- Highly sensitive dynamic comparator [6]

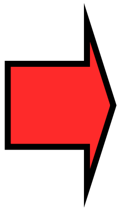
[5] S. W. M. Chen, and R. W. Brodersen, *JSSC*, 2006

[6] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, *ASSCC*, 2008

Operation principle

- Binary search algorithm
- Charge redistribution technique





Find the nearest sum of capacitance from DAC to sensor capacitance

Sampling phase

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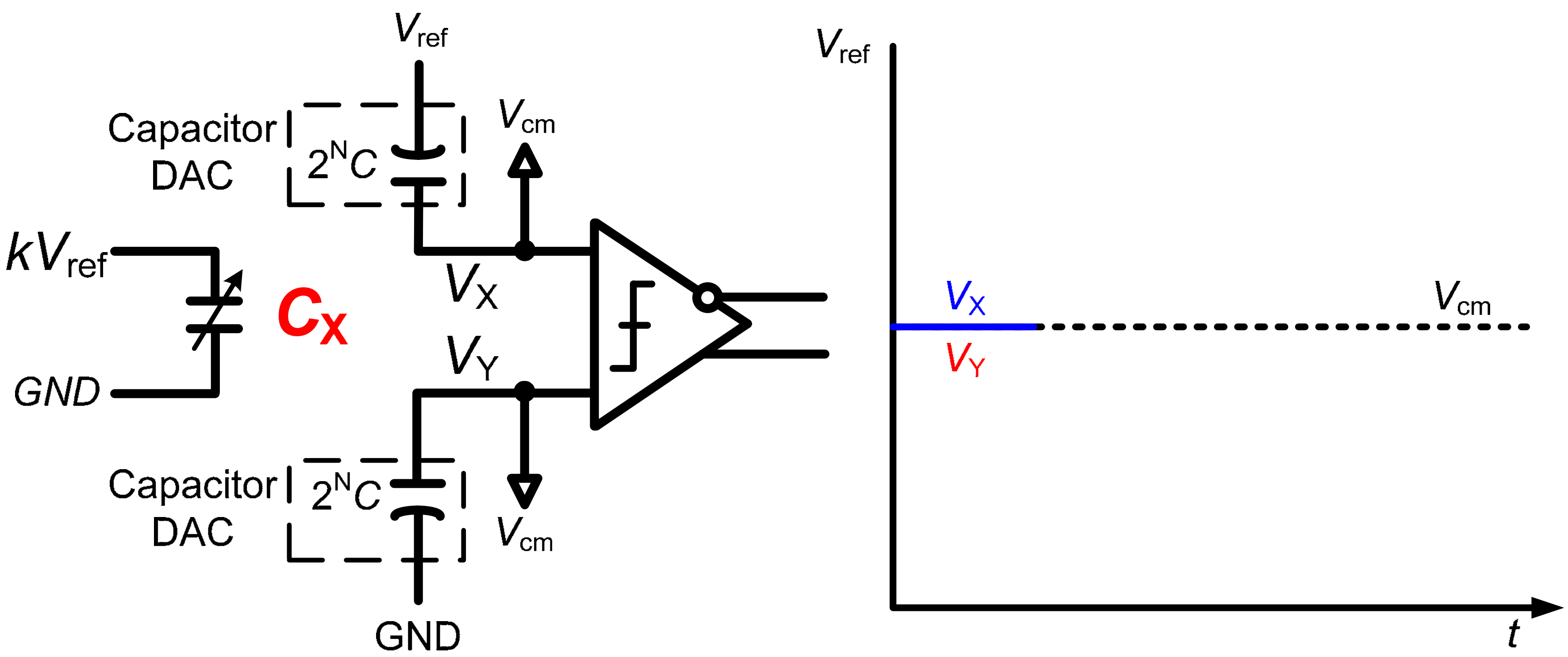
S_1:ON, $\overline{S}_1$:OFF



Store charge into the capacitor DAC and the capacitor sensor

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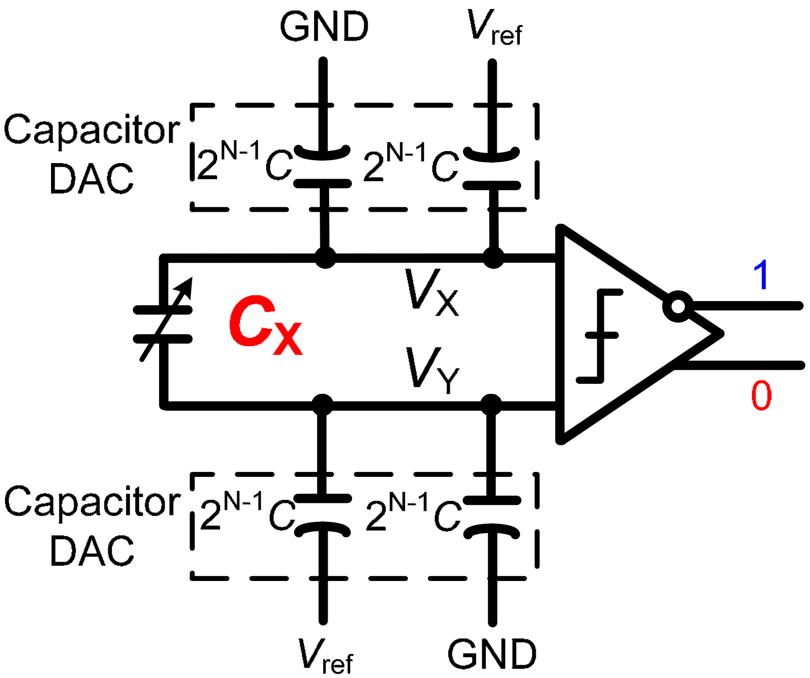
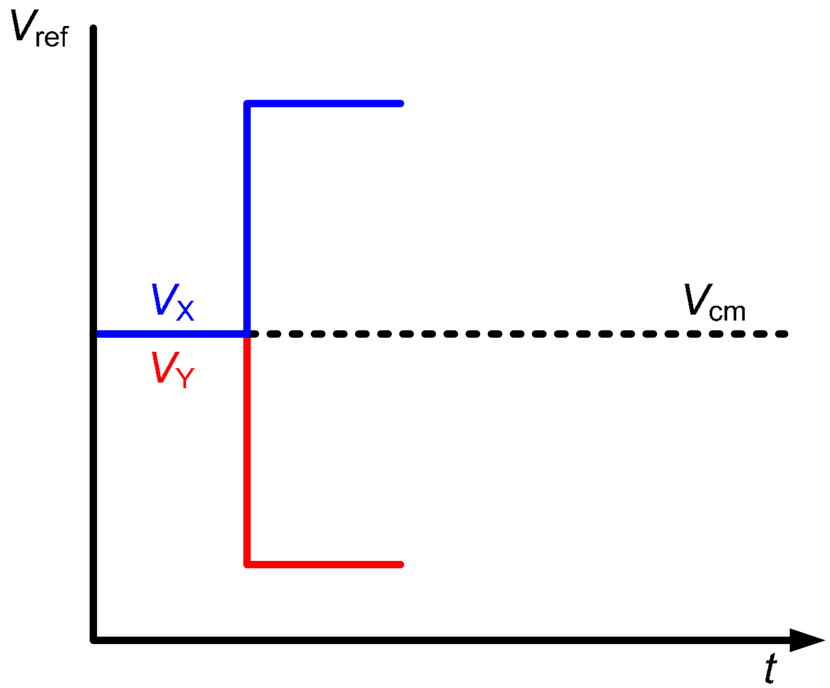
Conversion phase (MSB)

S_1:OFF, $\overline{S}_1$:ON

Capacitance > Charge > Voltage

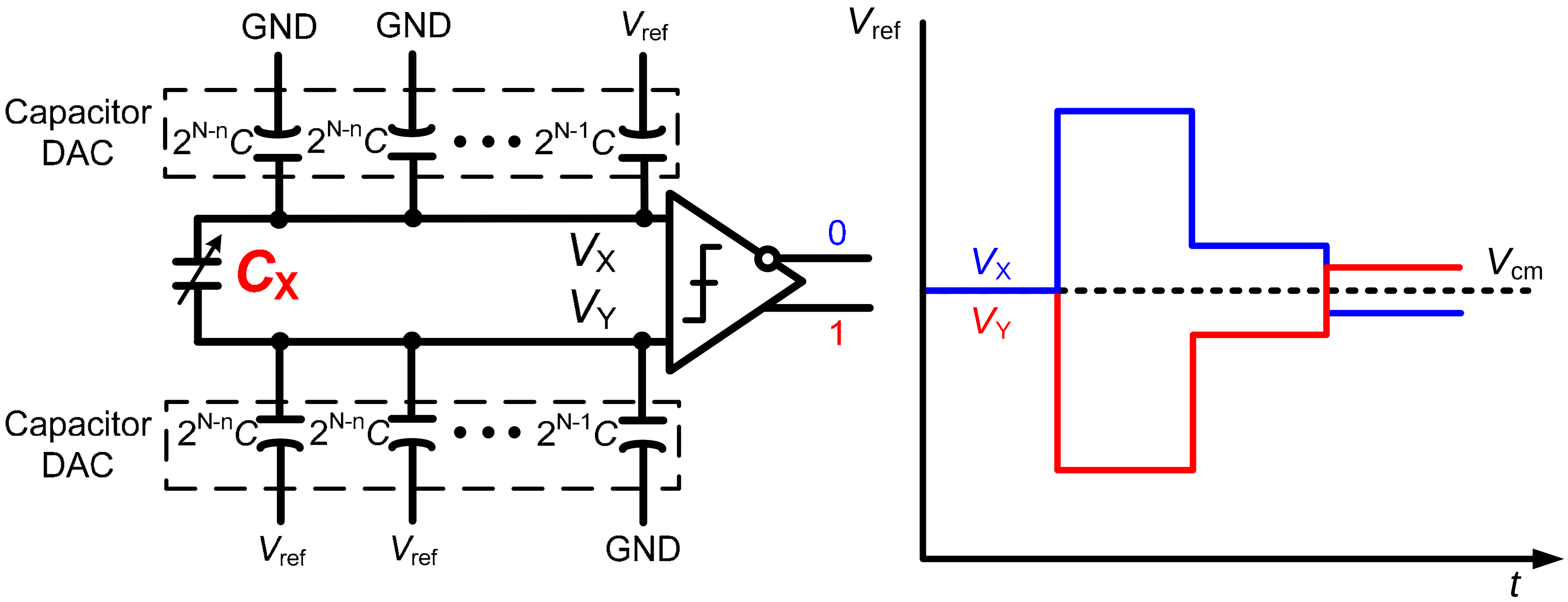




MSB is determined based on comparison result between V_X and V_Y

Conversion phase (nth bit)

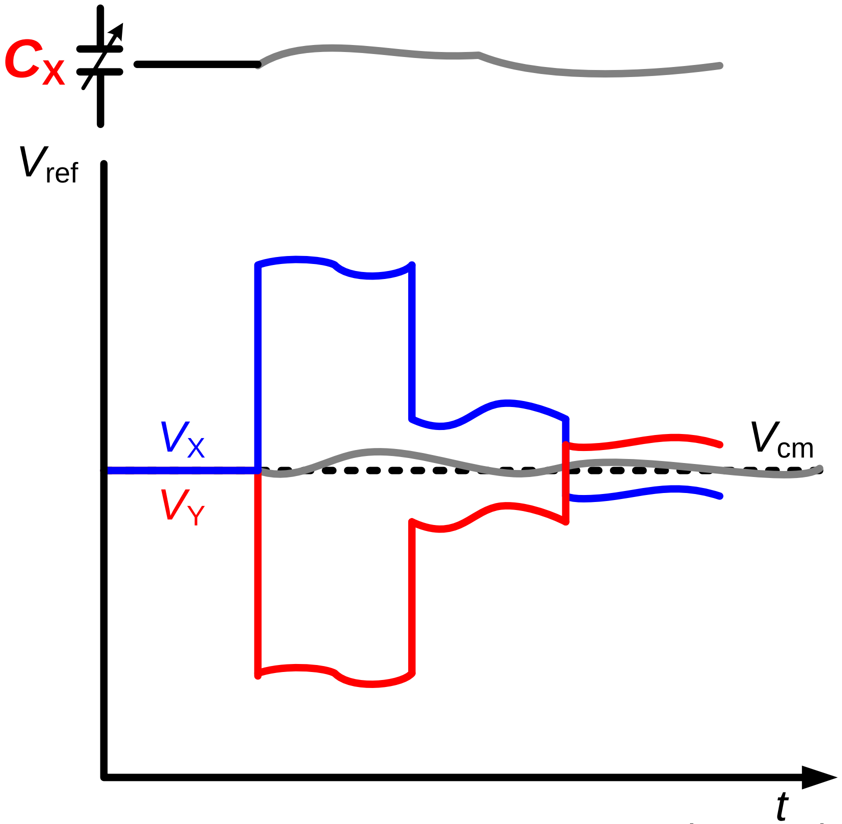
S_1:OFF, $\overline{S}_1$:ON



Reduce $V_X - V_Y$ and determine every bit step by step to LSB

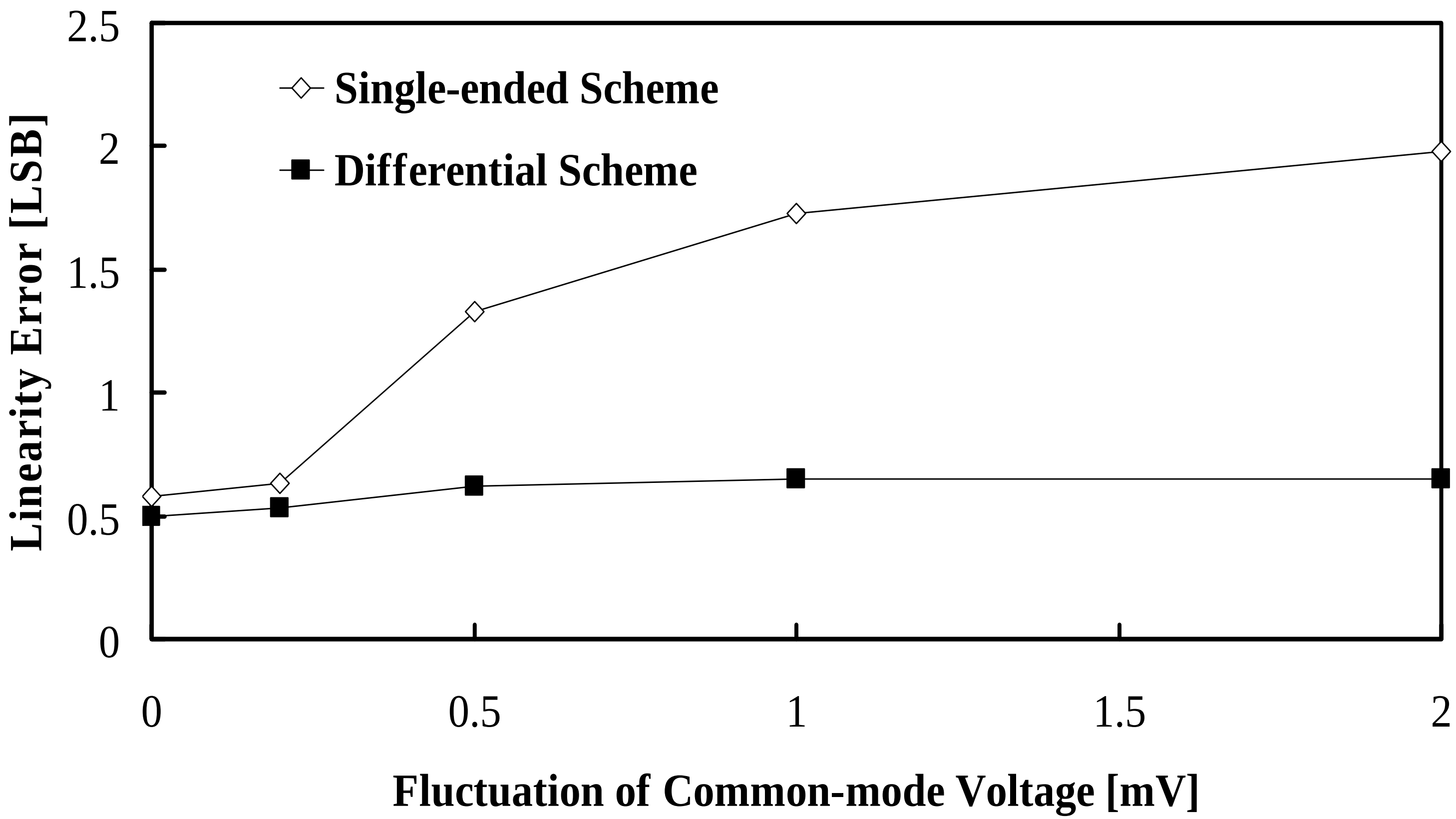
Merit of differential architecture

- Kickback noise of comparator
- Common-mode voltage fluctuation
- Sensor capacitance variation



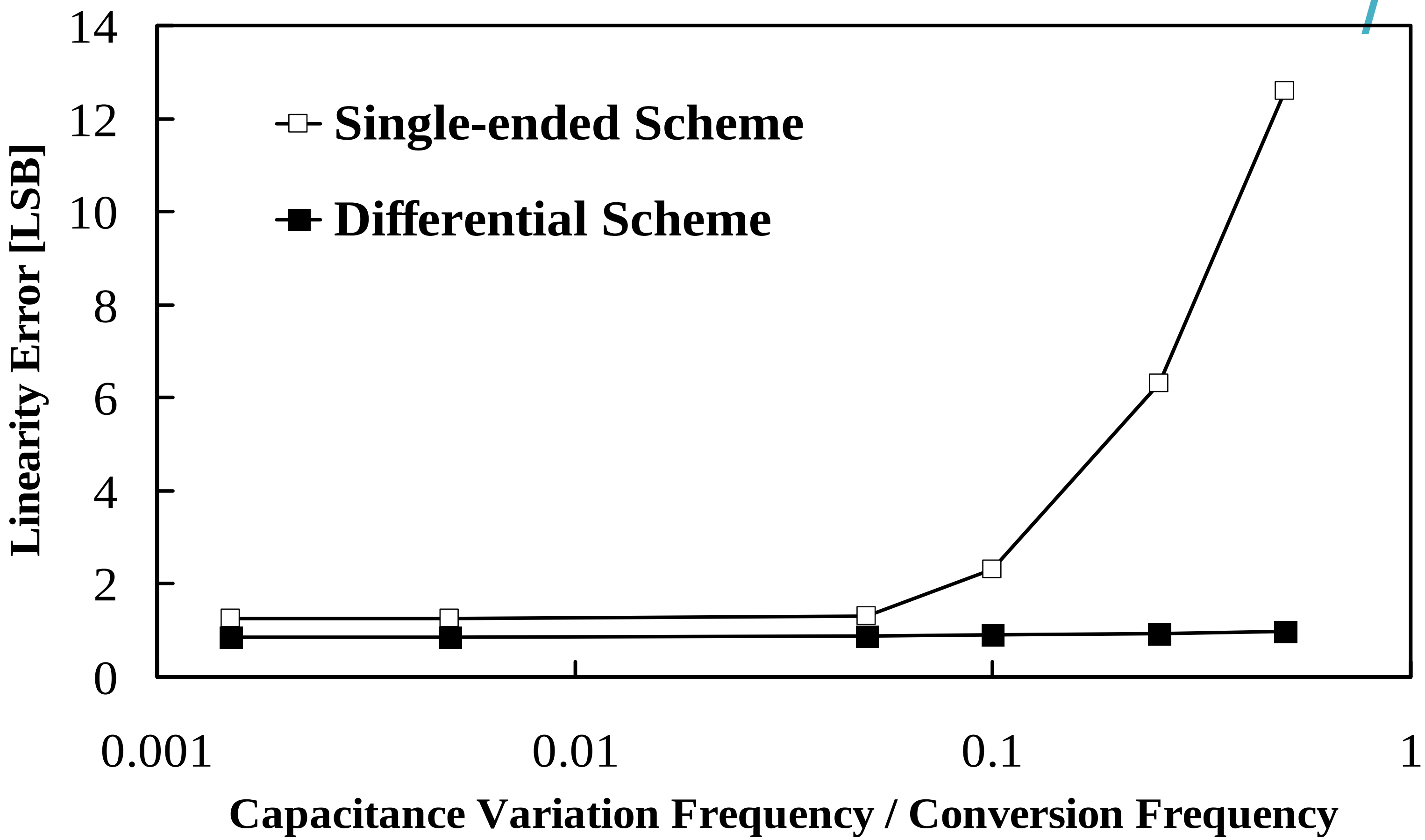
$V_X - V_Y$ is always fixed during conversion phase

Simulated result



Linearity of the proposed circuit is not affected from the common-mode voltage fluctuation

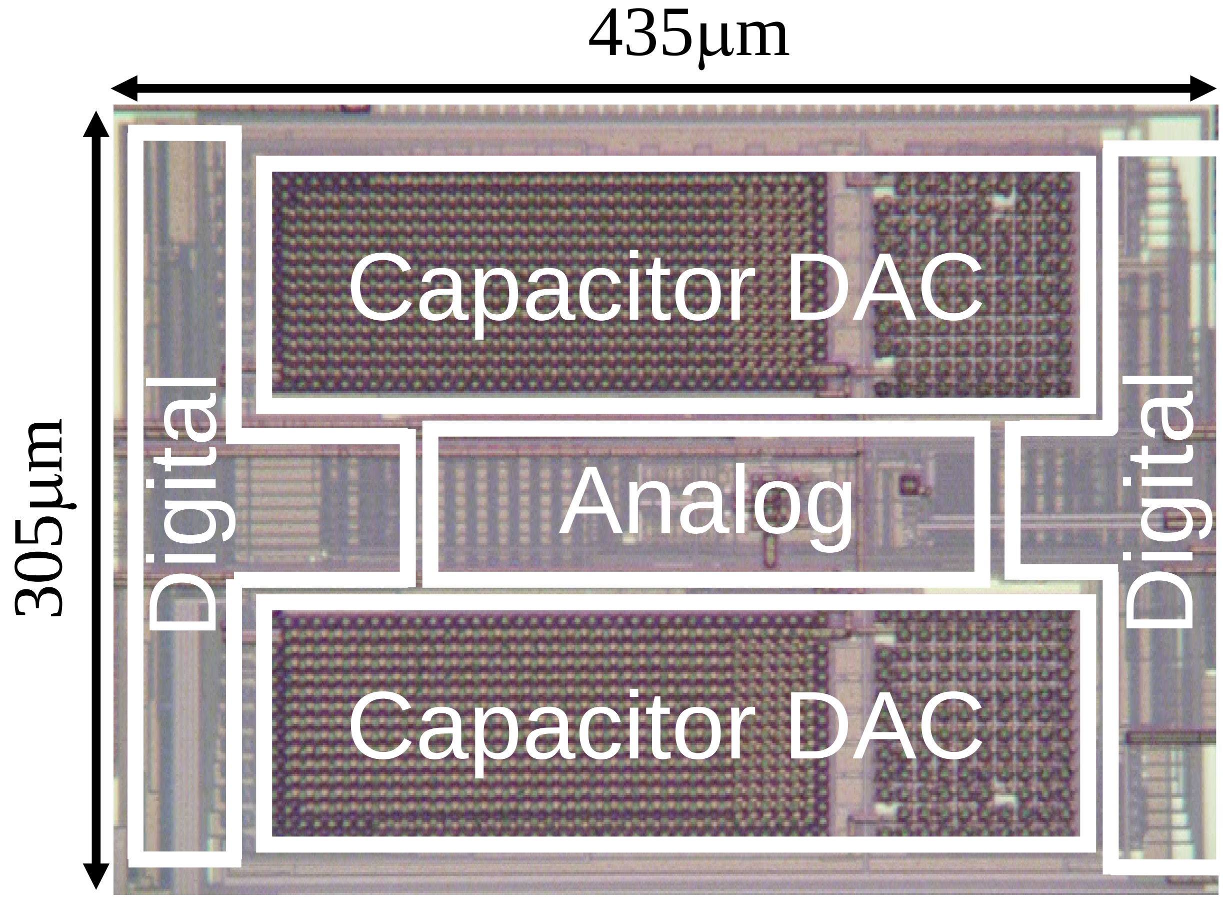
Simulated result



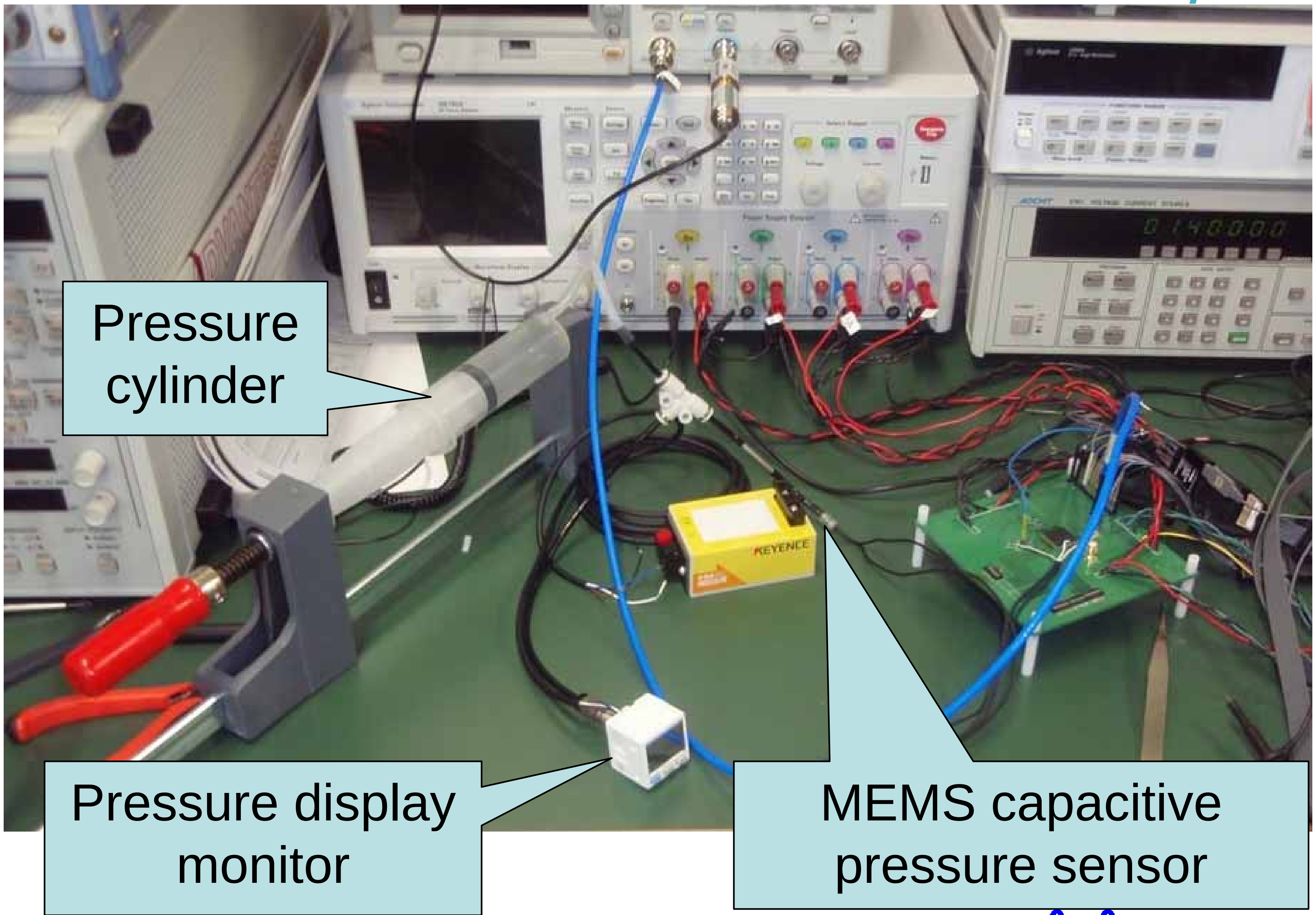
The proposed differential scheme keeps the linearity error sufficiently small

Prototype CDC

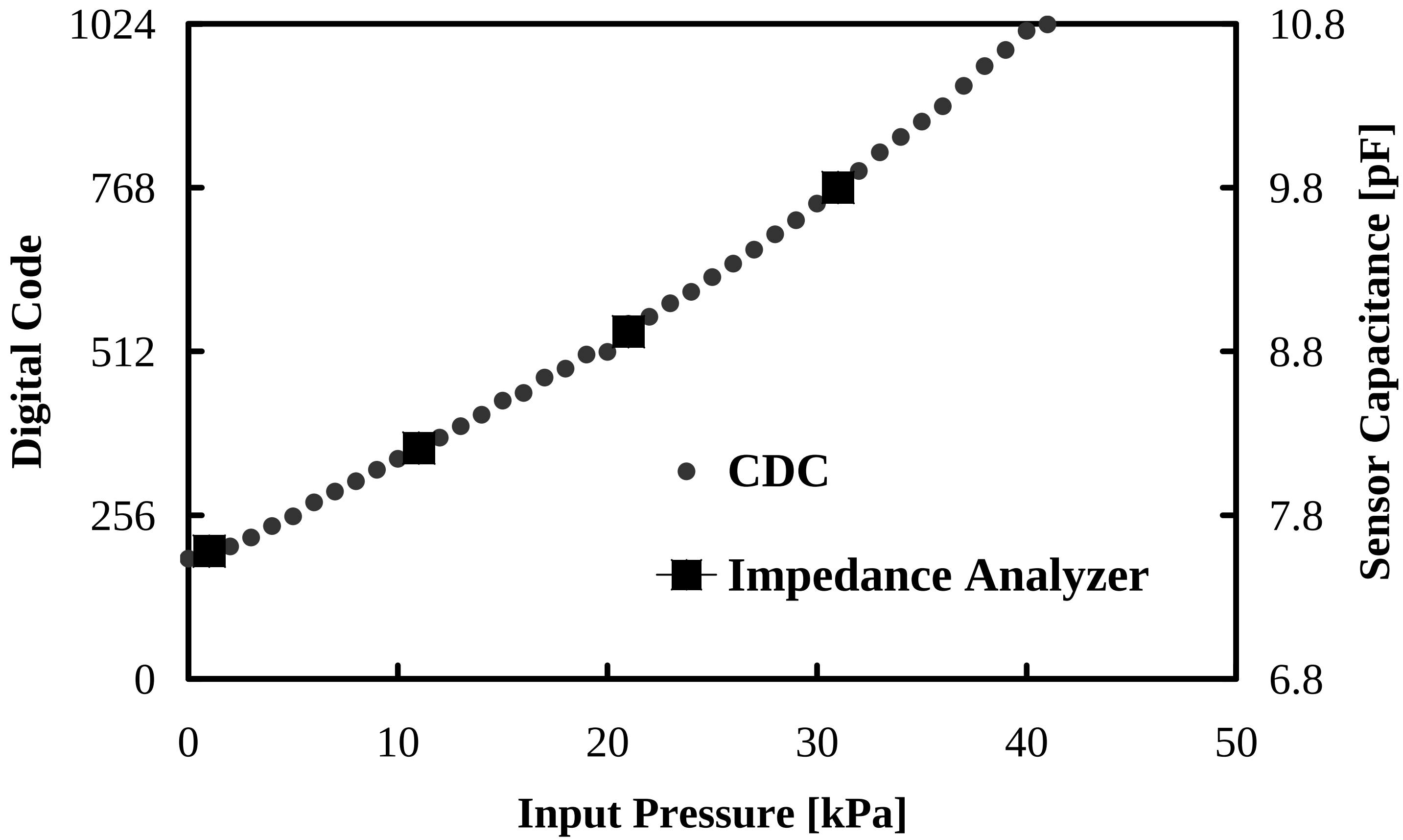
- 0.18μm CMOS 1Poly, 6Metal
- Core area $0.13mm^2$



Measurement environment



Experimental results



Digital code and estimated sensor capacitance vs. input pressure

The result fits with the characteristic of the real capacitive pressure sensor precisely

State of the art

	[1]	[2]	[4]	**This work**
Process Technology	0.35μm Bipolar	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage	3.3V	1V	1.4V	1.4V
Resolution (ENOB)	N/A	12Bit (10.2)	8Bit (6.83)	10Bit (8.25)
Current Consumption	4.8mA	895nA	169μA	**3nA**
Conversion Frequency	20kSps	1kSps	262kSps	30Sps
Size of Core	0.2mm^2	1mm^2	0.026mm^2 (C_m=3.6pF)	0.13mm^2 (C_m=10pF x 2)
Figure of Merit	N/A	760 fJ	5669 fJ	**290 fJ**

- Realized an ultra-low power capacitance to digital converter
- FoM = Power/(Frequency X 2^{ENOB})

  = 290 fJ/conv.step

Conclusions

- Ultra-low power sensor interface for in-vivo medical systems utilizing capacitive sensor
- Differential architecture
  - Small linearity error
- Prototype CDC
  - 10-bit
  - 0.18 μ m CMOS
  - 0.13mm^2
  - 3nA @30Sps, FoM : 290 fJ/conv.step
- Precisely measured data

Acknowledgment

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Thank You!

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