A 10-bit, 290fJ/conv. steps, 0.13mm^2, Zero-Static Power Self-Clocking Capacitance to Digital Converter

Tuan Minh Vo, Yasuhide Kuramochi, Masaya Miyahara, Takashi Kurashina and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27 Ookayama, Meguro-ku, Tokyo 152-8552 Japan
Tel/Fax: +81-3-5734-3764, E-mail: votuan@ssc.pe.titech.ac.jp

1. Abstract

This paper presents an ultra-low power 10-bit capacitance to digital converter. Full dynamic circuits realize zero-static power and ultra-low FoM of 290fJ/conv. steps. It, for example, consumes only 2nA at sampling frequency of 30Hz. A differential architecture keeps the linearity error small up to the Nyquist frequency of sensor capacitance variation. It doesn't require any clocks since it can generate clock signal self consistently and hence suitable for micro systems. The prototype was fabricated in 0.18μm CMOS process. Measured data fit with the real sensor characteristic precisely. These features are suitable for in-vivo medical systems or sensor-telemetry micro systems because of the ultra-low power and zero-static current operation with the high precision measure of pressure in asynchronous micro control systems.

Keywords: differential architecture, capacitance-to-digital converter and zero-static power.

2. Introduction

Recent researches in in-vivo medical systems utilizing capacitive pressure sensor are increasing greatly. The capacitive sensor is used because it has a small size, high sensitivity, robust structure and needs no static current. Also, a sensor interface having small-size, low-power and moderate resolution (8-10 bits) A/D converter is indispensable. There are several sensor interface architectures have been proposed so far as presented in [1-5]. However, power consumption and area of the entire circuit in these architectures are still large. This is due to the "semi-digital" solution in [1,2] which can not convert to a digital code directly, or due to power consuming operational amplifier in [2-4]. A small-size capacitive sensor interface having single architecture of direct capacitance-to-digital converter (CDC) has been proposed in [5]. However, the power consumption is large and the precision of conversion is degraded by sensor capacitance variation during conversion. In order to address these issues a small-size, an ultra low-power differential architecture of CDC is proposed in this paper. An asynchronous self-clocking scheme minimizes the power consumption of clock circuit and size of digital part [6]. Additionally, a dynamic comparator with higher sensitivity than in [7] is utilized to realize zero-static power consumption.

3. Circuit Architecture

The proposed circuit incorporates only one off-chip capacitive pressure sensor C_X, two identical capacitor DACs, a comparator, an asynchronous logic and opposite phase switches S_1, $\overline{S}_1$ as shown in Fig. 1. The circuit operates in two phase, based on binary search algorithm with a charge redistribution technique in [5].

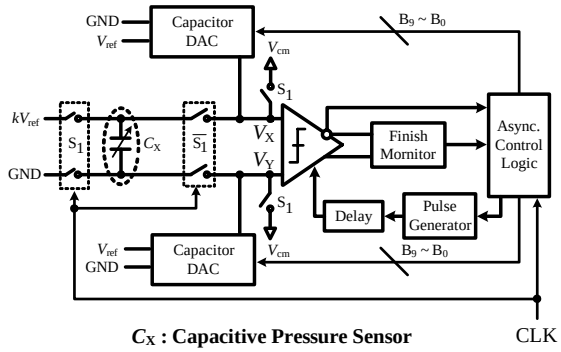

Fig. 1. Simplified block diagrams of the proposed CDC architecture and inside capacitor DAC

In the single architecture, determination of every bit is based on comparison result between the capacitor DAC output and the common-mode voltage V_{cm}. Thus, the DC level of the capacitor DAC output must be kept equal to V_{cm}. However, if the sensor capacitance varies in the conversion phase, this DC level will deviate from V_{cm}. Thus, this causes a conversion error.

The proposed differential architecture releases the sensor capacitance variation equally into two capacitor DAC outputs. In the sampling phase, switch S_1 is turned on and switches of bottom plates of the capacitor DAC are connected to V_{ref} or GND to store charge. In the conversion phase, switch S_1 is turned off. The voltage $V_X - V_Y$ at nth bit determination is defined as follow:

$$V_X - V_Y\big|_n = 2\frac{kC_{X\_sam} - \frac{C}{16}\sum_{m=0}^{n} 2^m B_m}{2C_{X\_con} + \left[C_m + \frac{C}{16}\sum_{m=0}^{9} 2^m\right]} V_{ref} \quad (1)$$

where C is a unit capacitance, C_{X_sam}, C_{X_con} are sensor capacitances in the sampling phase and conversion phase, respectively. All of bits are evaluated step by step to make the voltage $V_X - V_Y$ approaching zero. From Eq. (1), the comparison result is just determined by the numerator and not affected from the sensor capacitance variation in the conversion phase C_{X_con}. Additionally, the differential architecture also reduces kickback noise, common-mode voltage fluctuation. The asynchronous self clocking

TABLE 1
Performance comparison of this work and other presented design

	Reported in [2]	Reported in [3]	Reported in [5]	This work
Process Technology	0.35μm Bipolar	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage	3.3V	1V	1.4V	1.4V
Resolution (ENOB of ADC)	N/A	12Bit (10.2)	8Bit (6.83)	10Bit (8.25)
Total Current Consumption	4.8mA	895nA	169μA	2nA
Conversion Frequency	20kSps	1kSps	262kSps	30Sps
Size of Core	0.2mm^2	1mm^2	0.026mm^2 (C_m = 3.6pF)	0.13mm^2 (C_m = 10pF x 2)

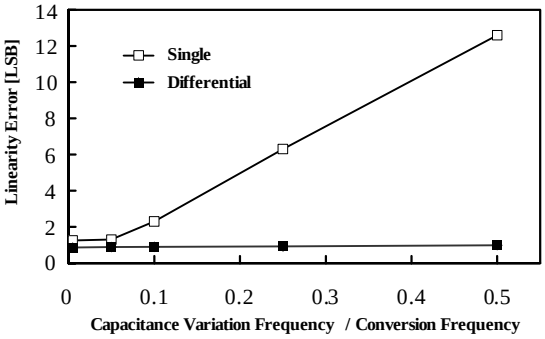

Fig. 2. Linearity error due to capacitance variation in conversion phase for single and differential schemes

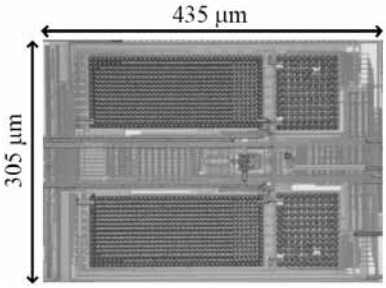

Fig. 3. Die photo micrograph

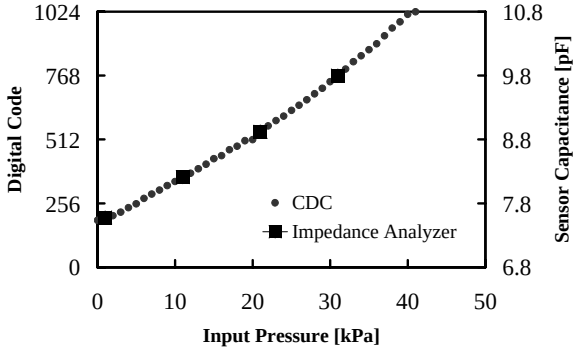

Fig. 4. Digital code and estimated sensor capacitance vs. input pressure

scheme is introduced to minimize the power consumption of the clock circuit and to realize asynchronous control by micro controller.

More highly sensitive dynamic comparator is required to realize higher resolution for this capacitive sensor application than the conventional SAR ADCs. This is because $|V_X - V_Y|$ is lowered by the sensor capacitance. Therefore, in this circuit, we increased capacitances between two latch stages of the comparator in [7].

Furthermore, the ranging capacitor array C_m is increased to cancel the stray capacitance at air pressure completely. Fig. 2 shows simulated linearity error caused by capacitance variation in conversion phase for single and differential schemes. Conventional single scheme degrades linearity so much. In contrast, the proposed differential scheme keeps the error sufficiently small. Fig. 3 shows the die photo micrograph.

4. Experimental Results

Experimental result of the conversion from capacitance of the capacitive pressure sensor to digital code by the proposed CDC is demonstrated in Fig. 3. Abscissas axis is the pressure applied to the capacitive pressure sensor; the left and the right ordinate axis are the output digital code converted by the CDC and the capacitance measured by impedance analyzer (4294A: Agilent), respectively. The result fits with the characteristic of the real capacitive pressure sensor precisely.

The prototype consumes only 6.3μA at 100kSps and 3nA at 30Sps. The FoM is about 290fJ/conv. steps.

Since a conventional sampling frequency of capacitive pressure sensor for biomedical applications and environment monitoring is several ten Hz, this small current consumption at low conversion frequency is very effective for these applications, in particular the in-vivo sensor telemetry systems.

Table 1 summarizes the prototype's performance and compares with other presented works. This work is superior in ultimate low power, reasonable occupied and suitable for microcontroller systems because of the asynchronous self-clocking technique.

Acknowledgment

This work was partially supported by MEXT, MIC, and VDEC in collaboration with Cadence Design Systems, Inc.

References

[1] D. D. Venuto, and B. Riccò, *Microelectronics Journal 37*, pp. 1610-1619, 2006.

[2] P. Bruschi, N. Nizza, and M. Piotto, *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1884-1891, Sep. 2007.

[3] X. Xu, X. Zou, L. Yao, and Y. Lian, *Proc. Symp. VLSI Circuits*, pp. 78–79, June. 2008.

[4] J. O'Dowd, A. Callanan, G. Banarie, and E. C. Bosch, *IEEE Sensors*, pp. 951-954, Oct. – Nov. 2005.

[5] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, and A. Matsuzawa, *IEEE Asian Solid-State Circuits Conference*, pp. 244-247, Nov. 2007.

[6] S. W. M. Chen, and R. W. Brodersen, *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669-2680, Dec. 2006.

[7] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, *IEEE Asian Solid-State Circuits Conference*, pp. 269-272, Nov. 2008.