R5-11 Asynchronous Differential Capacitance-to-Digital Converter for Capacitive Sensors

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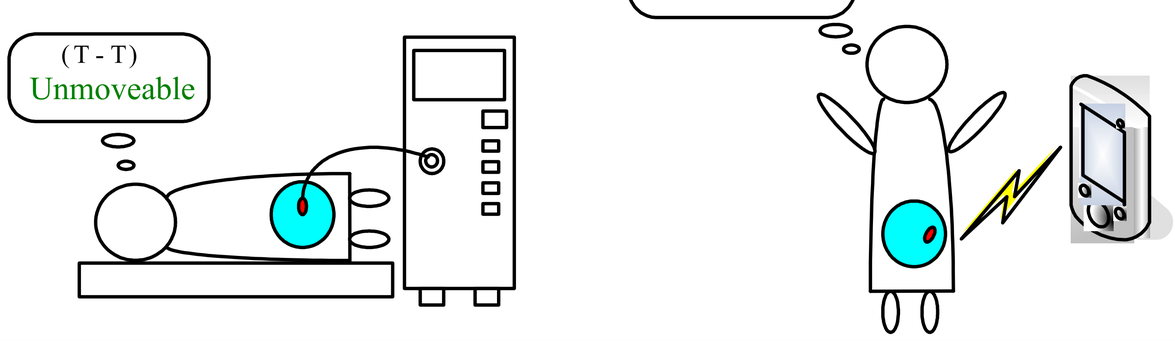
1. Background

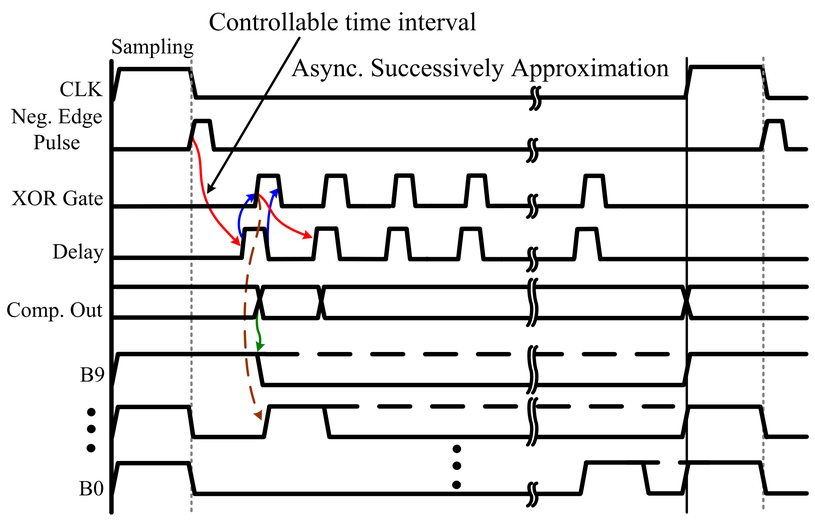
1. Increasing of research activities in low invasive diagnosis systems recently
2. The system needs to be very small size and low power
3. Utilizing of capacitive sensor in the system

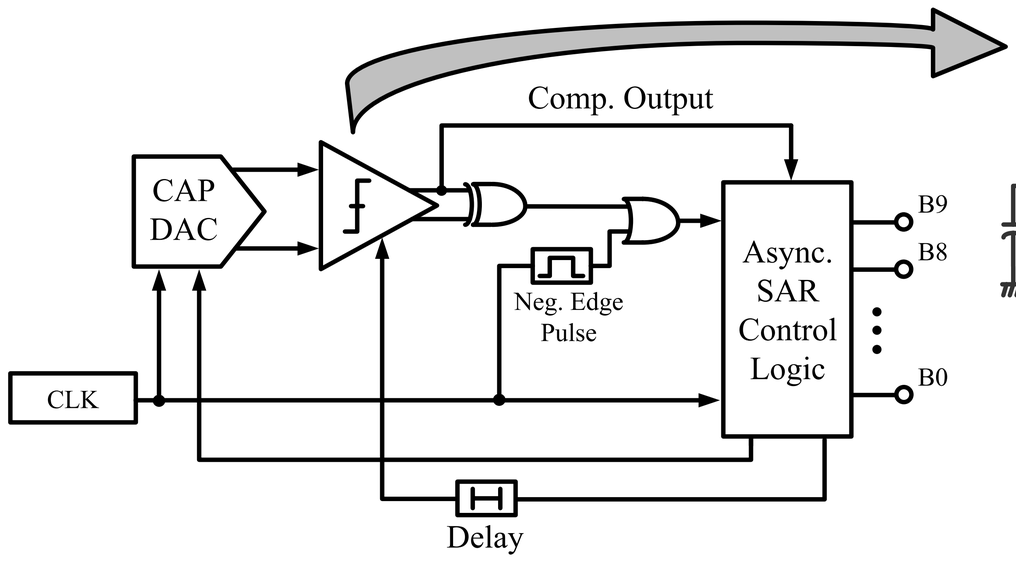
Ex. Application

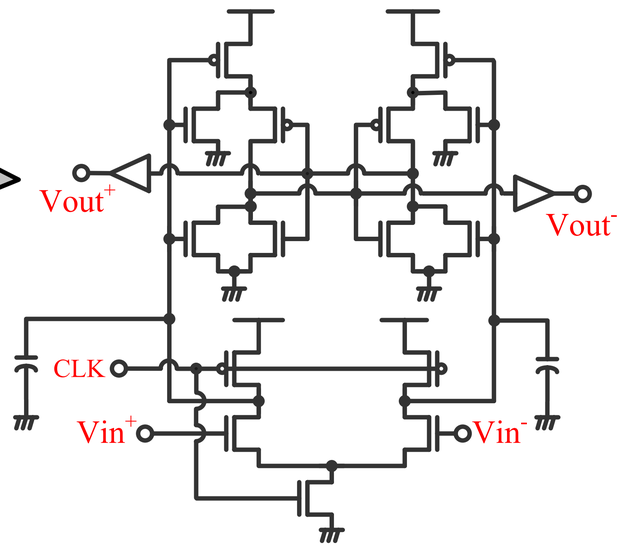


2. Asynchronous Processing and Dynamic Comparator

1. Lower speed clock $f_{CLK} = f_{Sampling}$
2. Intermittent movement

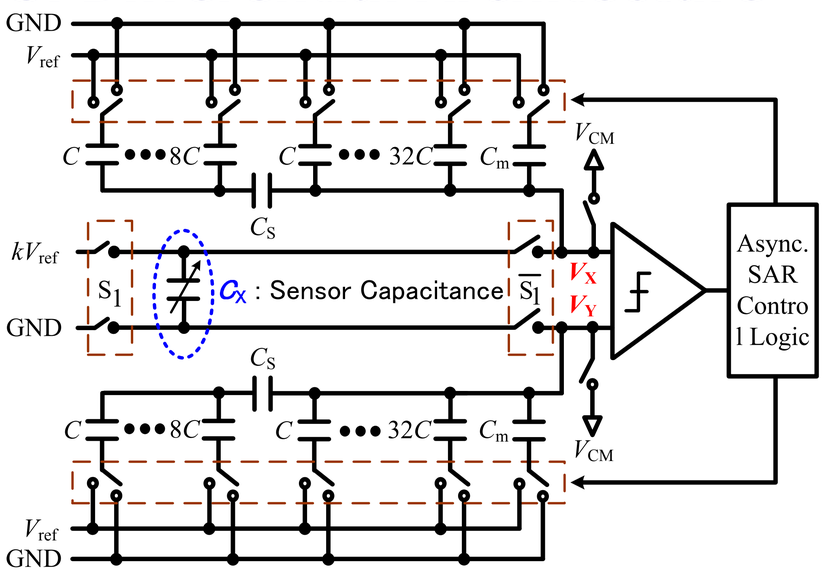






1. No static current
2. High sensitivity

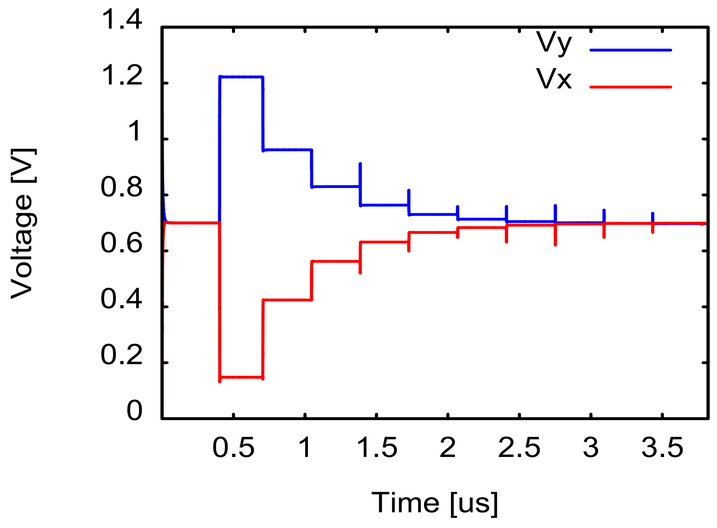
3. Differential Architecture

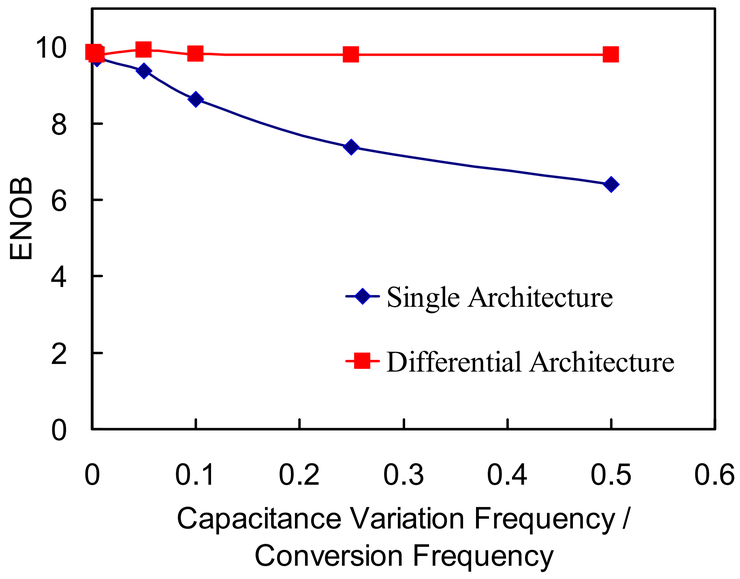


$$V_X - V_Y = \frac{(2^9 B_9 + \ldots + 2^n B_n)\frac{1}{2^4}C - kC_{X\_sam}}{2C_{X\_con} + \left[C_m + 2^5 C + \ldots + C + \frac{C_S(2^3 C + \ldots + C)}{C_S + 2^3 C + \ldots + C}\right]} 2V_{ref}$$

1. Define every bit step by step based on comparison result of V_X and V_Y
2. The comparison is not affected from C_{X_con} during conversion phase
3. Higher immunity to Vcm fluctuation, noise… than single-ended architecture

4. Simulation Results





Technology	180 nm CMOS
Supply Voltage	1.4 V
Resolution	10 Bit
Current Consumption	29.7 μA (with clock) 8.45 μA (w/o clock)
Conversion Frequency	262 kSps
Core Size	0.13 mm^2 (C_m = 10pF x 2)

5. Summary

1. A 10-bit very low power, small size direct Capacitance-to-Digital Converter is realized based on Charge Redistribution architecture
2. Asynchronous processing and a dynamic comparator lower power of the entire circuit
3. Differential architecture makes the circuit unaffected by the sensor variation