Asynchronous Differential Capacitance-to-Digital Converter for Capacitive Sensors

Abstract—**This paper proposed a 10-bit low-power asynchronous differential capacitance-to-digital converter (CDC) for capacitive sensor applications. The proposed differential architecture makes the circuit insensitive to variations of sensor capacitance. Additionally, asynchronous mechanism and a dynamic regenerative comparator are utilized to lower the overall power of the circuit. Simulation results show that the effective number of bits (ENOB) of the proposed circuit is improved by 3.3 bits at Nyquist frequency as compared with previous work. The power consumption at 262 kHz is 8.45 μA, which reducing from the previous work by 95% at the same frequency.**

I. INTRODUCTION

Recently, research activities in low invasive diagnosis systems are increasing greatly. Such systems can carry out measurements with less physical suffering and mental paint, so it is highly expected to be a future medical device. Because the system is attached to the body, it needs to be a system with very small size and low power. In this paper, we propose a low-power asynchronous differential capacitance-to-digital converter (CDC) for use in biotelemetry applications. For example, heartbeat monitoring of baby in the womb can be applied at home. In the system, heartbeat is monitored and converted to capacitance by a capacitive sensor. Then, this capacitance is converted to digital word, and data is sent to the hospital through a network. Inside the system, a micro-electro-mechanical systems (MEMS) capacitive sensor, which does not consume any static current, is used to convert heartbeat to capacitance. Then, for exact data acquisition of heartbeat through the MEMS capacitive sensor, a high resolution, insensitive to capacitance variation frequency in the order of kHz, very low-power CDC is an indispensable component.

There are various circuits that have been proposed so far for measuring the sensor capacitance, as reported in [1-9]. The technique used in [2,3] require an on-chip inductor and hence its size is very large. In [4,5], the applied technique is based on converting capacitance to voltage, and then this output voltage is read out by an analog-to-digital converter (ADC). However, large power consumption due to the operational amplifier (opamp) in the ADC is not appropriate for the system. In [6,7], a delta-sigma (ΔΣ) ADC is employed to convert capacitance directly to a digital word. However, these circuits also require large power consumption due to the opamp in the ADC.

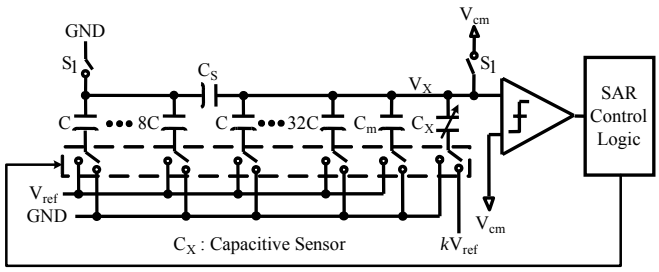

Fig. 1. Conventional capacitance-to-digital circuit

Thus, in [1], Tanaka *et al.* have proposed a low-power and small-area converter that converts sensor capacitance to digital word directly. The circuit is realized by incorporating an off-chip capacitive sensor and a ranging capacitor array into the successive approximation register (SAR) architecture shown in Fig. 1. Because the SAR converter consists of a capacitor digital-to-analog converter (DAC), a comparator, and a SAR without an opamp so its power consumption is very low and its size is very small when compare with other data converters.

In the circuit reported in [1], comparisons are performed in capacitance domain and hence it does not require an accurate reference voltage. Therefore, the circuit is highly compatible with biotelemetry applications. Beside that the degradation of the dynamic range of the conventional readout circuits using the SAR architecture in [8,9], caused by large parasitic capacitance of capacitive sensor, can be solved by the ranging capacitor array.

However, for applications in which variation frequency of sensor capacitance becomes much higher such in heartbeat

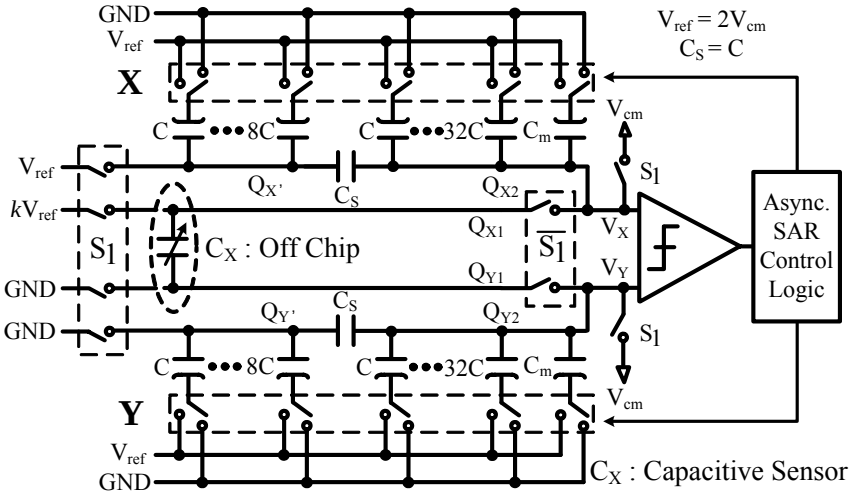

Fig. 2. The proposed differential CDC circuit

monitoring system, performance of the circuit is deteriorated extremely. This is due to the dependence of DC level at output of the capacitor DAC in this circuit on variation frequency of sensor capacitance. Also, overall power consumption of this circuit is still large due to the high speed internal clock circuit.

In this paper, to overcome these problems, a fully differential architecture is proposed to eliminate the influence of variation of sensor capacitance to DC level at output of the capacitor DAC. In addition, asynchronous mechanism presented in [10] is utilized to eliminate the need for a high speed clock circuit, and a dynamic regenerative comparator in [11] without drawing static current is applied, to lower the power consumption of the circuit.

II. CIRCUIT ARCHITECTURE

A. *Overview of the Proposed Circuit*

The proposed circuit incorporates an off-chip capacitive sensor C_X; two identical binary weighted capacitors arrays, including a main capacitor array and a ranging capacitor array C_m; a dynamic regenerative comparator; an asynchronous SAR control logic and switches as shown in Fig. 2. The fully differential architecture eliminates the influence of variation of sensor capacitance to DC level at the capacitor DAC output. The asynchronous mechanism eliminates the need for a high speed clock circuit, and the dynamic regenerative comparator without drawing static current lower the power consumption of the circuit.

B. *Operation of Fully Differential SAR CDC*

The proposed circuit operates in two phase, based on binary search algorithm with a charge redistribution architecture.

The first phase is the sampling phase. In this phase, switch S_1 is turned on, switch $\overline{S}_1$ is turned off and switches of bottom plates of capacitor arrays X and Y are connected to V_{ref} and GND, respectively. Then, the charge that is stored on the top plates of capacitor arrays X and Y and on both plates of capacitive sensor are:

$$Q_{X1} = kV_{ref}C_X, \quad Q_{X2} = -V_{cm}(C_{upper} + C_m + C_S) \tag{1}$$

$$Q_{Y1} = -kV_{ref}C_X, \quad Q_{Y2} = V_{cm}(C_{upper} + C_m + C_S) \tag{2}$$

$$Q_{X'} = V_{cm}C_S, \quad Q_{Y'} = -V_{cm}C_S \tag{3}$$

where C_{upper} is the total capacitance of the upper bits capacitor array at the right side of the scaling capacitors C_S, k is a scaling factor.

The second phase is the conversion phase. In this phase, switch S_1 is turned off and switch $\overline{S}_1$ is turned on; switches of bottom plates of C_m in capacitor arrays X and Y are connected to GND and V_{ref}, respectively, until the conversion is finished. The conversion phase begins with the conversion of the most significant bit (MSB). First, the MSB switch of capacitor array X is connected to GND and other switches in the array are connected to V_{ref}; in capacitor array Y, switches are connected in opposition to array X.

Applying the law of charge conservation to capacitor arrays X and Y:

$$Q_X = Q_{X1} + Q_{X2} = kV_{ref}C_X - V_{cm}(C_{upper} + C_m + C_S) \tag{4}$$

$$Q_Y = Q_{Y1} + Q_{Y2} = -kV_{ref}C_X + V_{cm}(C_{upper} + C_m + C_S). \tag{5}$$

During MSB conversion, V_X and V_Y can be expressed as below:

$$V_X = V_{cm} - \frac{C_m + C_{MSB} - kC_X}{2C_X + C_m + C_{upper} + \dfrac{C_S C_{lower}}{C_S + C_{lower}}} V_{ref} \tag{6}$$

$$V_Y = V_{cm} + \frac{C_m + C_{MSB} - kC_X}{2C_X + C_m + C_{upper} + \dfrac{C_S C_{lower}}{C_S + C_{lower}}} V_{ref}. \tag{7}$$

The voltage at the input node of the comparator is:

$$\left|V_X - V_Y\right| = 2\frac{C_m + C_{MSB} - kC_X}{2C_X + C_m + C_{upper} + \dfrac{C_S C_{lower}}{C_S + C_{lower}}}V_{ref} \quad (8)$$

where C_{MSB} is the MSB capacitance; C_{lower} is the total capacitance of the lower bits capacitor array at the left side of the scaling capacitor C_S.

Here, it is assumed that the sensor capacitance consists of an initial capacitance and an unknown capacitance caused by heartbeat

$$C_X = C_{X\_initial} + C_{X\_heartbeat}. \quad (9)$$

Because the ranging capacitor array C_m has the same value as the initial capacitance, Eq. (8) can be rewritten as:

$$\left|V_X - V_Y\right| = 2\frac{C_{MSB} - kC_{X\_heartbeat}}{2C_X + C_m + C_{upper} + \dfrac{C_S C_{lower}}{C_S + C_{lower}}}V_{ref}. \quad (10)$$

Obviously, V_X and V_Y become differential inputs to the comparator around a DC level of V_{cm}. The voltages of V_X and V_Y are compared mutually and the comparator output determines which input is in higher level. Comparing V_X with V_Y means the comparison of C_{MSB} and $kC_{X\_heartbeat}$. If C_{MSB} is smaller than $kC_{X\_heartbeat}$, the MSB is kept as "1", or else the MSB is set to "0". Correspondingly, the MSB switch of capacitor array X and Y is kept connected to V_{ref}, GND or reset to the other side.

When the conversion of MSB is finished, conversion of the next lower bit is carried out. Then, the same process is repeated to determine all bits.

Due to the law of charge conservation at both sides of scaling capacitor C_S, the voltage $|V_X - V_Y|$ at the input node of the comparator in each converting step is expressed as:

$$\left|V_X - V_Y\right| = 2\frac{C_{upper\_ON} + \dfrac{C_S C_{lower\_ON}}{C_S + C_{lower}} - kC_{X\_heartbeat}}{2C_X + C_m + C_{upper} + \dfrac{C_S C_{lower}}{C_S + C_{lower}}}V_{ref} \quad (11)$$

where C_{upper_ON} is the total capacitance between node V_X and GND, node V_Y and V_{ref} in the upper bits of capacitor array X and Y, respectively. This is the total capacitance for which the corresponding code is "1". Similarly, C_{lower_ON} is the total capacitance for which the code is "1" in the lower bits capacitor array. Therefore, all of capacitors in the array are evaluated step by step until the least significant bit (LSB) to make the voltage $|V_X - V_Y|$ approach 0. When all bits have been determined, the output digital code indicates the most nearest approximated value of the $kC_{X\_heartbeat}$. Due to the scaling factor k, full code of the digital word can match with the moving range of the sensor capacitance.

Comparing with the single-ended architecture used in [1,8,9], the voltage at the input node of the comparator in this circuit is enlarged. This improves the tolerance of the circuit to hysteretic of the comparator. Also, from Eq. (11), the comparison of V_X and V_Y is independent of the fluctuation of the common voltage of the comparator in conversion phase.

C. Analysis of Variation of Sensor Capacitance in Conversion Phase

In the single-ended SAR architecture, output of the capacitor DAC is compared with a fixed voltage in the entire period of conversion phase, so it also needs to keep the DC level of the DAC output fixed. However, in this architecture, the capacitive sensor is attached to capacitor DAC during conversion phase, so its variation may cause fluctuation of the DC level as proved below. For simplicity, it is assumed that there is no scaling capacitor C_S in capacitor DAC in Fig. 1. Thus, charge stored at node V_X in the sampling phase is:

$$\begin{aligned} Q_X &= C_{X\_sam}(V_{cm} - kV_{ref}) + C_{all}V_{cm} \\ &= V_{cm}(C_{X\_sam} + C_{all}) - kV_{ref}C_{X\_sam} \end{aligned} \quad (12)$$

where C_{X_sam} is the sensor capacitance in the sampling phase, C_{all} is the total capacitance of the capacitor DAC.

In conversion phase, due to the law of charge conservation, the charge that is stored at node V_X is:

$$Q_X = (C_{X\_con} + C_{all})V_X - C_{ON}V_{ref}. \quad (13)$$

Then

$$V_X = \frac{2C_{X\_sam} + C_{all}}{2C_{X\_con} + C_{all}}V_{cm} - \frac{C_{ON} - kC_{X\_sam}}{2C_{X\_con} + C_{all}}V_{ref} \quad (14)$$

where C_{X_con} is the sensor capacitance during the conversion phase, C_{ON} is the capacitance for which the corresponding code is "1".

If the variation frequency of the sensor capacitance is much lower than the conversion frequency, it can be approximated by:

$$C_{X\_con} = C_{X\_sam}. \quad (15)$$

Thus, the DC level of V_X is equal to V_{cm} and the comparison result is not affected. However, when the ratio of variation frequency of the sensor capacitance and the conversion frequency becomes large, Eq. (15) will be inexact. Therefore, it will cause fluctuation of the DC level of the DAC output during the conversion phase. Therefore, it will cause errors in the comparison result and deterioration of the ENOB.

A differential architecture reduces this effect by releasing the variation of the capacitive sensor into differential output of the DAC. In the proposed differential CDC:

$$\begin{aligned} Q_X &= C_{all}V_X - V_{ref}C_{OFF} + (V_X - V_Y)C_{X\_con} \\ &= kV_{ref}C_{X\_sam} - V_{cm}C_{all} \end{aligned} \quad (16)$$

$$\begin{aligned} Q_Y &= C_{all}V_Y - V_{ref}C_{ON} + (V_Y - V_X)C_{X\_con} \\ &= -kV_{ref}C_{X\_sam} + V_{cm}C_{all} \end{aligned} \quad (17)$$

where C_{OFF} is the capacitance for which the corresponding code is "0" and $C_{ON} + C_{OFF} = C_{all}$.

Therefore,

$$V_X = V_{cm} - \frac{C_{ON} - kC_{X\_sam}}{2C_{X\_con} + C_{all}}V_{ref} \quad (18)$$

$$V_Y = V_{cm} + \frac{C_{ON} - kC_{X\_sam}}{2C_{X\_con} + C_{all}}V_{ref}. \quad (19)$$

From Eqs. (18) and (19), the DC level of both outputs of the capacitor DAC is always the same, it is equal to the

common voltage V_{cm} and hence is not affected by variation of the sensor capacitance.

D. Methods for Lower Power Consumption

This section describes methods to lower power consumption of the circuit by utilizing an asynchronous mechanism and a dynamic regenerative comparator.

In the conventional SAR architecture, conversion of every bit is carried out synchronously with the internal clock. Thus, the frequency of the internal clock is much higher than the frequency of the sampling clock expressed as below:

$$f_{\text{internal\_clk}} = (N + \alpha)\ f_{\text{sampling\_clk}} \tag{20}$$

where $f_{\text{internal\_clk}}$ is the internal clock frequency, $f_{\text{sampling\_clk}}$ is the sampling clock frequency, N is the resolution of the CDC, and α is the number of clock that used in the sampling phase.

As known, the power consumption of digital circuit is

$$P = V_{\text{dd}}^2 f C_{\text{L}} \tag{21}$$

where V_{dd} is supply voltage, f is the frequency, and C_{L} is the load capacitance.

According to this, the overall power consumption of the circuit will be large due to the internal clock circuit. To resolve this problem, the proposed circuit applies asynchronous mechanism to eliminate the high speed internal clock circuit as shown in Fig. 3. In the asynchronous mechanism, only a low speed sampling clock is needed. Therefore, the overall power consumption is reduced effectively in the circuit.

The difference between the asynchronous and synchronous mechanisms is that in the asynchronous mechanism there is no need for the internal clock. In the asynchronous mechanism, the starting pulse for every bit conversion is generated automatically. This is due to a negative edge pulse generator, a XOR gate, and a delay line which were arranged like in Fig. 3.

Principle of behavior of the proposed circuit is based on time chart as shown in Fig. 4. First, when the sampling phase finishes, the negative edge pulse generator generates the starting pulse to start up the SAR control logic, keep the MSB at '1' and set other bits at '0'. In this period, the comparator is in reset mode. Next, after a controllable time interval, the start pulse passes through the delay line to the comparator and drives the dynamic latch. This time interval is set to give the output of the capacitor DAC sufficient time to settle into a stable condition. Then, the dynamic latch changes into active mode and compares two outputs of the capacitor DAC. The XOR gate monitors the finishing instant of the comparison, generates a pulse for the next bit conversion. This pulse again passes the delay line and the dynamic latch returns to reset mode after finishing comparison of the MSB. At the same time, the SAR control logic determines the digital code of the MSB based on the comparator output. And then, when the pulse generated from the XOR gate passes through the delay line, the same process is repeated to convert the next bit and continues automatically to other bits.

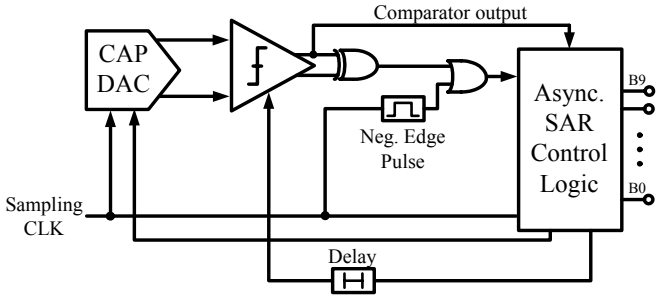

Fig. 3. Asynchronous mechanism of SAR converter

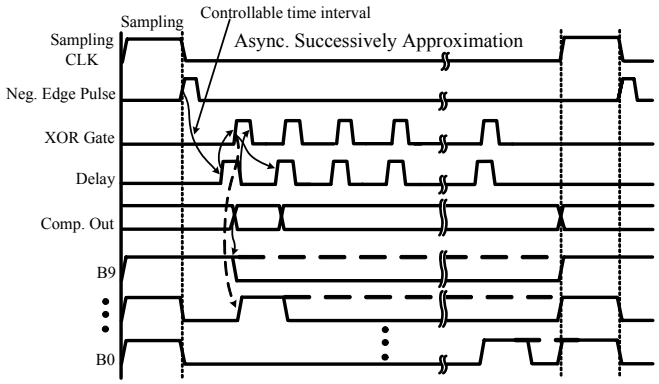

Fig. 4. Time chart of asynchronous mechanism

When the conversion of all bits have finished, the SAR control logic creates a signal which prevent the pulse from passing the delay line to stop the conversion. The circuit is turned into standby status until the next conversion.

Aside from the high speed internal clock circuit, the comparator in a typical SAR converter is also a large power consumption component that often occupies over 50 % of the overall energy dissipation. That is because in a single-ended architecture, to reduce the influence of kick-back noise and fluctuation of the common voltage of the comparator, the pre-amplifier is often connected in series with the comparator and hence draws a static current during conversion. However, in the proposed circuit, these influences are reduced due to the differential architecture and hence there is no need for a pre-amplifier in the first stage of comparator. A two stage dynamic regenerative comparator is utilized, because this type of comparator does not draw any static current, so its power consumption is very low.

III. SIMULATION RESULTS

Simulation was carried out in SPECTRE based on a single-ended architecture and a differential architecture with 10-bit capacitor array; asynchronous mechanism designed using a CMOS 0.18μm process. The smallest unit capacitor C was chosen to minimize area while still satisfying kT/C noise and matching the total capacitance of capacitor array to the moving range of sensor capacitance in the case of the

TABLE 1
Performance of This Work

	Reported in [1]	Reported in [8]	Reported in [9]	This work
Supply Voltage	1.4 V	5 V	2.5 V	1.4 V
Resolution (ENOB)	8 Bit (6.83)	6 Bit (N/A)	10 Bit (7.32)	10 Bit
Total Current Consumption (with clock circuit)	360 μA			29.7 μA
Current Consumption of Core	169 μA	N/A	3 μA	8.45 μA
Conversion Frequency	262 kSps	12.5 kSps	0.8 kSps	262 kSps
Area	0.026 mm^2 (C_m = 3.6pF)	N/A	N/A	0.11 mm^2 (estimated) (C_m = 10pF x 2)

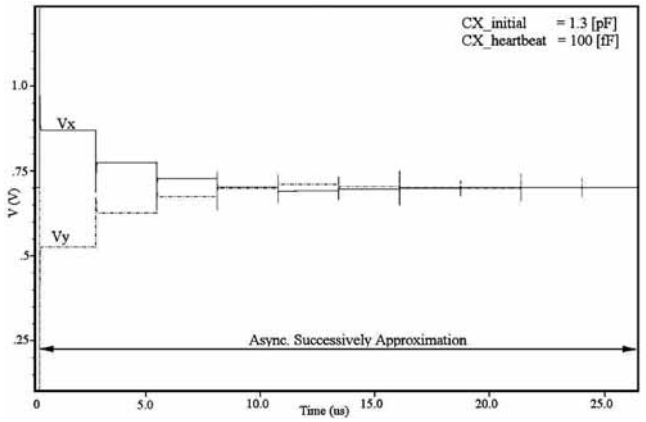

Fig. 5. Behavior of voltage at output of capacitor DAC in a conversion cycle

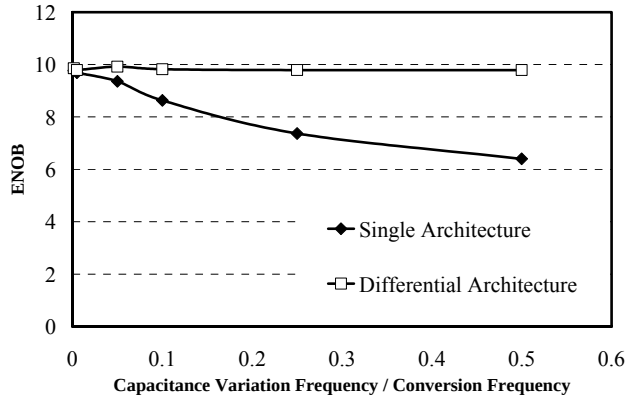

Fig. 6. ENOB vs. (Capacitance variation frequency / Conversion frequency)

scaling factor k is 1. To evaluate the ENOB of the converter, a continuously variable capacitance based on sine wave, written in Verilog-A, was applied at the input. Simulation of power consumption is carried out on transistor level.

Fig. 5 shows the simulation result of the voltage at output of the capacitor DAC, V_X and V_Y. In this case, $C_{X\_initial}$ and $C_{X\_heartbeat}$ were set at 1.3 pF and 100 fF, respectively, and the conversion frequency was set at 37 kHz. Simulation result shows that these two voltages are symmetry around the common voltage V_{cm} = 700 mV, become a differential input pair to the comparator.

From Fig. 6, the proposed differential CDC can convert capacitance to a digital word to Nyquist frequency without deteriorating the ENOB. However, in the single-ended architecture, when the ratio of capacitance variation frequency to conversion frequency becomes larger, the ENOB is deteriorated dramatically. At Nyquist frequency, ENOB in the single-ended architecture is lowered by 3.3 bits.

Table 1 shows the performance of this work which compares to other techniques that using SAR architecture to read-out sensor capacitance. Power consumption of the proposed circuit at 262 kHz is 8.45 μA and 29.7 μA, with clock circuit and without clock circuit, respectively. This is reduced by 92 % and 95 % as compared with the previous work [1] at the same sampling frequency. In the SAR architecture area is dominated by capacitors, so the area of the proposed circuit is estimated based on capacitor number. In the proposed circuit, the ranging capacitor C_m is bigger than in the previous work [1] to be able to cancel entirely the parasitic capacitance of capacitive sensor.

IV. CONCLUSION

We have proposed a 10-bit low-power asynchronous differential capacitance-to-digital converter (CDC) for capacitive sensor applications. The proposed circuit can be used to directly convert capacitance to a digital word exactly, even if the capacitance varies with high frequency. The ENOB of the proposed circuit is kept fixed at Nyquist frequency, while it is lowered 3.3 bits if using the single-ended architecture in the previous work [1]. Thus, the conversion frequency of the circuit can be lower as twice as capacitance variation frequency in theory to lower the power consumption. Additionally, comparing to the conventional single-ended CDC, the proposed circuit is much more endure to the hysteretic and the kick-back noise of the comparator.

Also, by utilizing the asynchronous mechanism and a dynamic regenerative comparator, the proposed circuit consumes very low power which is appropriate for biotelemetry applications. Power consumption of the proposed circuit at 262 kHz is 8.45 μA and 29.7 μA, with clock circuit and without clock circuit, respectively.

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REFERENCES

[1] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, and A. Matsuzawa, "A 0.026mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique," *IEEE Asian Solid-State Circuits Conference*, pp. 244-247, Nov. 2007.

[2] A. D. Hennis, and D. W. Kensall, "A double-sided single-chip wireless pressure sensor," *IEEE International Conference on Micro Electro Mechanical Systems*, pp. 252-255, 2002.

[3] O. Akar, T. Akin, and K. Najafi, "A wireless batch sealed absolute capacitive pressure sensor," *Sensors and Actuators A : Physical*, Vol. 95, No. 1, pp. 29-38, Dec. 2001.

[4] J. C. Lotters, W. Olthuis, P. H. Veltink, and P. Bergveld, "A sensitive differential capacitance to voltage converter for sensor applications," *IEEE Transactions on Instrumentation and Measurement*, Vol. 48, No. 1, pp. 89-96, Feb. 1999.

[5] K. Mochizuki, T. Masuda, and K. Watanabe, "An interface circuit for high-accuracy signal processing of differential-capacitance transducers," *IEEE Transactions on Instrumentation and Measurement*, Vol.47, No. 4, pp. 823-827, Aug. 1998.

[6] M. Yamada, and K. Watanabe, "A capacitive pressure sensor interface using oversampling Δ-Σ demodulation techniques," *IEEE Transactions on Instrumentation and Measurement*, Vol.46, No.1, pp. 3-7, Feb. 1997.

[7] J. O'Dowd, A. Callanan, G. Banarie, and E. Company-Bosch, "Capacitive sensor interfacing using sigma-delta techniques," *IEEE Sensors*, pp. 951-954, Oct. – Nov. 2005.

[8] C.P.L. Van Vroonhoven, D. Rocha, M.J. Vellekoop, and C. Nohammer, "A readout circuit for capacitive biosensors with integrated SAR A/D conversion," *IEEE International Symposium on Circuits and Systems*, 4 p, May 2006.

[9] B. Bechen, D. Weiler, T. V. D. Boom, and B.J. Hosticka, "A 10 bit very low-power CMOS SAR-ADC for capacitive micro-mechanical pressure measurement in implants," *Advances in Radio Science*, Vol. 4, pp. 243-246, 2006.

[10] J. Craninckx, and G. V. D. Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS," *IEEE International Solid-State Circuits Conference*, pp. 246-247, Feb. 2007.

[11] M. Miyahara, Y. Asada, D. Paik, and Akira Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," *IEEE Asian Solid-State Circuits Conference*, Nov. 2008.