CMOS Device Modeling for Millimeter-Wave Power Amplifiers

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***Abstract* — Practical characterization of active and passive devices in CMOS technology is presented in this paper for designing millimeter-wave power amplifiers. Detailed modeling strategy for transmission line, T-junction, and transistor is explained with some actually-designed millimeter-wave amplifiers. A 4-stage PA is implemented in 65nm CMOS process. A 20dB power gain and a 9.9dBm 1dB output compression point are achieved at 60GHz.**

***Index Terms* — CMOS, power amplifier, transmission line, millimeter wave, modeling, characterization**

I. Introduction

Recently, wireless communications of 60GHz are paid attention to because the 60GHz band can be used without license and high-speed wireless communications are possible. Moreover, with the scaling down of CMOS process, CMOS front end of 60GHz band is published in recent years for lowering the cost instead of compound semiconductors such as GaAs.

Because it is difficult to match simulation results to measurement results at high frequency it becomes a problem for 60GHz PA design. Therefore, an accurate de-embedding method and modeling method are demanded.

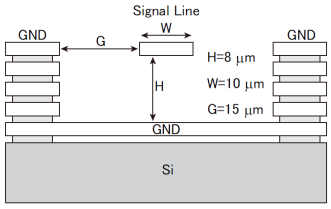

Fig. 1 The structure of TL.

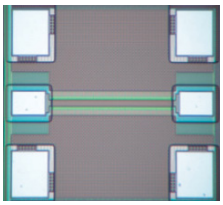

Fig. 2 Micrograph of TL.

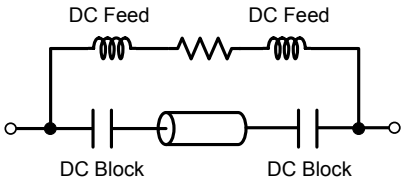

Fig. 3 Model of TL.

II. De-embedding and Modeling Methods

Transmission line model

The Multi-Line De-Embedding (MLDE) method is used in this paper [1]. Guided Micro-Strip Line (GMSL) is used as illustrated in Fig. 1 and the micro photo is shown in Fig. 2. Up to now, to accurately de-embed transmission line at high frequency, two kinds of length are needed for each width of transmission lines [2]. Moreover, this method can only be used to de-embed transmission line.

In [1], parasitic elements of the pad can be extracted from the transmission lines with two kinds of length. Therefore, there is an advantage that the pad can be modeled by using the extracted results. De-embedding can be applied to not only other transmission lines but also components such as transistors by using the model of the pad.

The model of the transmission line is made by employing the following measurement result after de-embedding as shown in Fig.3. The attenuation constant α, phase constant β, quality factor Q and characteristic impedance Z_0 are showed in Fig. 4. As can be seen that the modeling matches with the measurement results. Moreover, because the drain voltage V_{ds} of the transistor influences on the performance of PAs considerably, it is necessary to characterize resistance in power-supply path. Therefore, modeling with high accuracy was realized by separating the AC path and DC path as shown in Fig. 3.

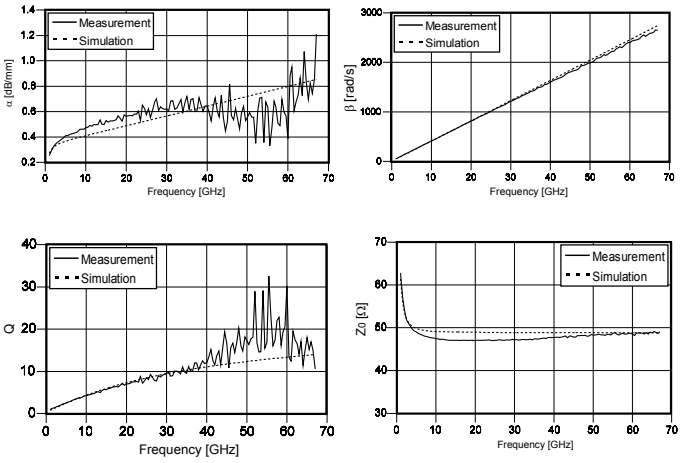

Fig. 4 Guided Micro-Strip: Line width=10μm

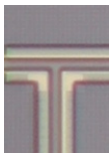

Fig. 5 Micrograph of T-junction.

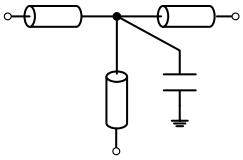

Fig. 6 Model of T-junction.

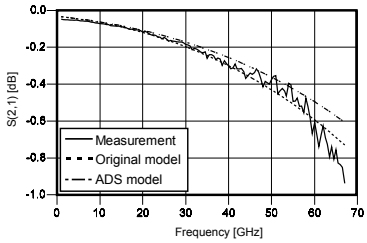

Fig. 7 T-junction S(2,1)

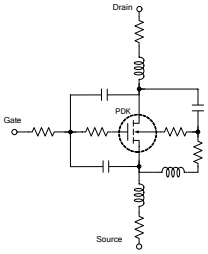

Fig. 8 Model of transistor.

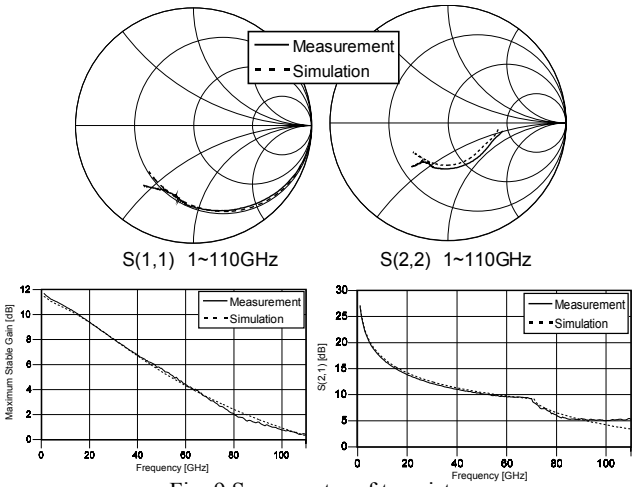

Fig. 9 S-parameter of transistor.

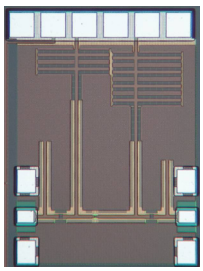

Fig. 10 Micrograph of 1-stage amplifier.

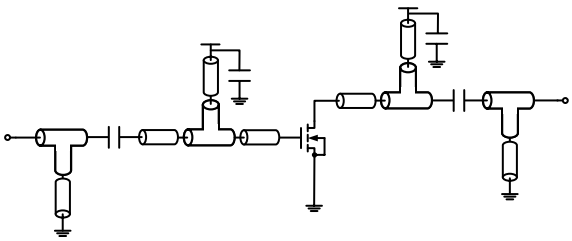

Fig. 11 Circuit of 1-stage amplifier.

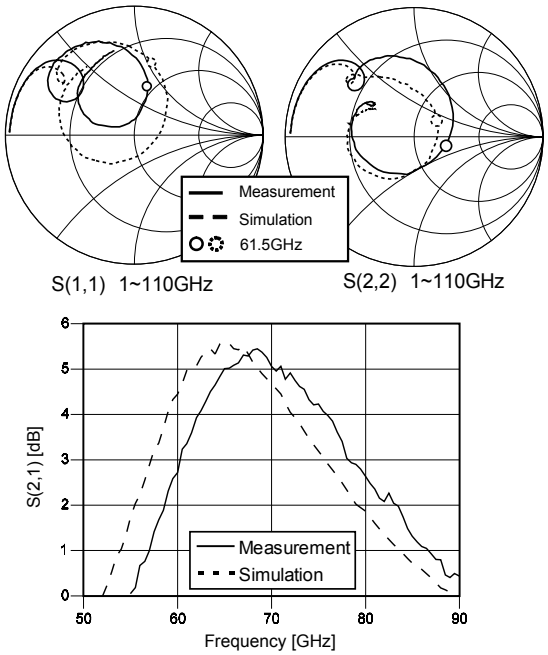

Fig. 12 S-parameter of 1-stage amplifier.

T-junction model

Fig. 5 shows the chip photograph of the T-junction. . GMSL structure is used for T-junction; therefore it can be modeled by using the model of the straight transmission line. And the loss of the T-junction is corrected by connecting a capacitor to the joint point as shown in Fig. 6. Fig. 7 shows the comparison among the simulated results by using the T-junction model, the measurement result of T junction and the simulation results of the T-junction model in ADS.

It can be seen that at high frequency the ADS model does not match with the measurement. So it is necessary to model the T-junction by using the measurement results.

Transistor model

Transistors are de-embedded by using the MLDE method. The parasitic element part was added to PDK and the model was made as shown in Fig. 8. Fig. 9 shows the simulated results based on the model and the measurement results.

1-stage PA

To verify the accuracy of the models, a 1-stage PA is fabricated by using the modeled transistor and transmission line. Fig. 10 shows the chip photograph of the 1-stage PA. The schematic diagram is shown in Fig. 11. The results of the S-parameter are shown in Fig. 12. It is able to confirm that the measurement results and simulation results using the models are matched except that the peak shifts about 2 GHz. The following reasons can be guessed that (1) inaccuracy of DC supply impedance, (2) increase of transistor's source impedance caused by the ground plane, and (3) modeling error related to short stub, e.g., transmission line and de-coupling MIM model [3].

III. Comparison between result of a measurement and simulation result of 4-stage PA

The measurement result of the 4-stage PA is described. Fig. 13 shows the chip photograph of the 4-stage PA. The schematic diagram is shown in Fig. 14.

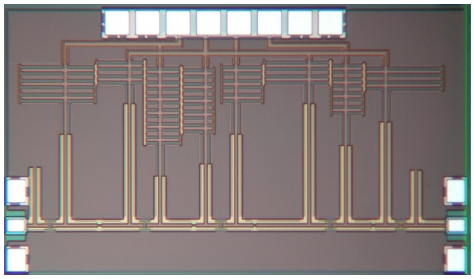

Fig. 13 Micrograph of 4-stage amplifier.

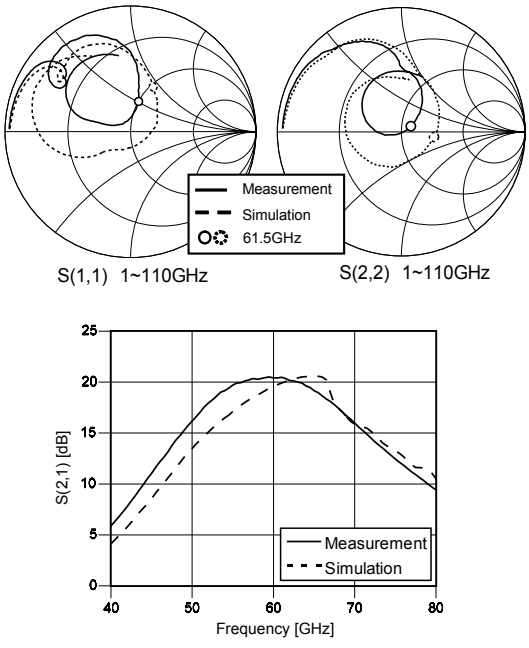

Fig. 15 S-parameter of 4-stage amplifier.

Fig. 15 shows the results of the small-signal characteristics. S_{21} achieves a maximum value of 20dB. The measurement result and the simulation result almost coincide. The accuracy of the model of each component can be confirmed because the simulation results of the 1-stage PA and 4-stage PA are corresponded with the measurement results.

Next, the large-signal characteristic is shown in Fig.16. A 1dB output compression point of 9.9dBm is achieved. The simulation result and the measurement result of the large-signal characteristic have shifted slightly. This can be considered as the influences of the DC characteristic of the transistor.

Fig. 17 shows the measurement result of the temperature performance. S_{21} has been changed by about 4dB or less when the temperature changes from -20 degrees to +80 degrees.

Table 1 shows the comparison with other researches. This work realizes a good power gain and 1dB output compression point.

IV. Conclusion

Practical characterization of active and passive devices in CMOS technology is presented in this paper for designing millimeter-wave power amplifiers. Detailed modeling strategy for transmission line, T-junction, and transistor is explained with some actually-designed millimeter-wave amplifiers. A 4-stage PA is implemented by using a 65nm CMOS process, and the measurement results agree with the simulated results using the proposed models. A 20dB power gain and a 9.9dBm 1dB output compression point are achieved.

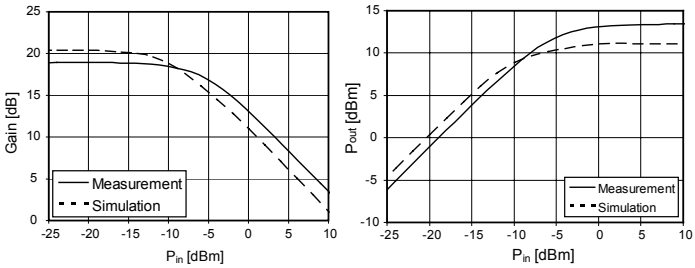

Fig. 16 Large-signal characteristic of 4-stage amplifier.

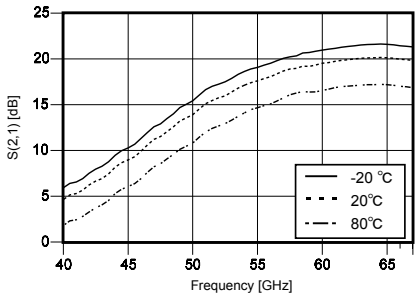

Fig. 17 Temperature property of 4-stage amplifier.

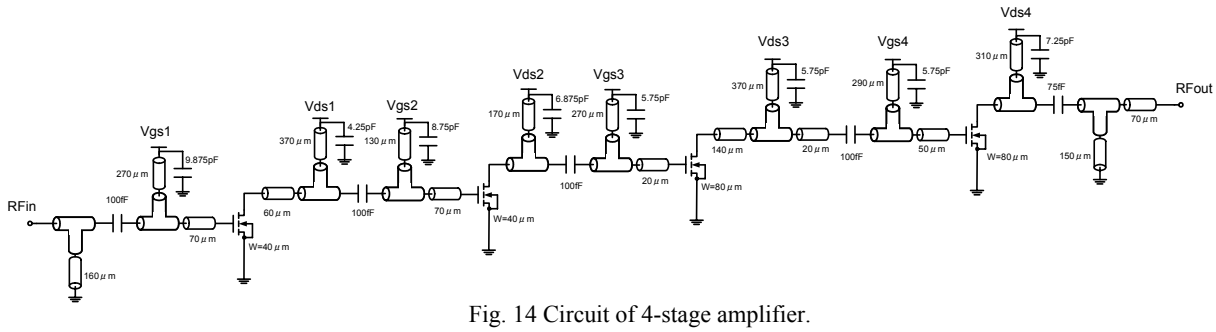

Fig. 14 Circuit of 4-stage amplifier.

TABLE1 Performance summary.

Reference	Technology	Freq. [GHz]	Gain [dB]	P1dB [dBm]	PAE [%]	PDC [mW]	VDD [V]
[3] JSSCC 2007	90nm CMOS	61	5.2	6.4	7.4	21	1.5
[4] RFIC 2008	90nm CMOS	63	14	11	15	81	1.2
[5] ISSCC 2008	90nm CMOS	60	8.2	8.2	2.4	229	1.2
[6] ISSCC 2008	90nm CMOS	60	5.5	9	6	80	1
[7] ISSCC 2008	90nm CMOS	60	13.3	10.5	8	150	1
[8] ISSCC 2009	65nm CMOS	60	15.8	2.5	3.95	43.5	1
[9] ISSCC 2009	45nm CMOS	60	13.8	11	–	–	1.1
[10] MWCL 2009	90nm CMOS	60	30	10.3	6	178	1.8
This work	65nm CMOS	61.5	20	9.9	6.68	144	1.2

ACKNOWLEDGEMENT

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