ダミーフィルを考慮した 60GHz CMOS増幅器設計

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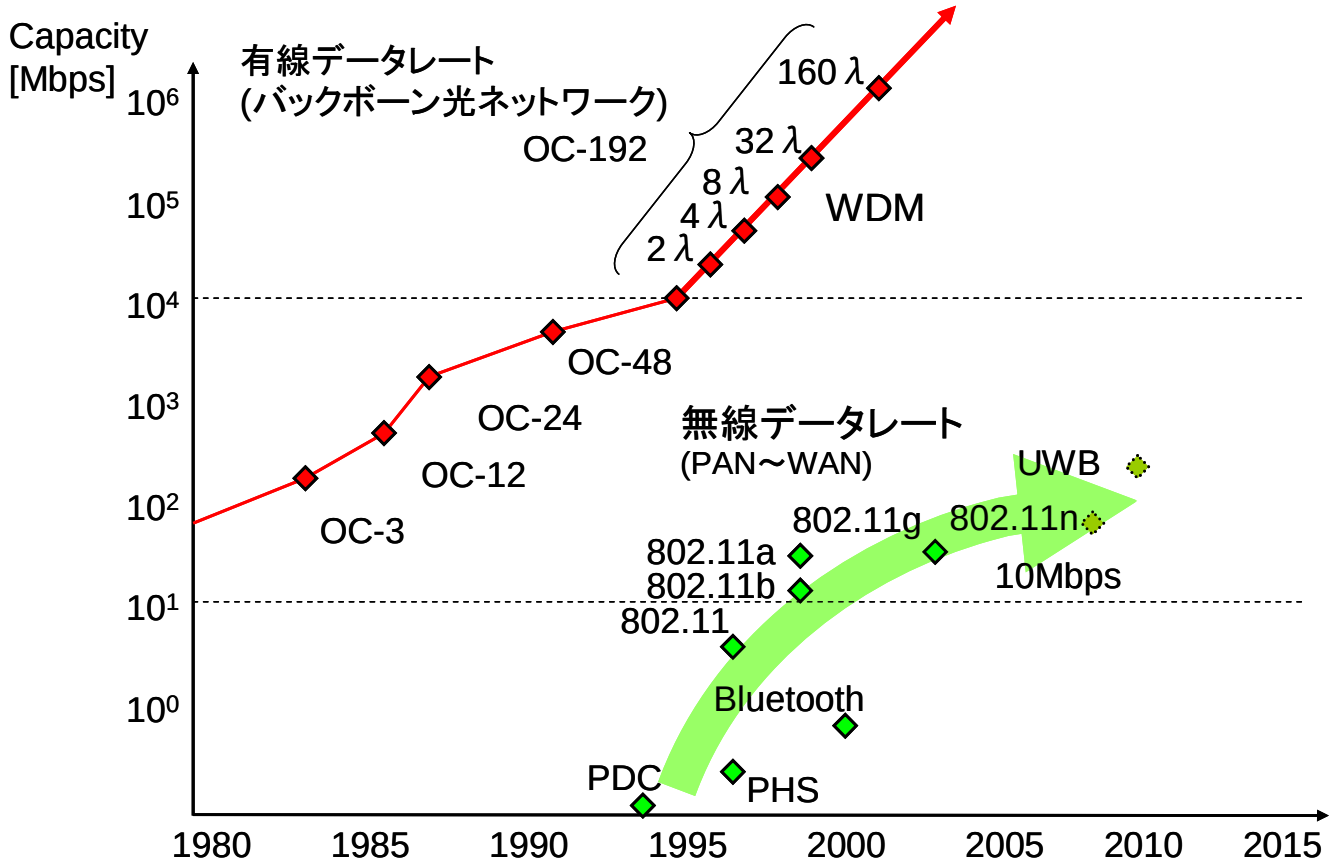
2009/11/10

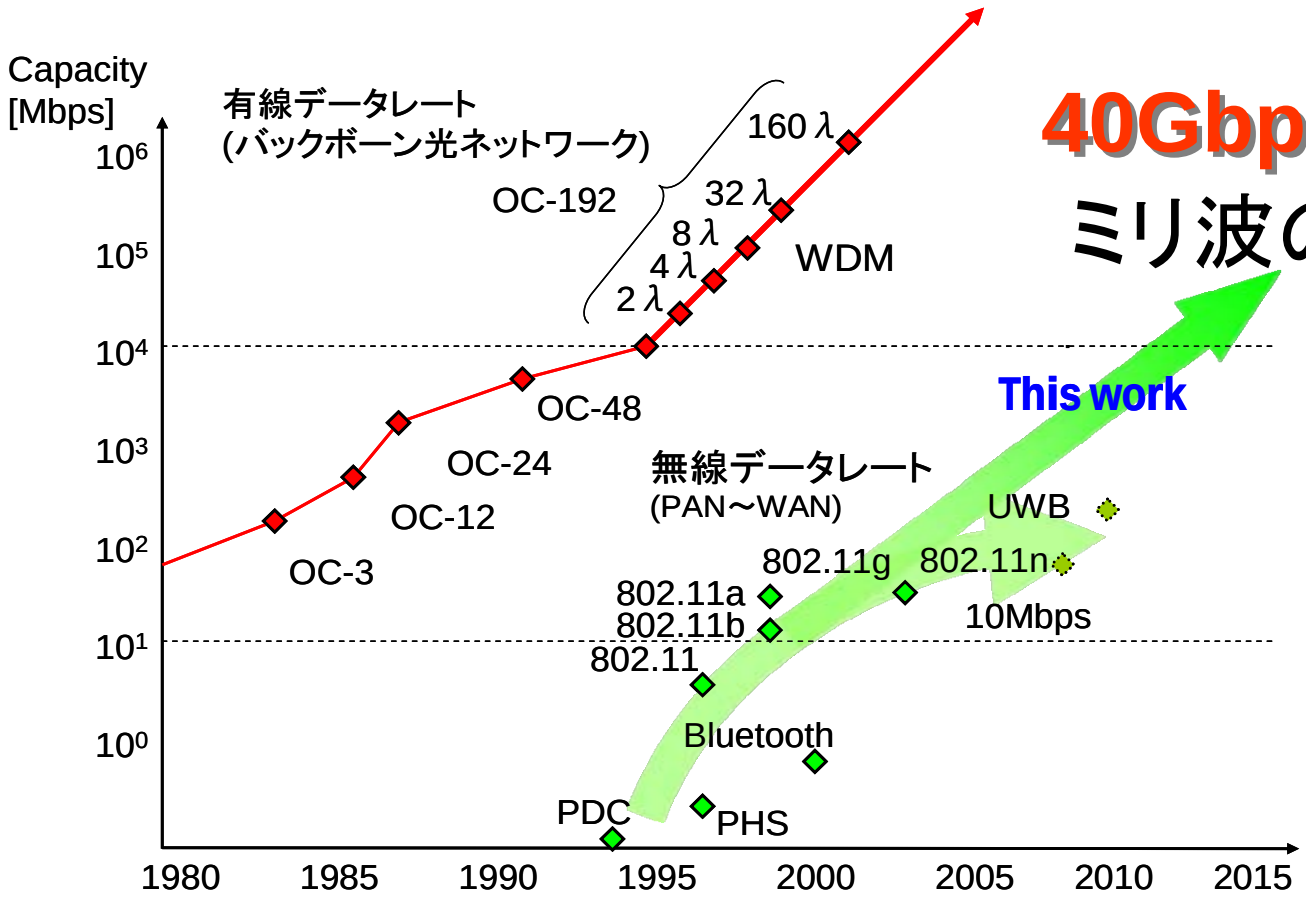
Matsuzawa & Okada Lab.

無線通信の陳腐化



コンテンツの情報量 ∝ LSIの性能
有線の通信速度 ∝ LSIの性能
無線の通信速度 ∝ 周波数帯域

無線スケーリング



コンテンツの情報量 ∝ LSIの性能
有線の通信速度 ∝ LSIの性能
無線の通信速度 ∝ 周波数帯域

ミリ波による
超高速無線通信

目標

60GHz帯で、最大9GHz帯域の利用が可能

あくまでも机上の空論ですが. . .

carrier	57GHz-66GHz
channel-BW	8640MHz(**4ch**)
symbol rate	6912Mbps
変調	**64QAM**

＝ **約40Gbps**

Motivation

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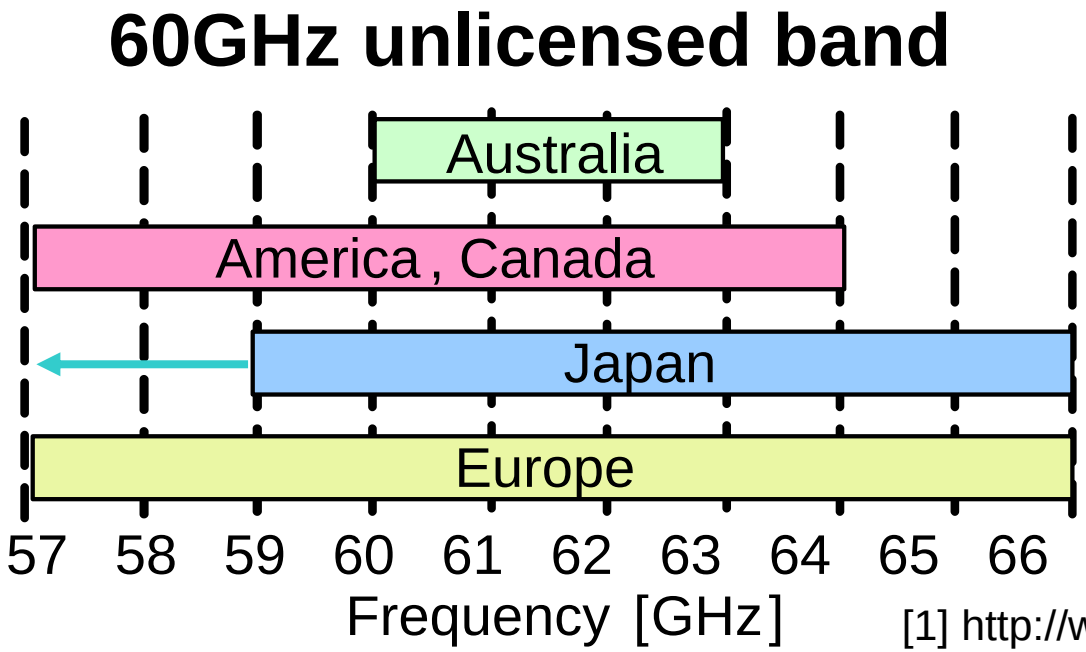

[1] http://www.tele.soumu.go.jp

- 9GHz-BW around 60GHz
  - ⇨ Several-Gbps wireless communication
- Use of CMOS process
  - ⇨ Fab. cost is very important to generalize it.
    RF&BB mixed chip can be realized.

60GHz channel plan

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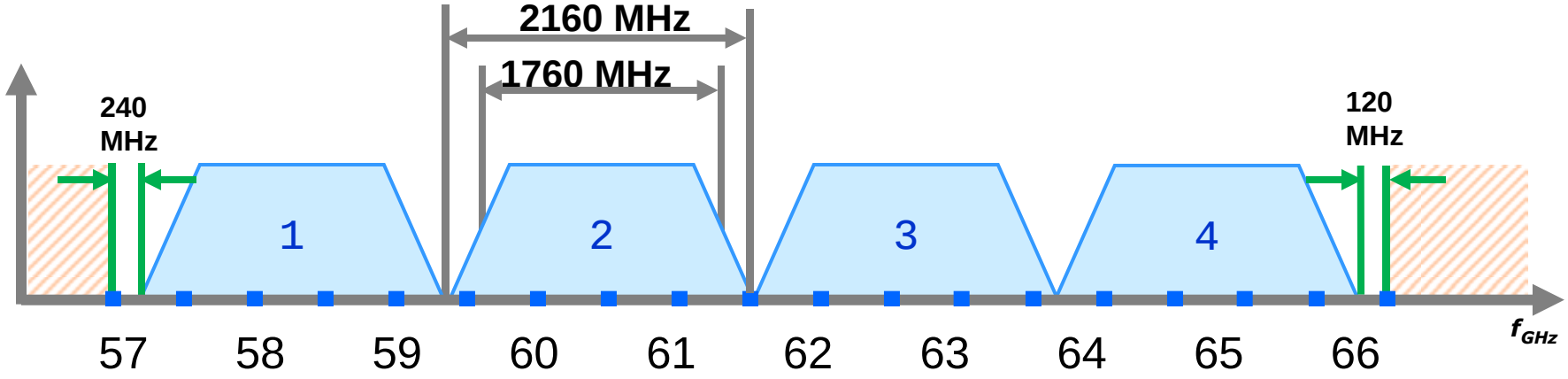
IEEE802.15.3c

Ref: IEEE 802.15-09-192-003c with draft doc.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)	Roll-Off Factor
A1	57.240	58.320	59.400	1760	0.227
A2	59.400	60.480	61.560	1760	0.227
A3	61.560	62.640	63.720	1760	0.227
A4	63.720	64.800	65.880	1760	0.227



4 channel of 2.16GHz-BW

Overview on TG3c System Design

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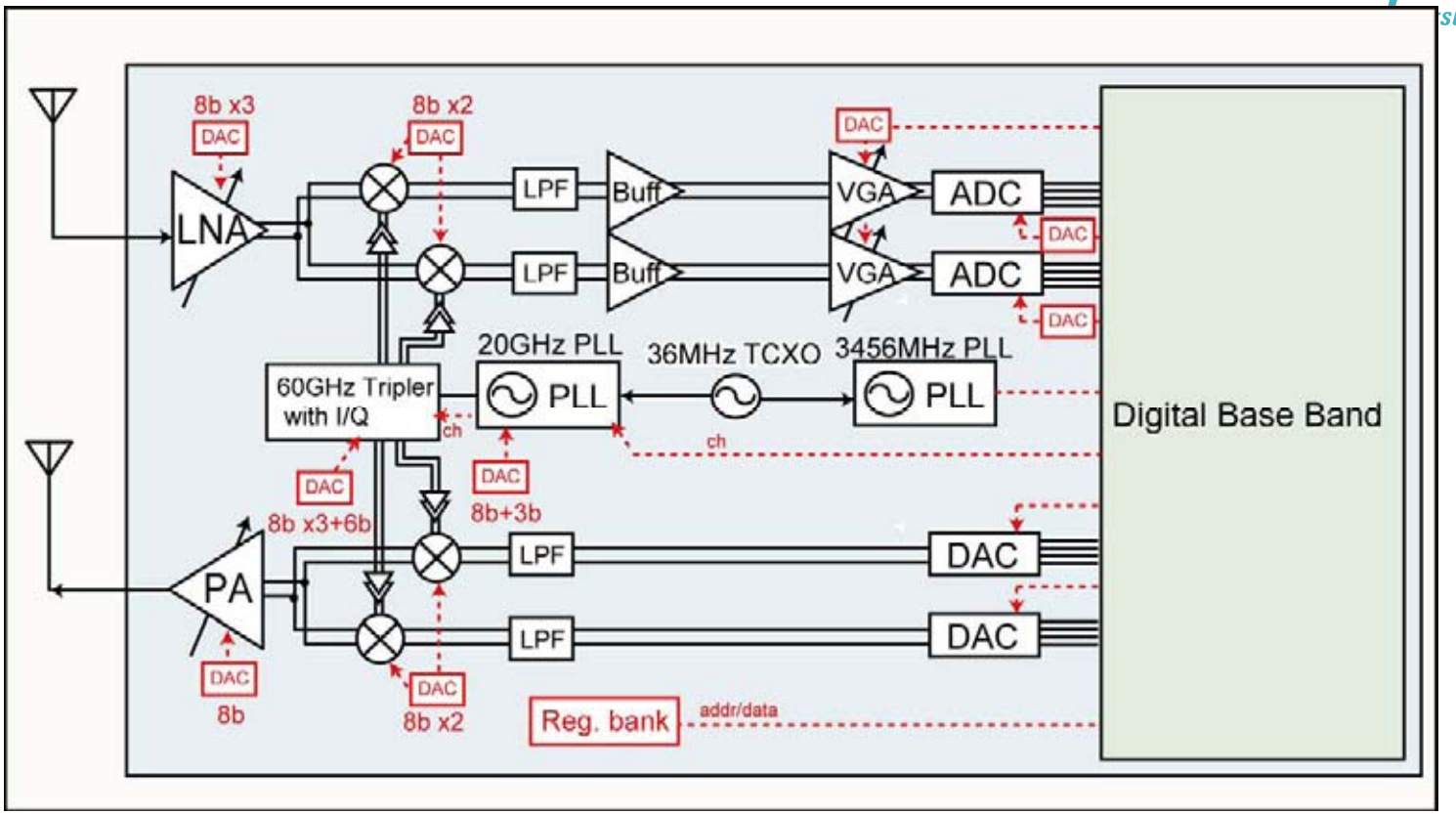
- One unified MAC
- Three PHYs optimized for respective and specific market segments
  - **Single carrier (SC) PHY**
    - low complexity, low power consumption and low cost
    - handheld mobile applications
  - **High speed interface (HSI) PHY - OFDM**
    - low latency bi-directional data communications
    - PC peripherals
  - **AV PHY - OFDM**
    - optimized for high speed uncompressed video transmission
    - Audio/visual consumer electronics (CE) applications

Ref: IEEE 802.15-09-192-003c

Our target



60GHz 2.16GHz-**full 4ch direct-conversion** by **CMOS**

QPSK 3Gbps & **16QAM 6Gbps & 64QAM 9Gbps**

IEEE 802.15.3c conformance

Dynamic power management: <300mW for RF front-end

60GHz CMOS回路設計における課題

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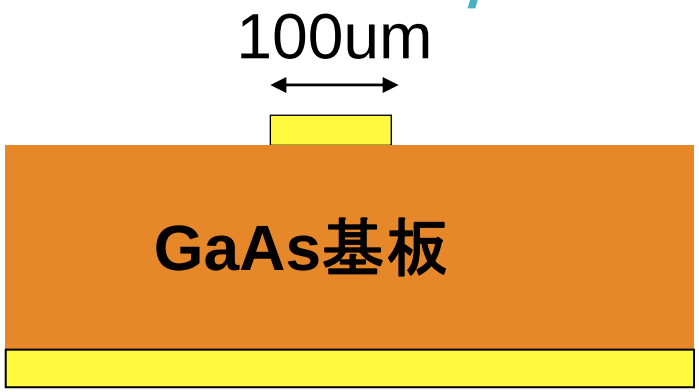
- **そもそも素子性能が低い**
  - トランジスタの利得が低い
  - マッチング用素子の損失が大きい (TL, Inductor等)
- **モデリング・シミュレーション精度が低い**
  - 測定精度
  - レイアウト精度 (微小な寄生容量でも致命的に)
- **素子モデルがない**
  - ファウンダリからのPDKはせいぜい20GHzまで
- **ダミーメタル (密度ルール)**

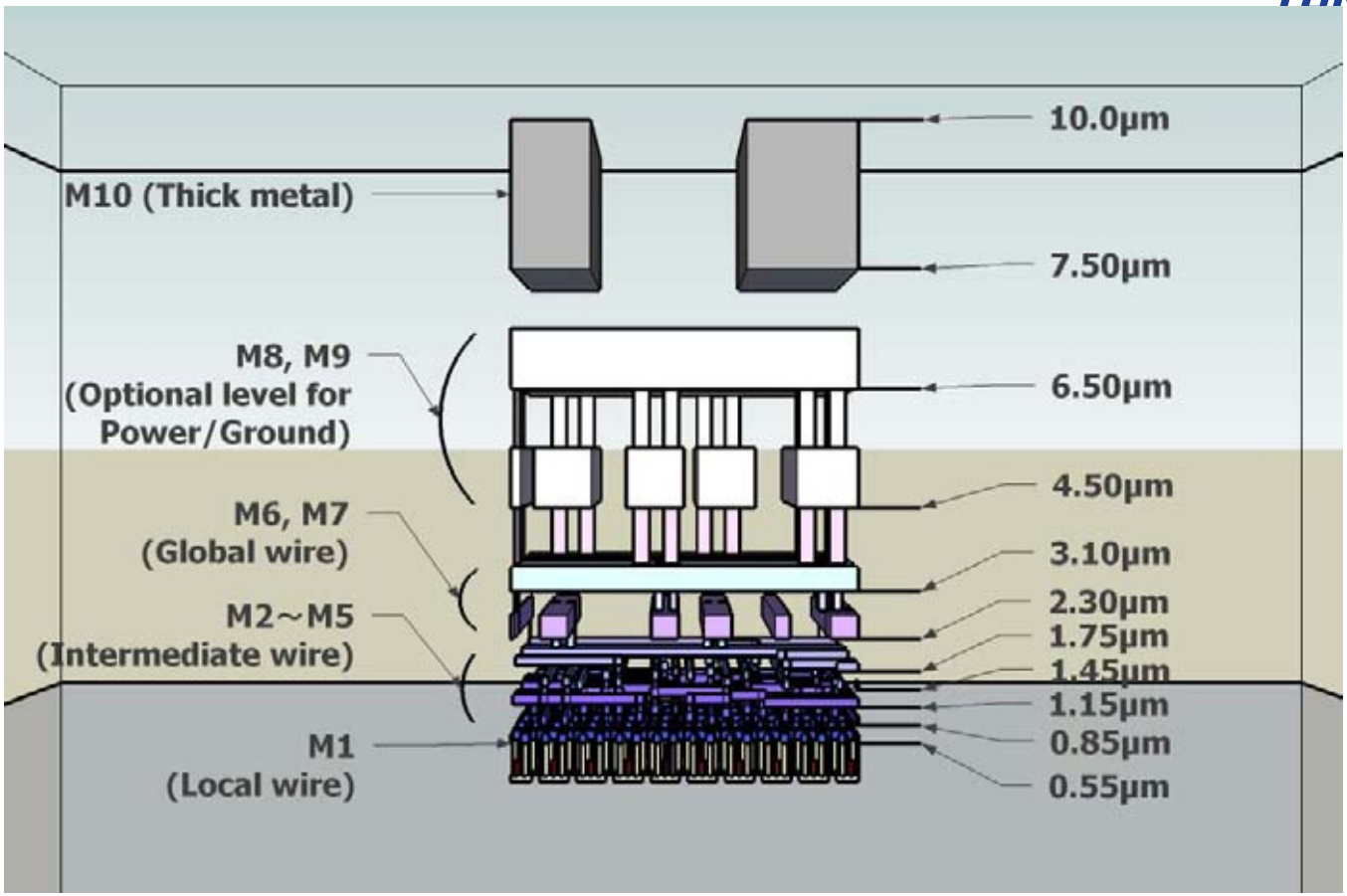
Passive素子のロス



裏面がGNDでない
配線幅 10um
配線厚 1～2um (最大)
誘電体厚～5um
導体損＋基板による渦電流損

⇒**0.5～1dB/mm @60GHz**

CMOS多層配線プロセス(65nm相当)

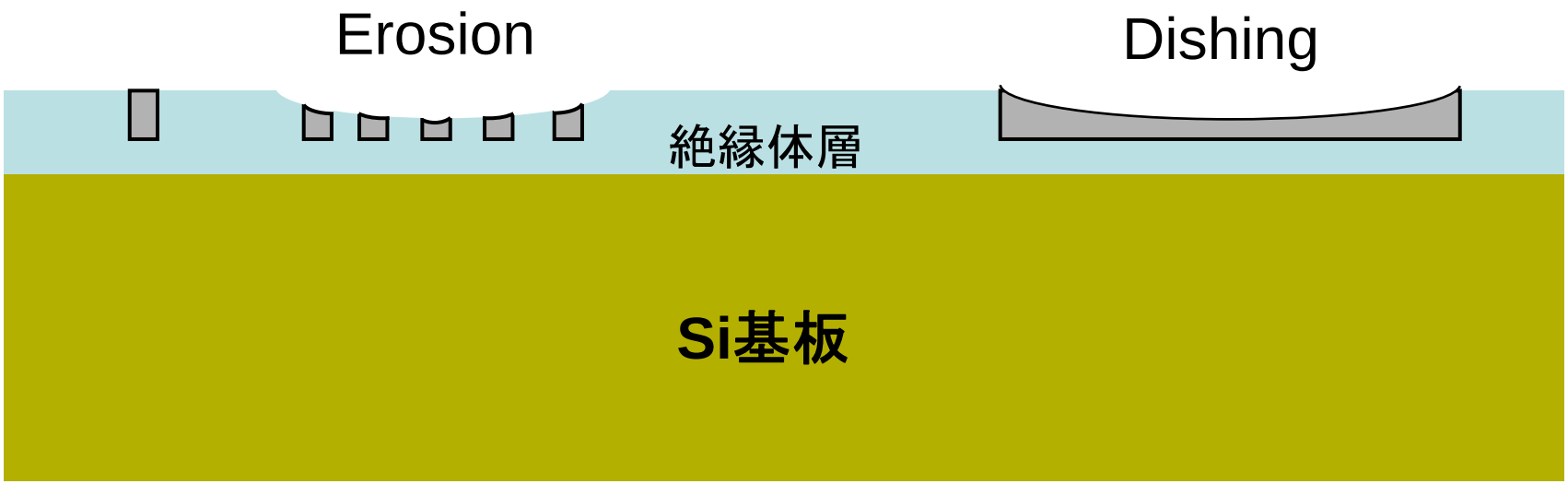


http://www.tamaru.kuee.kyoto-u.ac.jp/~tsuchiya/LSI-3D-CG.html

- 層によって誘電率が異なる
- Cu配線は、バリアメタルにより、外辺部分が高抵抗

CMOS多層配線プロセスにおける密度ルール

一層ごとに配線を削り、平滑化する
CMP (Chemical Mechanical Polishing/Planarization)



CMPによる削れムラを減らすために、
ダミー配線を入れて、配線密度を一定にする必要がある。

Dummy metal in TL

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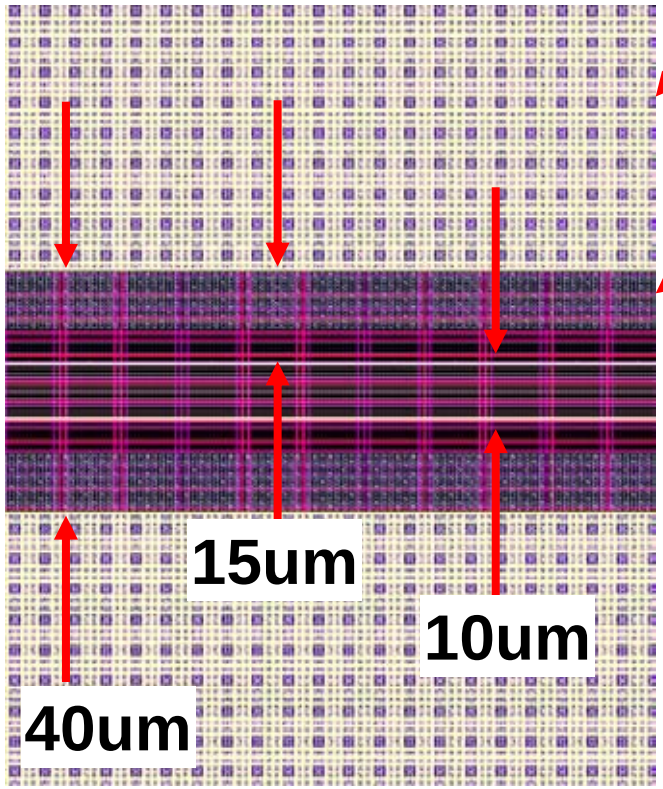
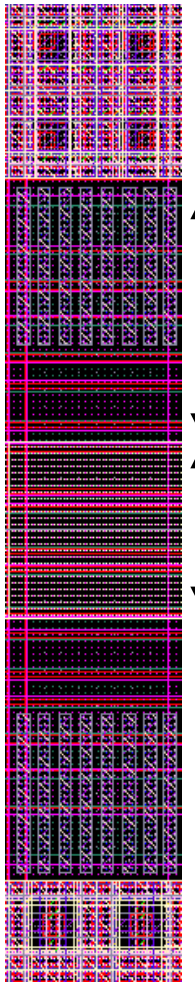
To avoid random production of dummy metal, it is manually placed to keep good reproducibility.



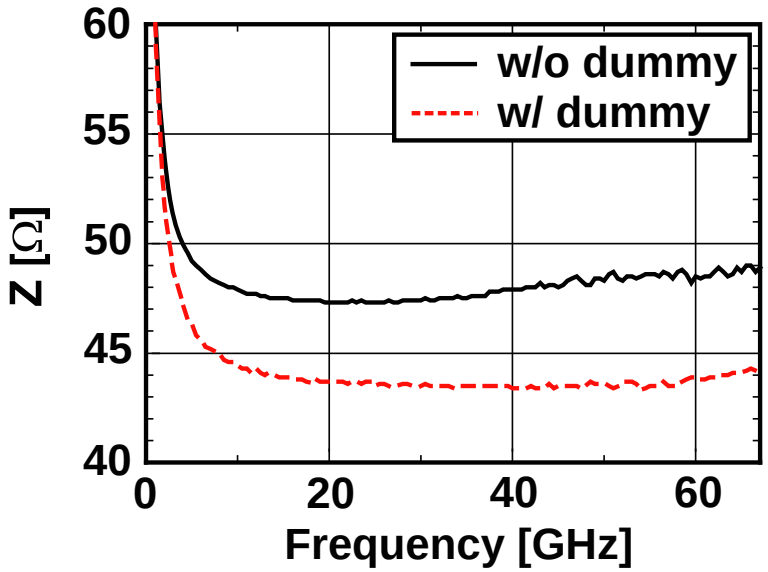
Ground mesh

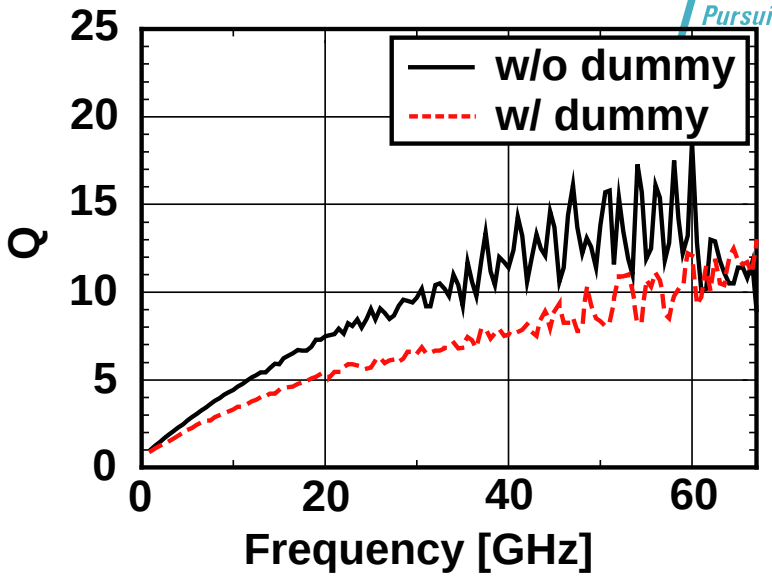
Manually-placed dummy metal

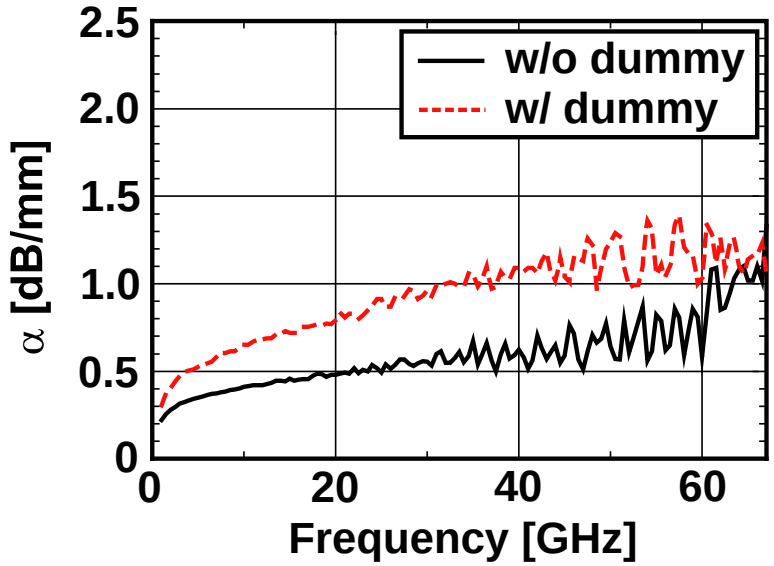
Signal line

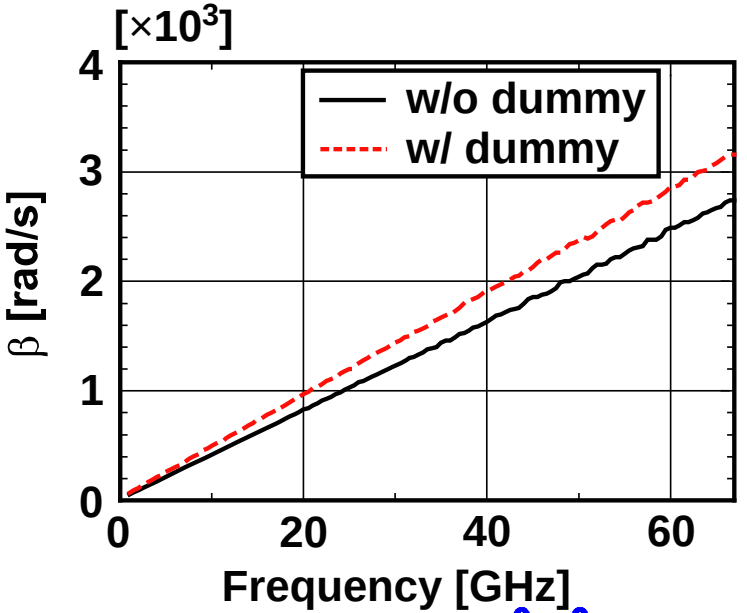


ダミー入り伝送線路の特性1

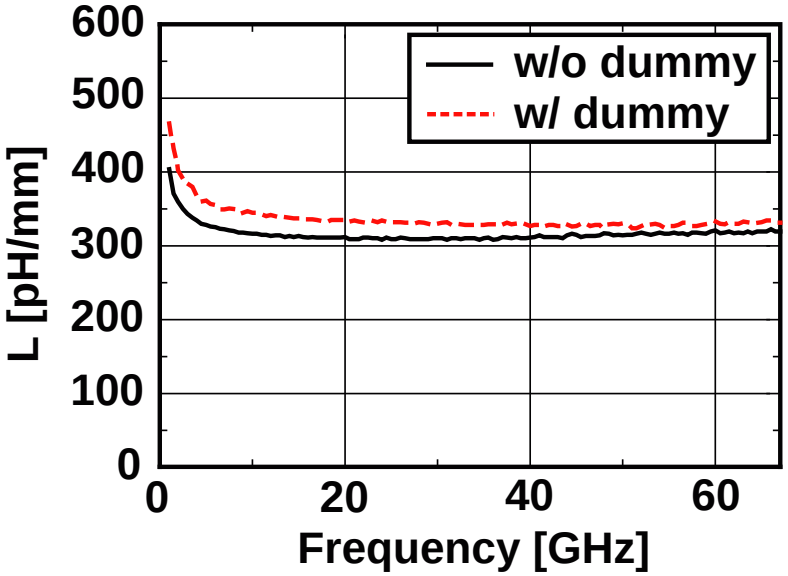


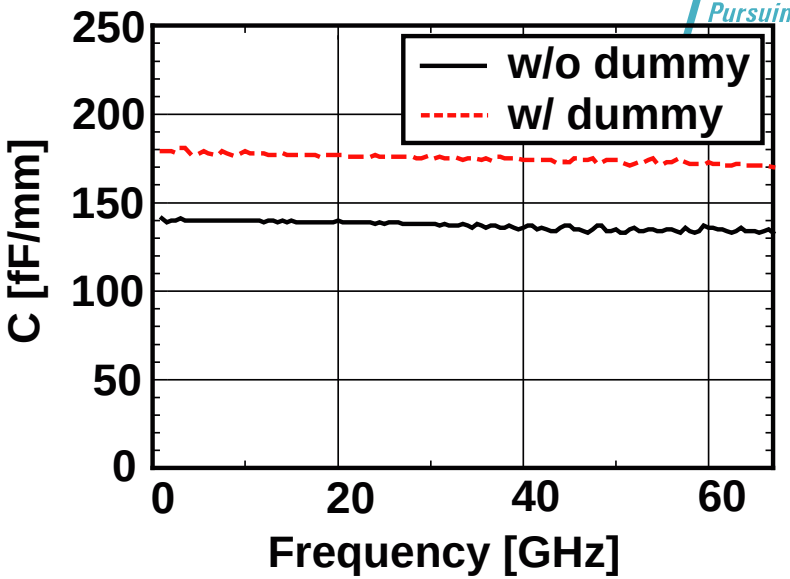


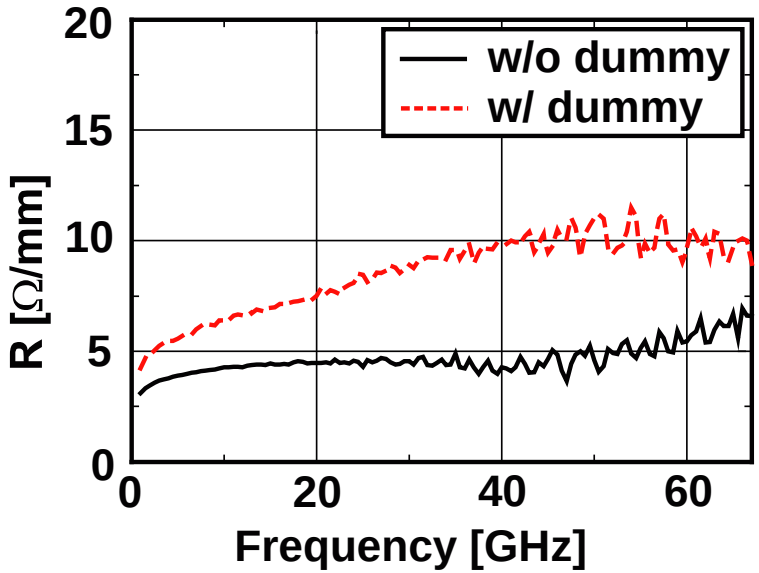


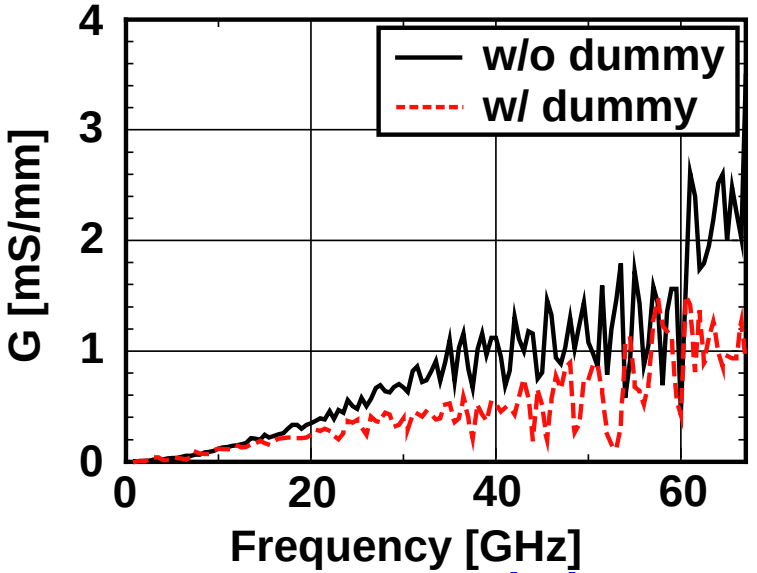


ダミー入り伝送線路の特性2









ダミーメタルの影響

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ダミー手置き ⇒ ダミー自動生成の影響

Z: 10%程度低下

Q: 15⇒10

α : 0.7dB/mm ⇒ 1.2dB/mm

β : 10%程度増加

L: ほぼ変化なし

C: 20%程度増加

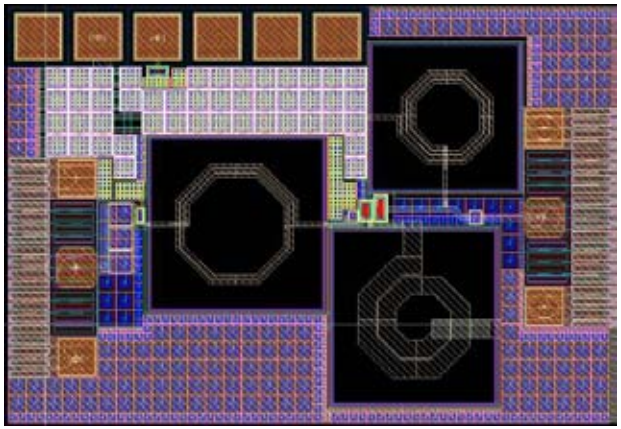
R: 50%増加(測定誤差大)

G: 40%減少(測定誤差大)

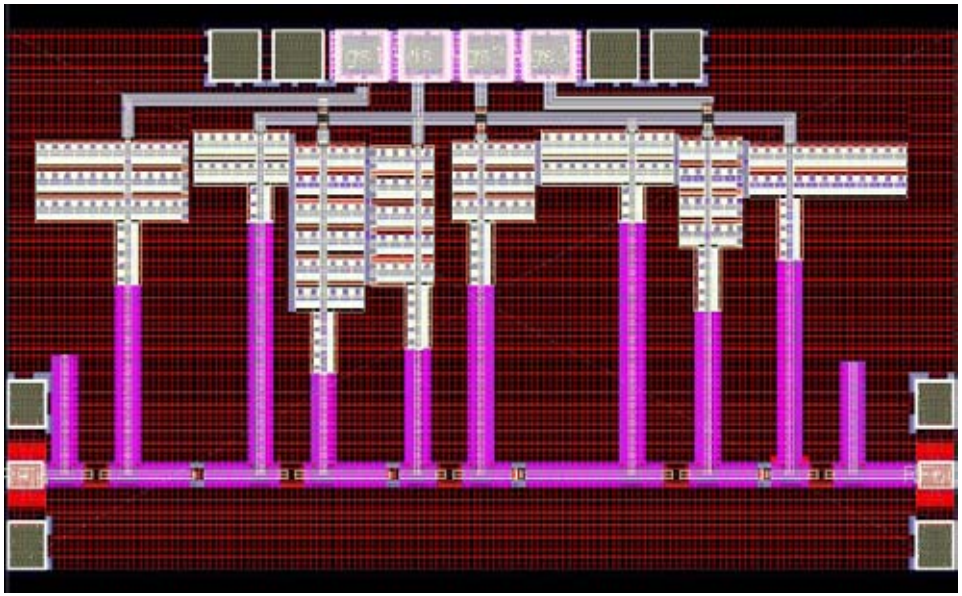
60GHz CMOSロバスト設計へのアプローチ

- **伝送線路によるマッチング**
  寄生素子の排除
- **タイルベースレイアウト**
  厳密にレイアウトとモデルを一致させる
  ダミーメタルの手置き
- **実測に基づくIn-house PDK**
  実測ベースの分岐・曲げモデル
  分布デカップリングモデル
  伝送線路によるマッチング (vs インダクタ)
  固定寸法トランジスタモデル

伝送線路によるマッチング



Inductor@5GHz



Transmission line@60GHz

- 引き出し線、素子間配線の影響 (寄生インダクタンス)
- 寄生容量の影響の排除
- スケーラブル (長さ調整)

Tile-base layout

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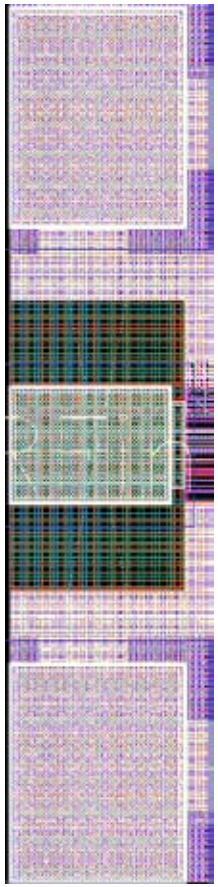
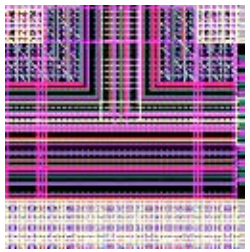
Each component is previously measured and modeled.
The same layout is utilized to maintain modeling accuracy.



RF PAD

5mm pitch

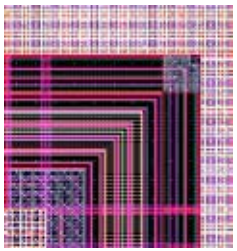


T-Junction

Tr

TL

C



L-Bend

MIM TL

GND-Tile

In-house PDK

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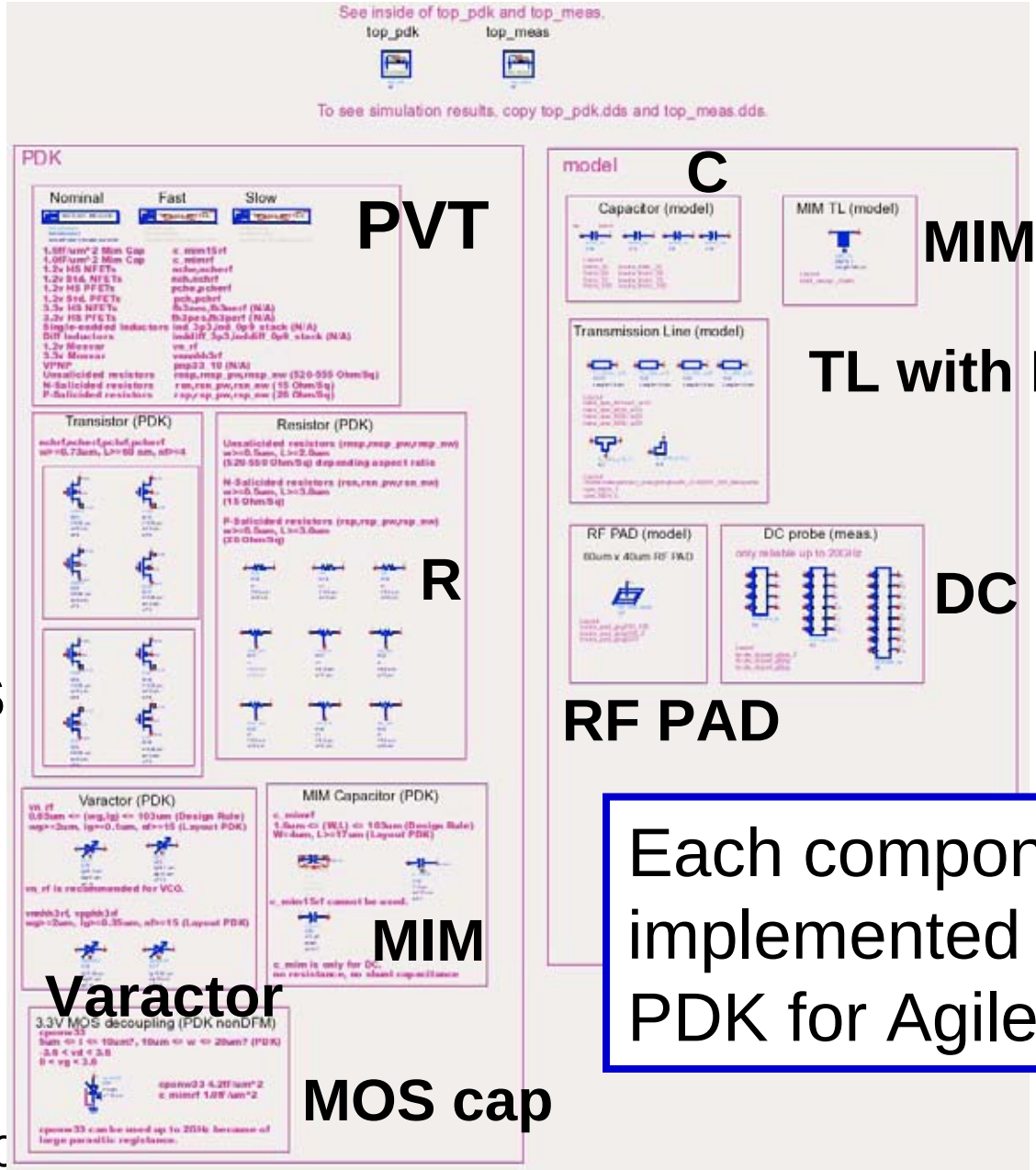
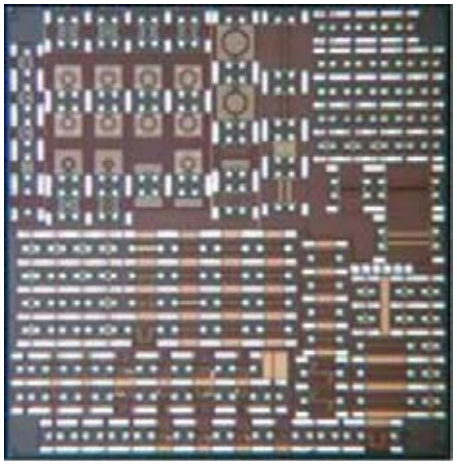
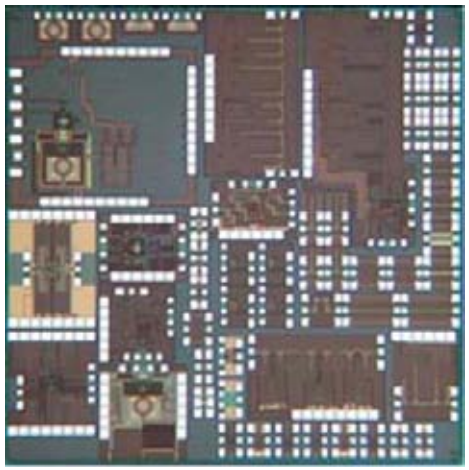


Each component is implemented as an in-house PDK for Agilent ADS.

Overview of device characterization



Initial T.O.



Second T.O.

Initial T.O. for **Modeling**

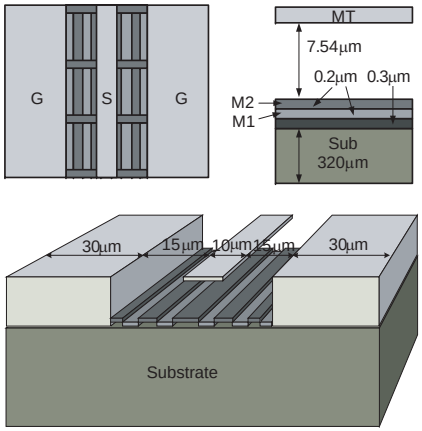
- Transistors (CS, CG with various layouts)
- Transmission line (various length & Z_0)
- Branch & bend line
- Spiral inductor
- Balun
- Series capacitor
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier for the model evaluation
- DC probe

低い素子特性を可能な限り補うため、モデリングは非常に重要

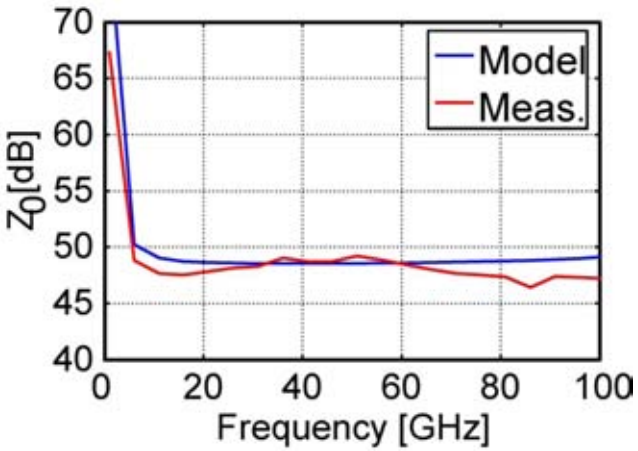
Second T.O.

- Circuit building blocks
- Whole system

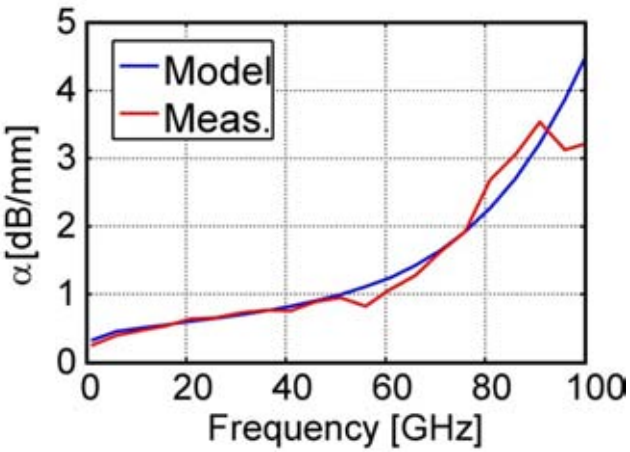
Transmission Line Modeling



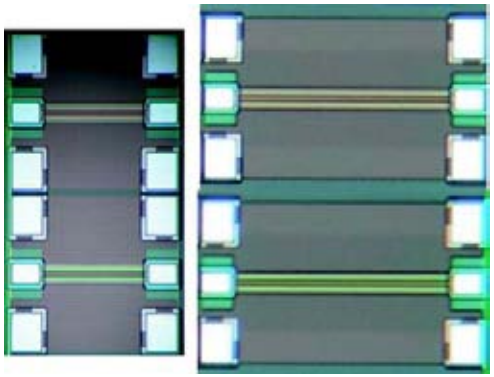
Cross Section



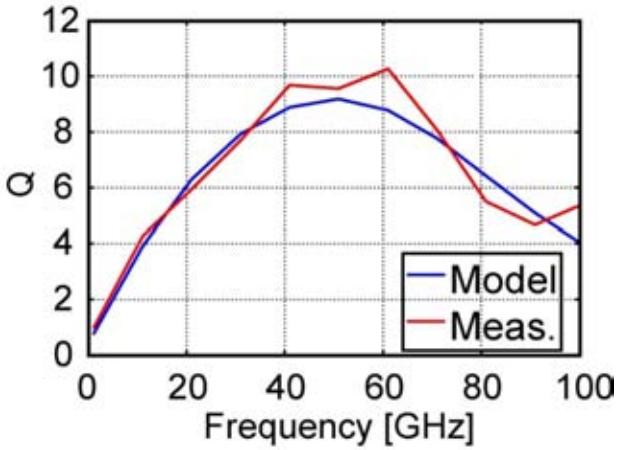
Z_0



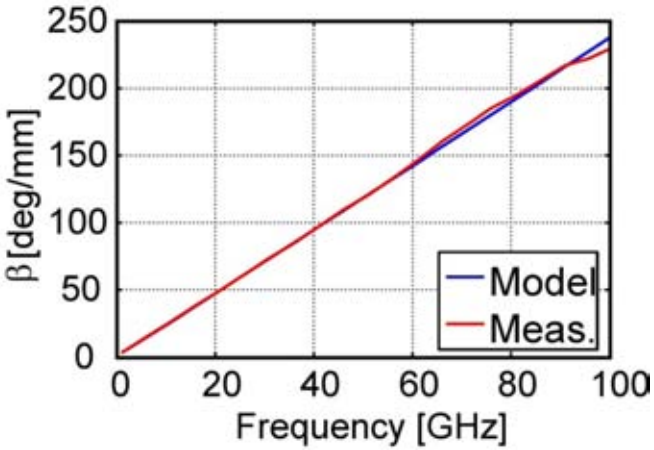
α



Chip photo



Q



β

トランジスタのモデリング

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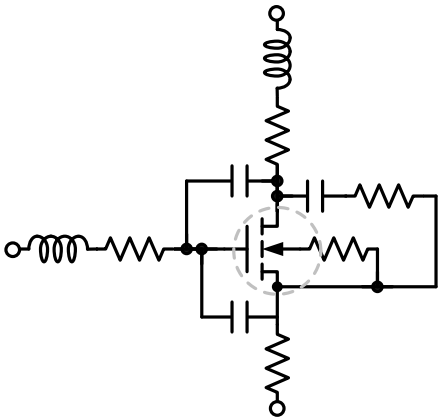
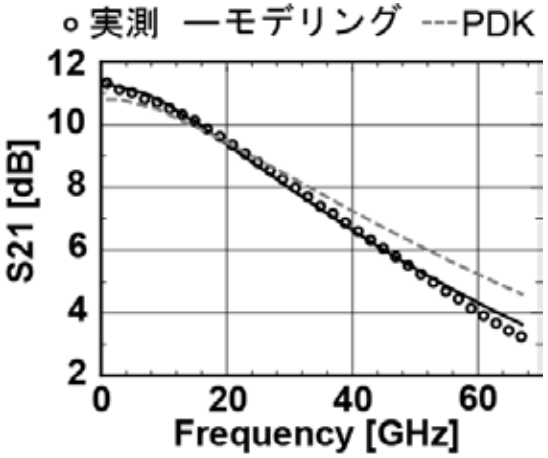
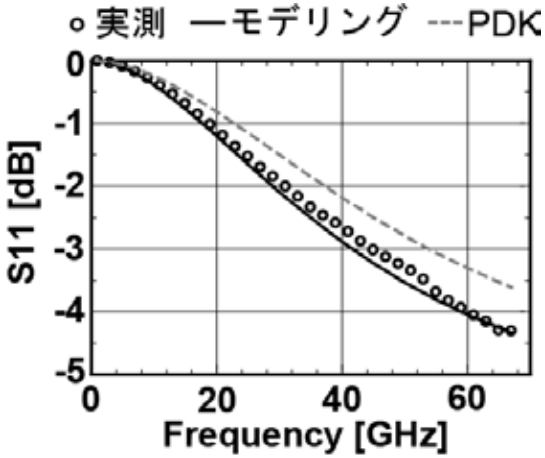
- 寄生成分を付け足し、測定データと合わせる
  - トランジスタの利得
    - 誤差 1 dB ⇒ 0.2 dB
  - 反射特性
    - 誤差 0.8 dB ⇒ 0.1 dB



モデル回路

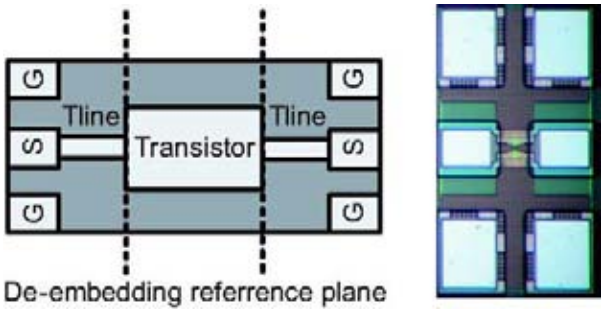


利得特性

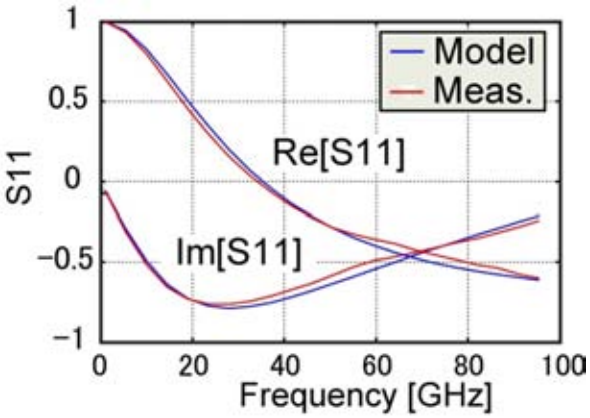


反射特性

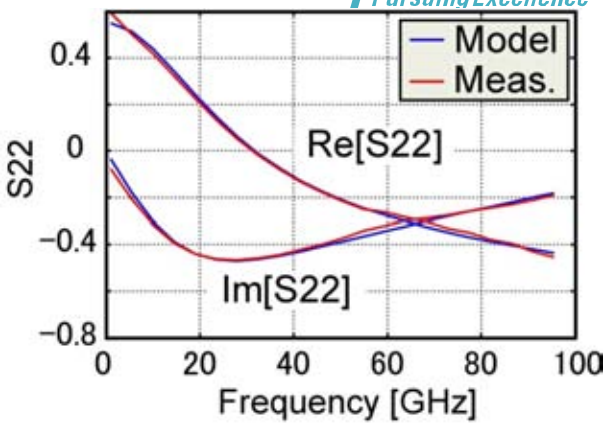
Transistor Modeling



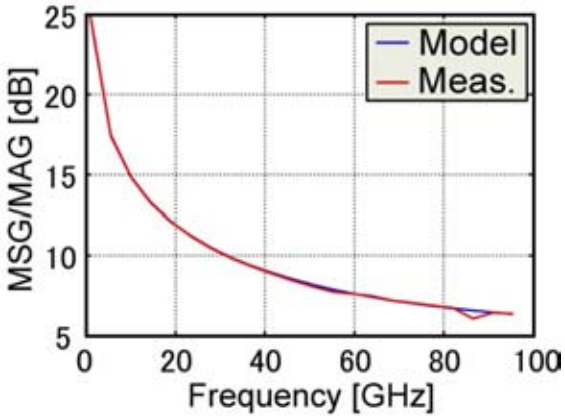
Chip photo



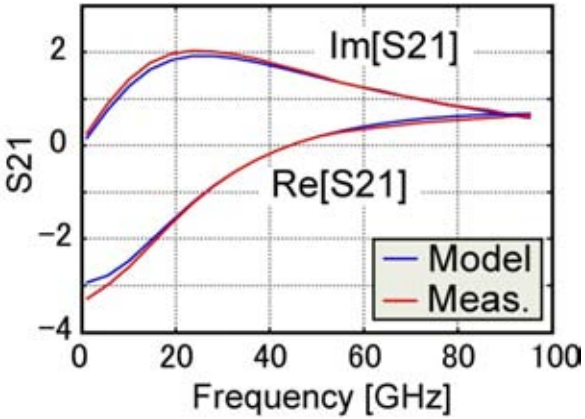
S11



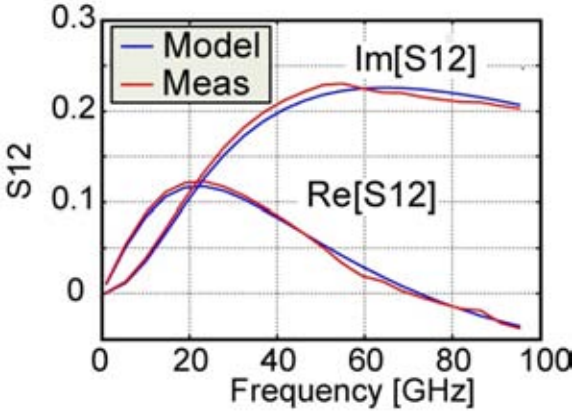
S22



MSG/MAG



S21



S12

60GHz CMOS PA設計

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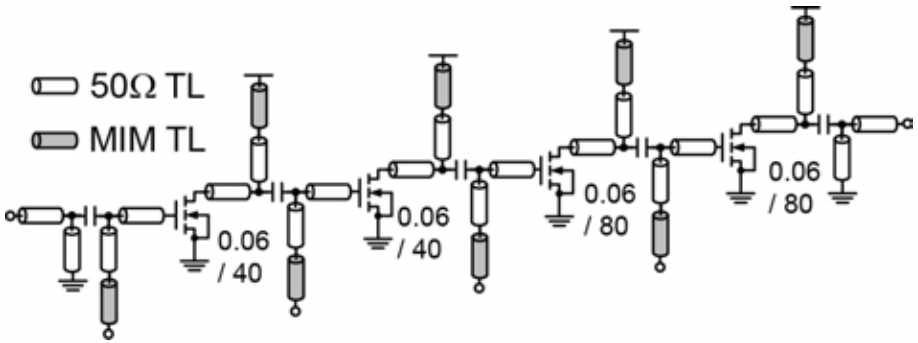
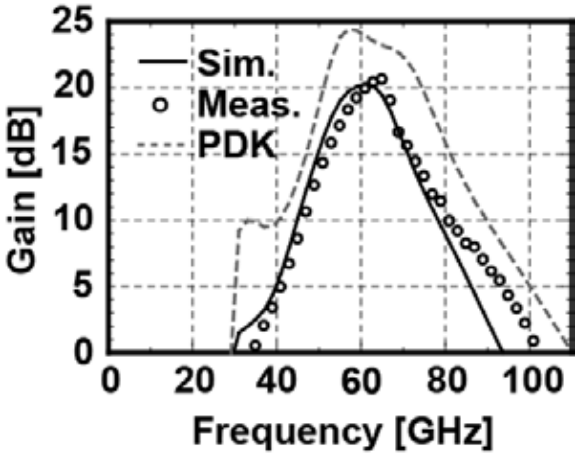
- 回路構成
  - モデリングした各素子を用いて設計
  - 4-stage構成
  - CMOS 65nm
- 測定結果
  - 素子のモデリングにより、シミュレーションの精度が向上
    - Sim.-Meas.誤差　5dB　⇒　0.5dB以下



パワーアンプ回路図



回路利得の測定結果

Chip micrograph

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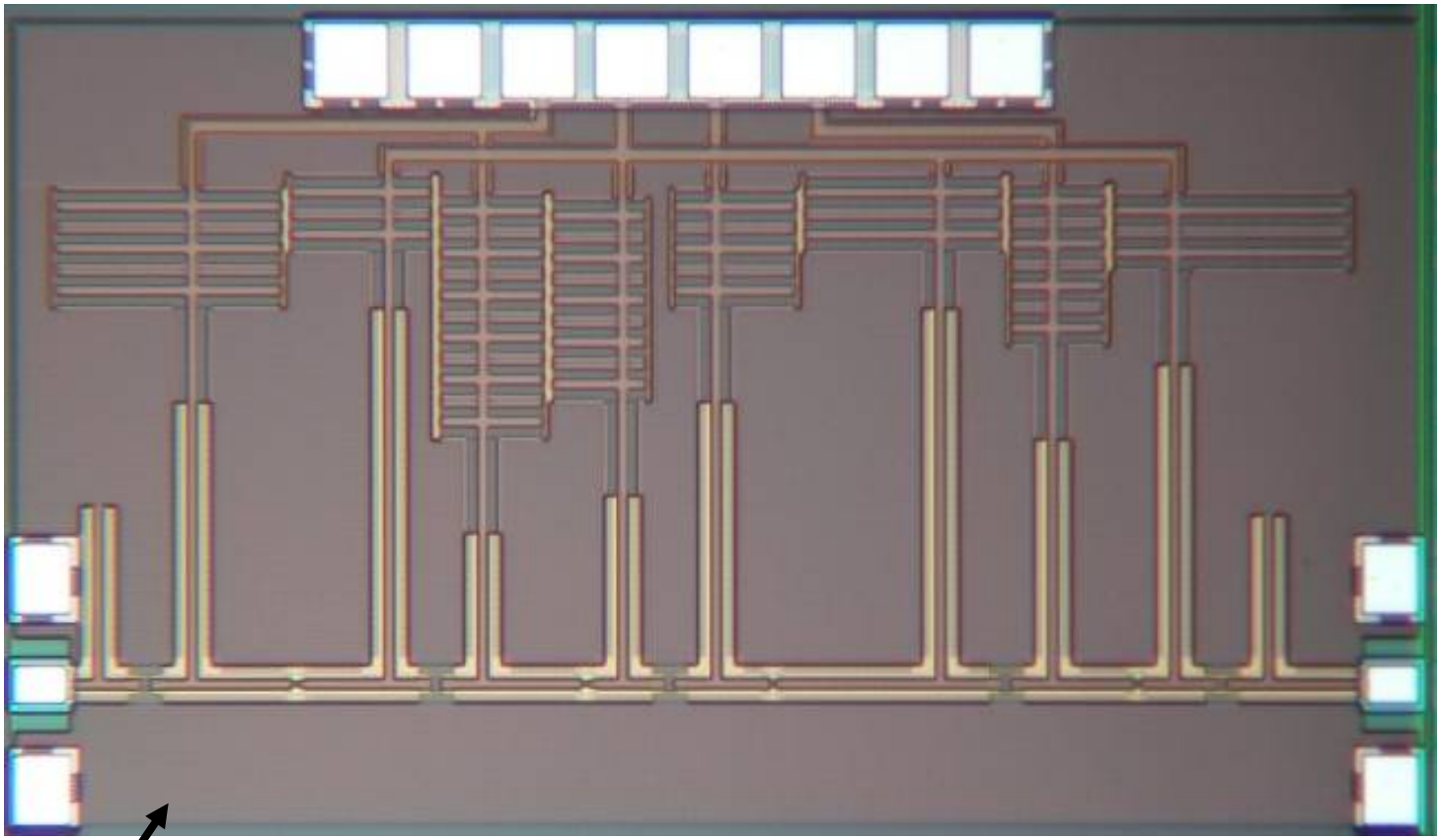
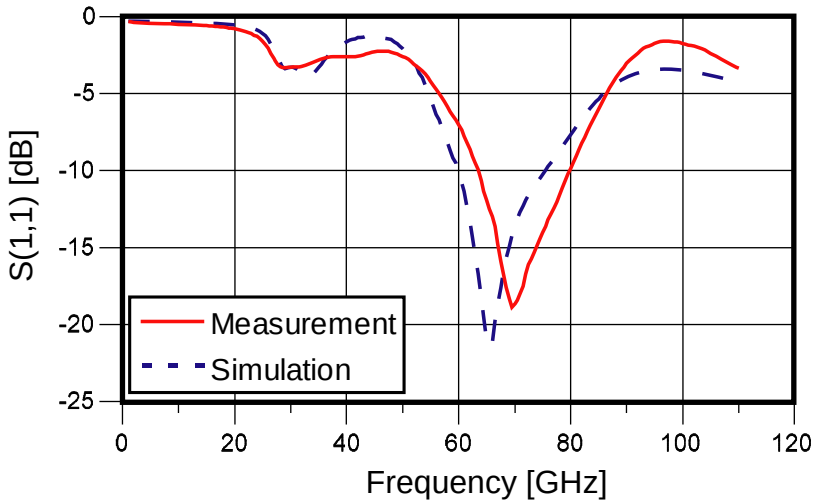
60GHz CMOS PA

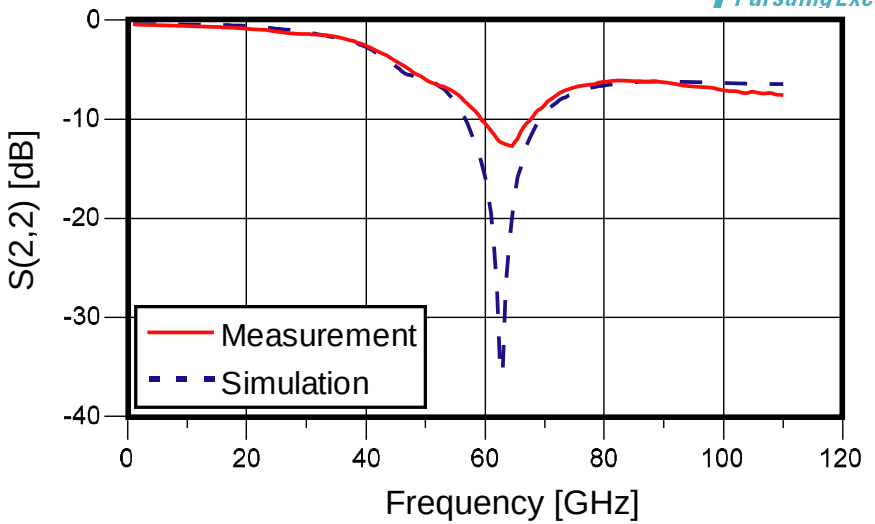


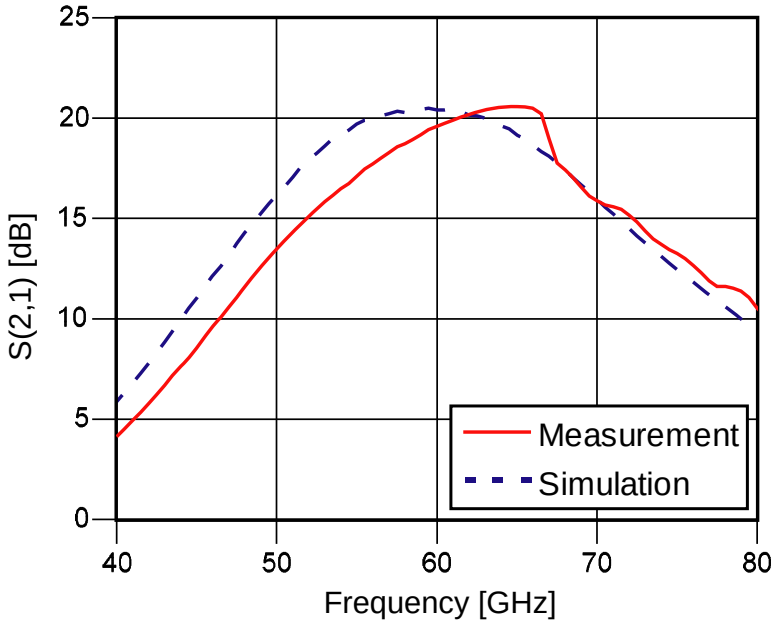
CMOS 65nm process

Matsuzawa & Okada Lab.

Measurement results





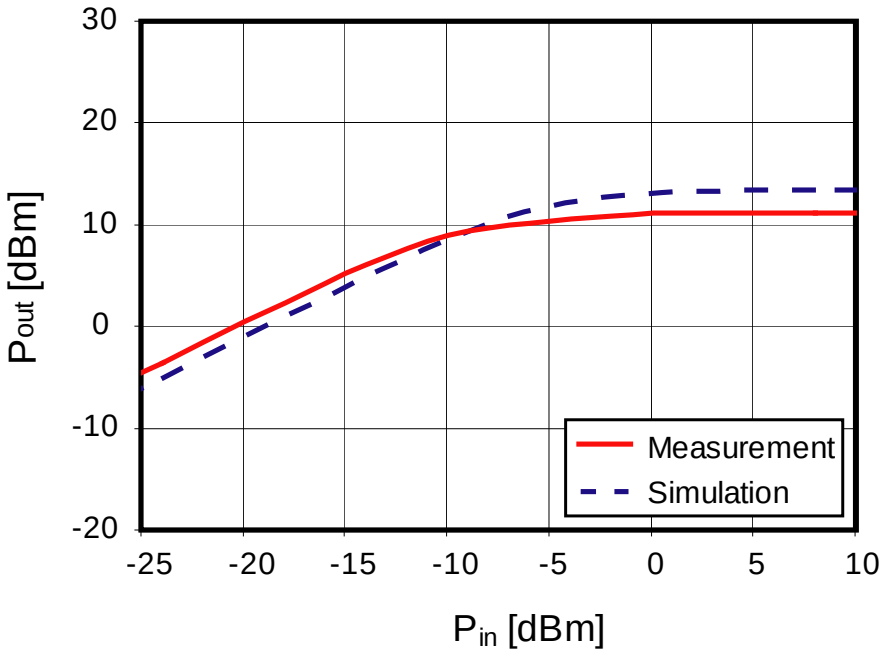


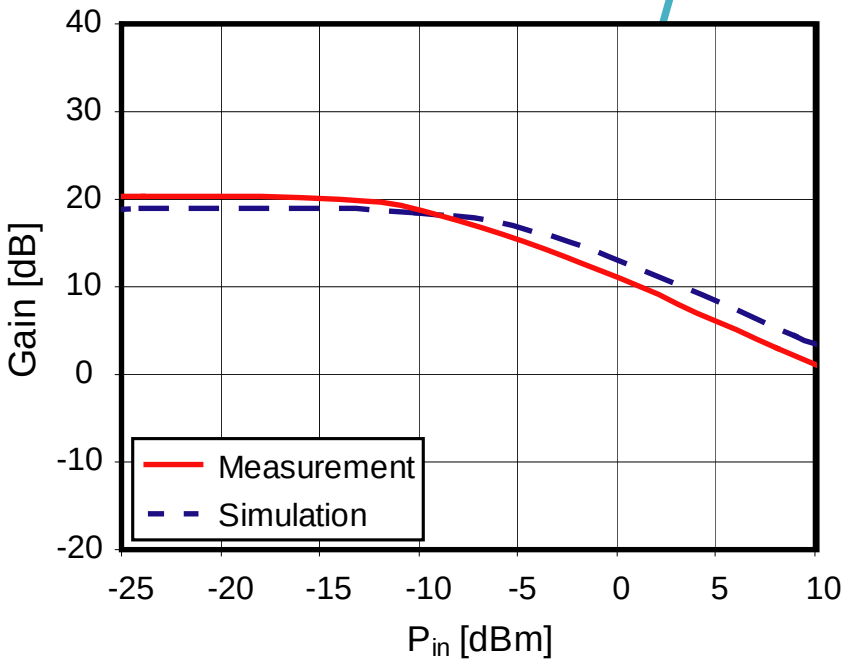
@61.5GHz

S_{21}: >20dB

S_{22}: <-10dB

Measurement results





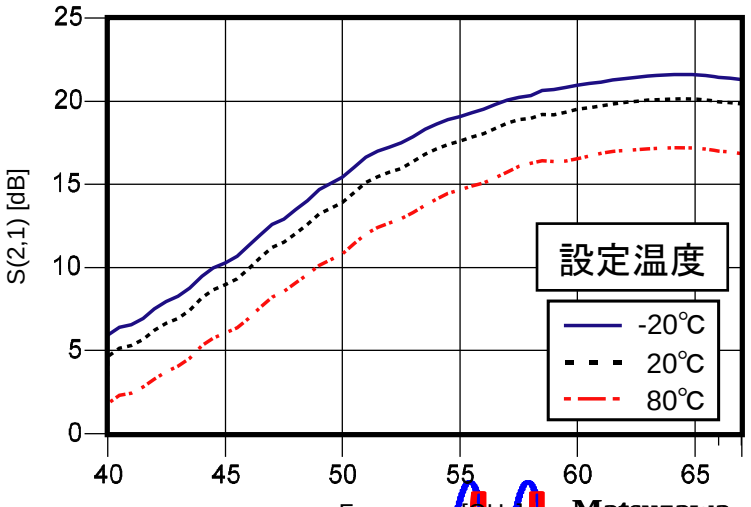
@61.5GHz

PG: 20.4dB

P_{1dB}: 9.9dBm

P_{sat}: 11.1dBm

P_{DC}: 144mW @P_{1dB}



Measurement summary

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Reference	Technology	Freq. [GHz]	Gain [dB]	P_{1dB} [dBm]	PAE@P_{1dB} [%]	P_{DC} [mW]	V_{DD} [V]
[4] JSSCC 2007	90nm CMOS	61	5.2	6.4	7.4	21	1.5
[5] RFIC 2008	90nm CMOS	63	14	11	15	81	1.2
[6] ISSCC 2008	90nm CMOS	60	8.2	8.2	2.4	229	1.2
[7] ISSCC 2008	90nm CMOS	60	5.5	9	6	80	1
[8] ISSCC 2008	90nm CMOS	60	13.3	10.5	8	150	1
[9] ISSCC 2009	65nm CMOS	60	15.8	2.5	3.95	43.5	1
[10] ISSCC 2009	45nm CMOS	60	13.8	11	-	-	1.1
[11] MWCL 2009	90nm CMOS	60	30	10.3	6	178	1.8
This work	**65nm CMOS**	**61.5**	**20**	**9.9**	**6.7**	**144**	**1.2**

[4] T.Yao, *et al*., JSSC 2007(Tronto Univ.) [5] T.L.Rocca, *et al*., RFIC 2008 (UCLA) [6] T.Suzuki, *et al*., ISSCC 2008 (Fujitsu)
[7] D. Chowdhury, *et al*., ISSCC 2008 (UCB) [8] M. Tanomura, *et al*., ISSCC 2008 (NEC)
[9] W.L. Chan, *et al*., ISSCC 2009 (Delft Univ.) [10] K. Raczkowski, *et al*., ISSCC 2009 (KU Leuven&IMEC)
[11] J.-L.Kuo, *et al*., MWCL 2009 (NTU)

まとめ

TOKYO TECH Pursuing Excellence

- **伝送線路によるマッチング**
  寄生素子の排除
- **タイルベースレイアウト**
  厳密にレイアウトとモデルを一致させる
- **実測に基づくIn-house PDK**
  ADS提供モデルを流用
  ただし、レイアウト依存・周波数依存は、
  Heuristicにモデル化