0.2V電源で動作可能な 0.114mWデュアルコンダクション Class-C VCO

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Outline of Presentation

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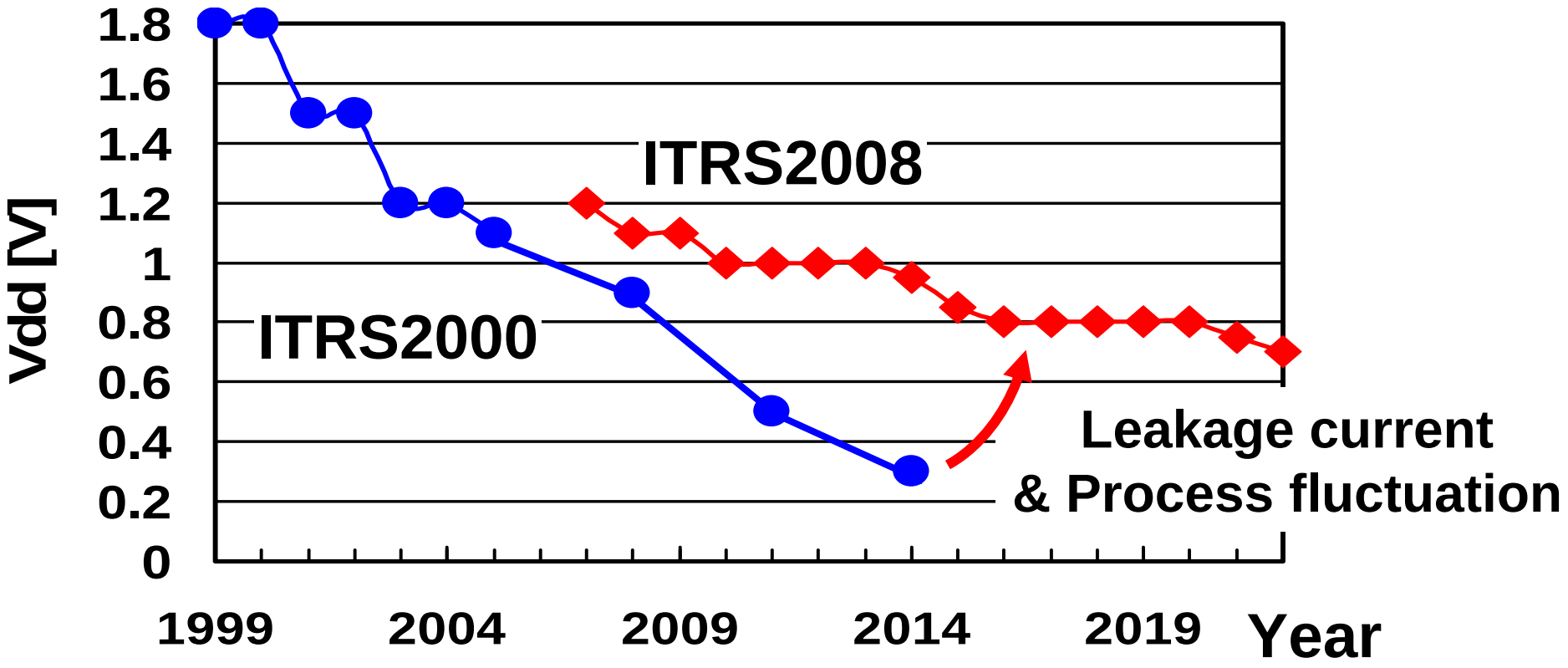
- Motivation
  - Supply voltage scaling
  - Jitter degradation
- Low-voltage VCO's issues
- The proposed Dual-Conduction topology
  - Low-power and Low-phase noise with a very low supply voltage
- Measurement results
- Conclusions

電源電圧のスケーリング



The voltage scaling is required again.
Low-voltage circuit design is challenging.

位相雑音の比較

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LC-VCO [A.Mazzanti, et al., JSSC 2008]

$$\frac{\omega_0^2}{\omega_{\text{offset}}^2}\cdot\frac{kT}{V_{\text{DD}}I_{\text{bias}}}\cdot\frac{1+\gamma_n}{Q^2}$$

+30dB worse

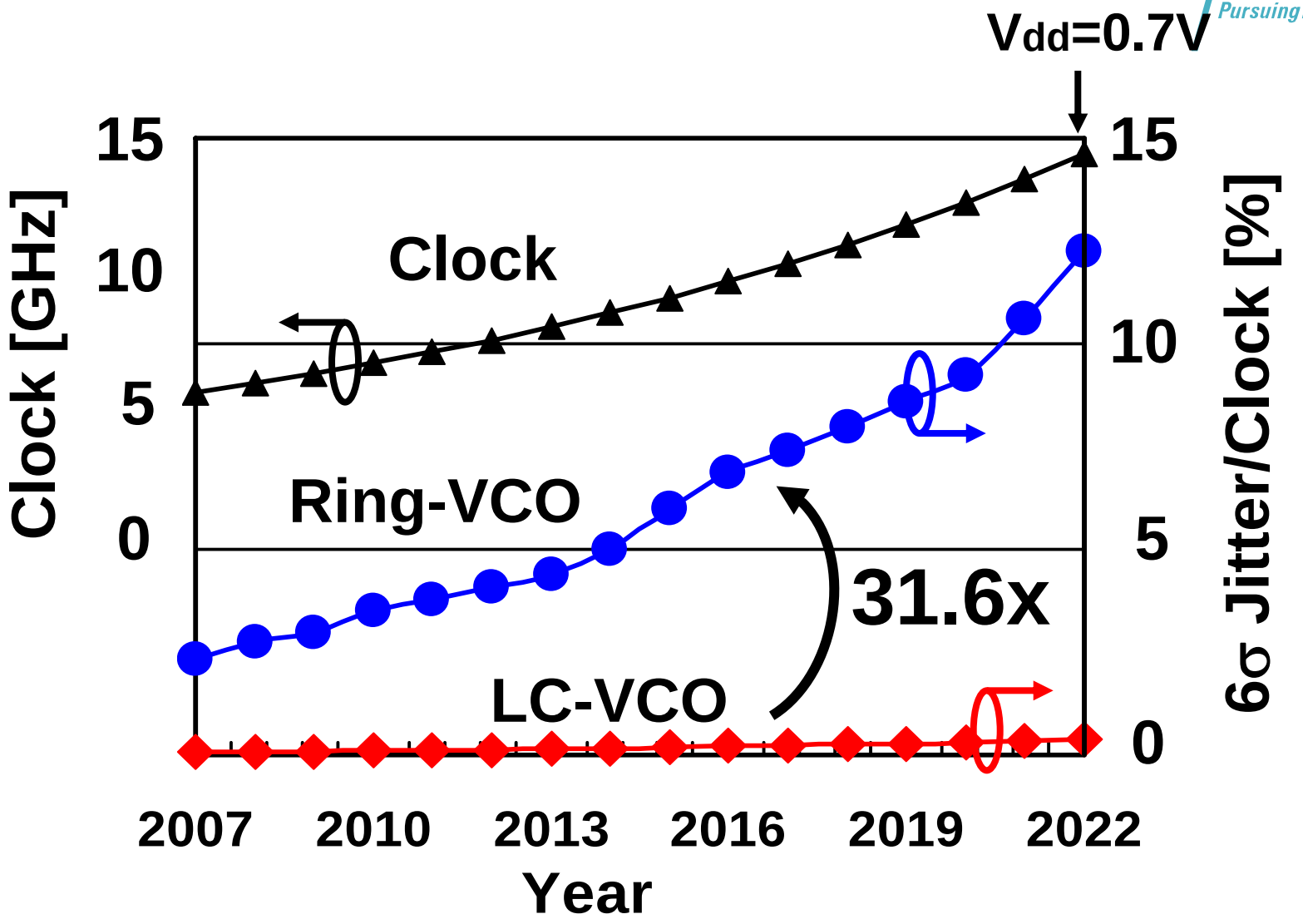
Ring-VCO [A.Abidi, JSSC 2006]

$$\frac{\omega_0^2}{\omega_{\text{offset}}^2}\cdot\frac{kT}{V_{\text{DD}}I_{\text{bias}}}\cdot 2M\left\{\frac{V_{\text{DD}}}{V_{\text{DD}}-V_{\text{TH}}}(\gamma_n+\gamma_p)+1\right\}$$

M: #stages

$$V_{\text{TH}}=\frac{V_{\text{DD}}}{4},\ \gamma_n=\gamma_p=\frac{2}{3},\ M=3,\ Q=10$$

ジッタのスケーリング



With the same power consumption, LC-VCO has much smaller jitter performance.

リングオシレータのジッタ劣化

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Vdd	Type	Pdc	Phase Noise +10dB margin	Jitter
1.2	LC	1mW	-121.6 dBc/Hz-1MHz	0.16ps (0.074%)
	Ring	1mW	-91.6 dBc/Hz-1MHz	5.0ps (2.3%)
0.5	LC	0.17mW	-114.0 dBc/Hz-1MHz	0.38ps (0.67%)
	Ring	0.17mW	-84.0 dBc/Hz-1MHz	12.0ps (21%)
		174mW	-114.0 dBc/Hz-1MHz	0.38ps (0.67%)

LC型とリング型の比較

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・LC-VCOと分周器を組み合わせることにより、
面積の縮小と周波数可変範囲の拡大が可能
・単純に消費電力だけを比較すると、高い周波数ほどLC型が低消費電力
・ジッタ性能が厳しい場合は、LC型が有利な周波数帯はどんどん低くまで広がる
・面積の問題はなくなる

リング型が有利な場合
- ジッタ仕様が緩く、周波数が100MHz程度以下の場合

LC型が有利な場合
- それ以外すべて

比較項目
ジッタ、消費電力、周波数可変範囲、回路面積、最高発振周波数

Clock Generation with Low Vdd

- Lowering of supply voltage is required to realize high-speed and low-active-power circuits.
- Jitter will become larger according to the voltage scaling.
- Ring-VCO become infeasible due to too large jitter and too large power consumption.
- To reduce the power consumption of the clock generator, use of LC-VCOs is an unavoidable way in such the low-voltage condition.

Low-Voltage LC-VCO

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- Transformer-Feedback VCO can operate with a low supply voltage.
- 0.5V and 0.35V VCOs are reported.

[1] K. Kwok, and H. C. Luong, JSSC 2005

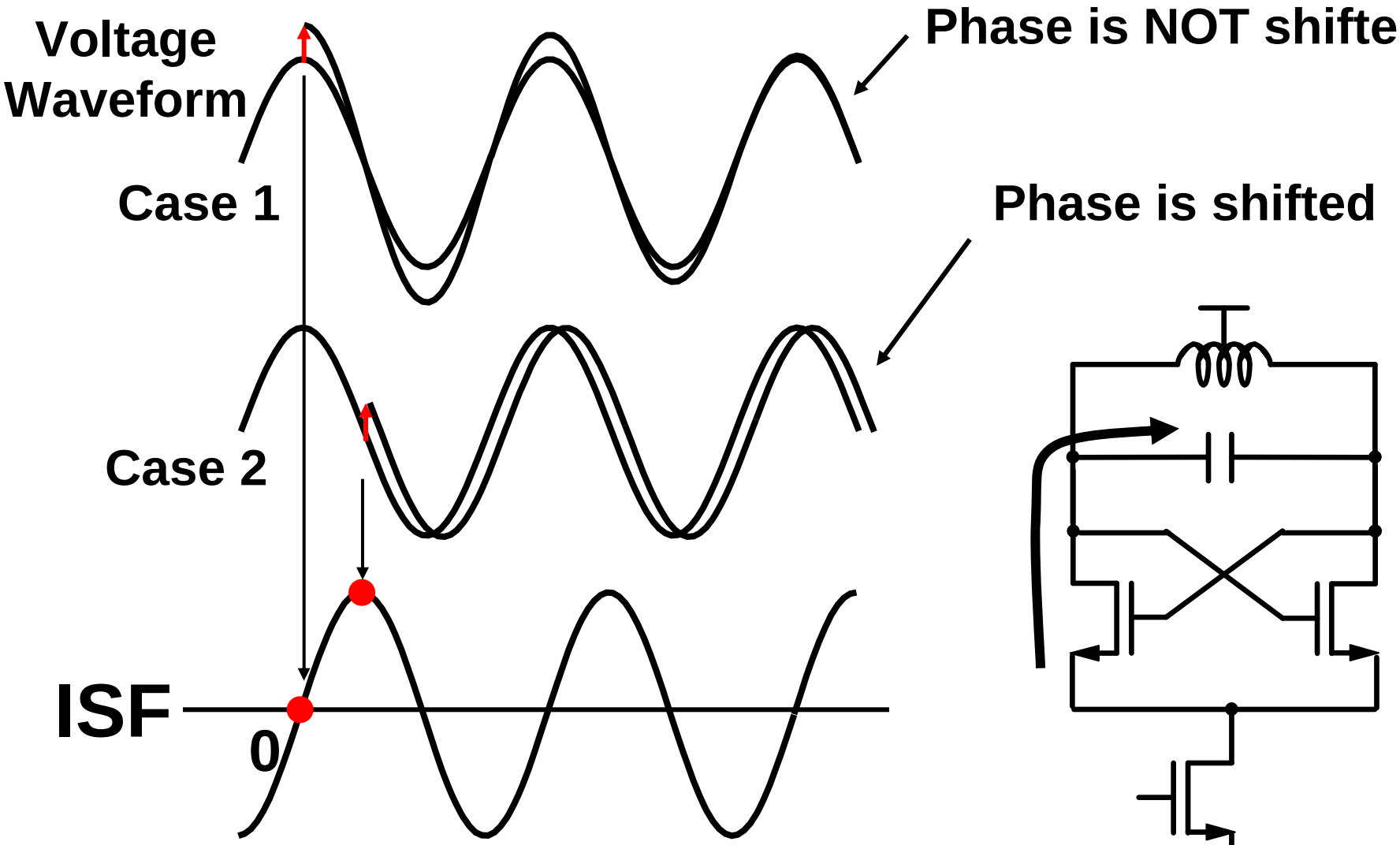
- Class-C VCO achieves 196dBc/Hz of FoM.
- Startup is an issue of Class-C VCO under the low-voltage condition.

[2] A. Mazzanti, and P. Andreani, JSSC 2008

Summary of This Work

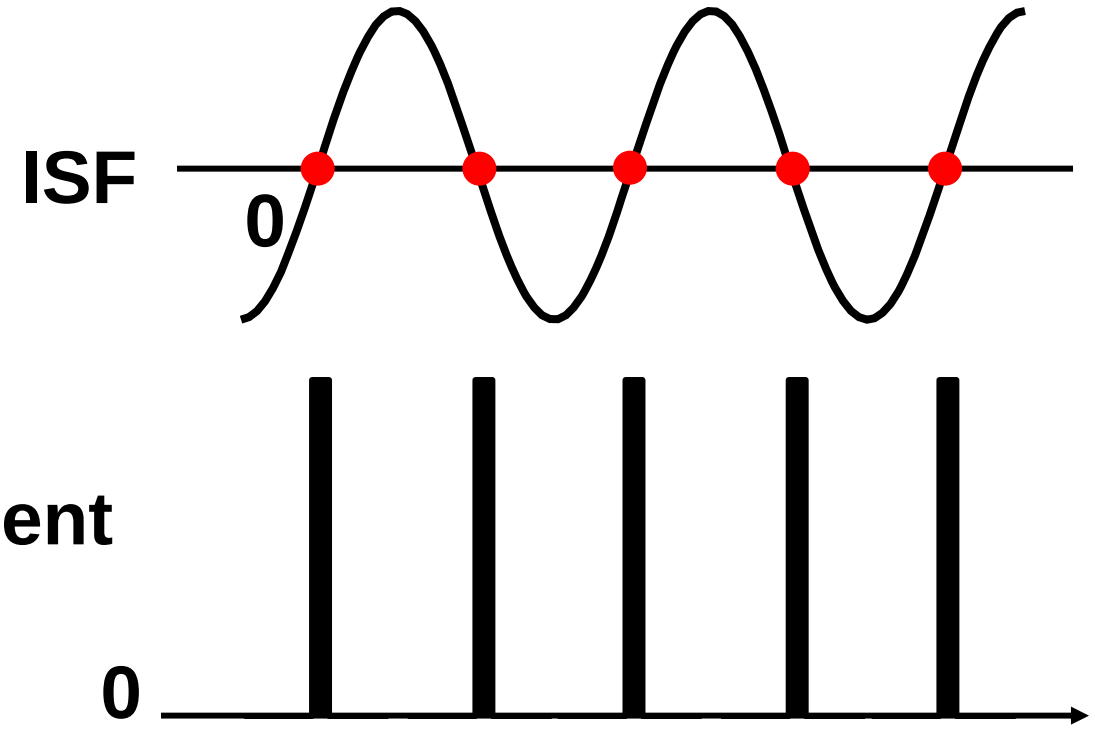
- Sub-0.5V LSI
- A Dual-Conduction topology is proposed for Class-C VCO in this work.
- It is modified to work with a very low supply voltage.
- 0.2V VCO is realized by using a 0.18μm CMOS process with 114μW of power consumption.

Impulse Sensitivity Function (ISF)

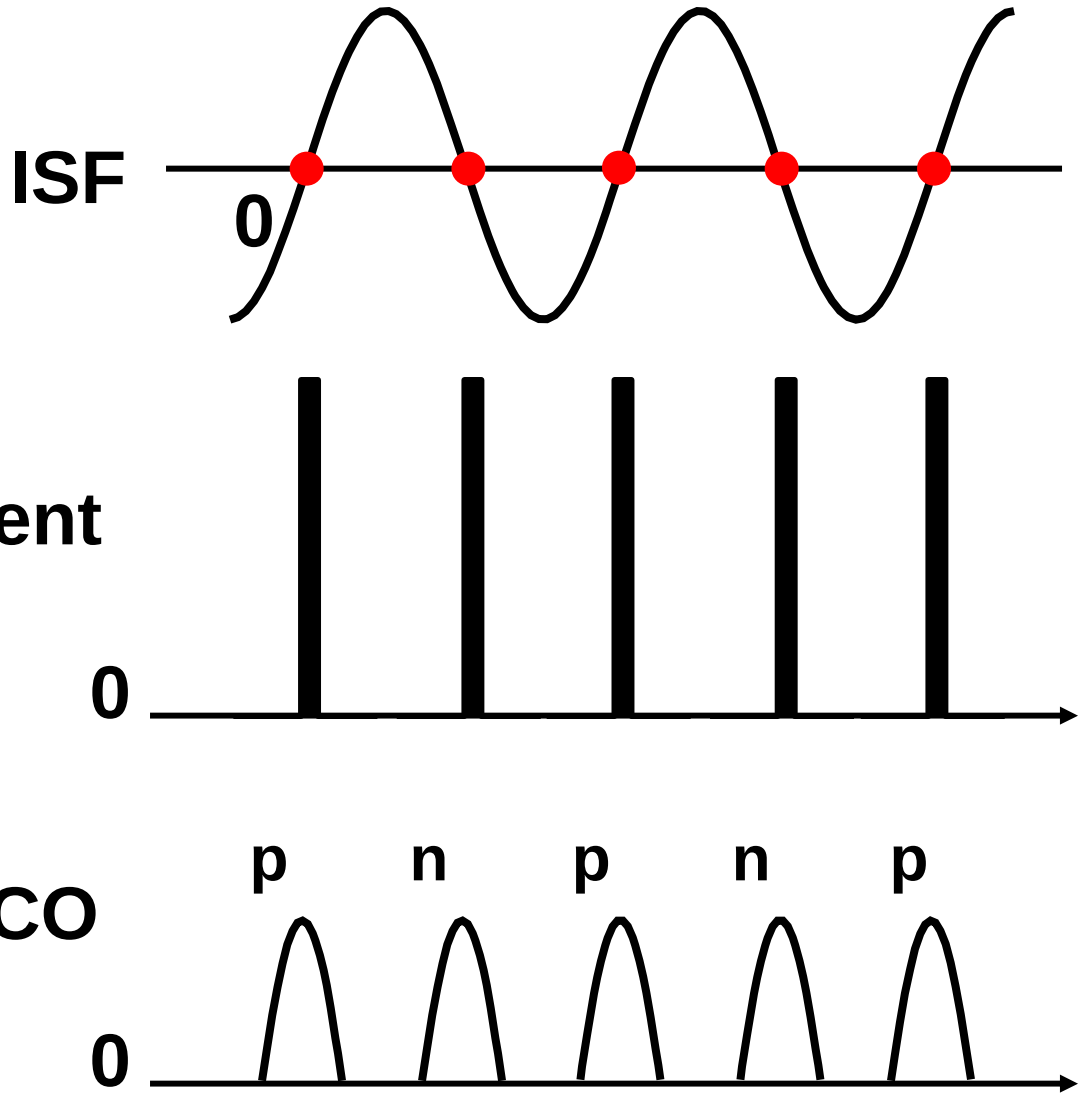


[3] A.Hajimiri, and T.Lee, JSSC 1998

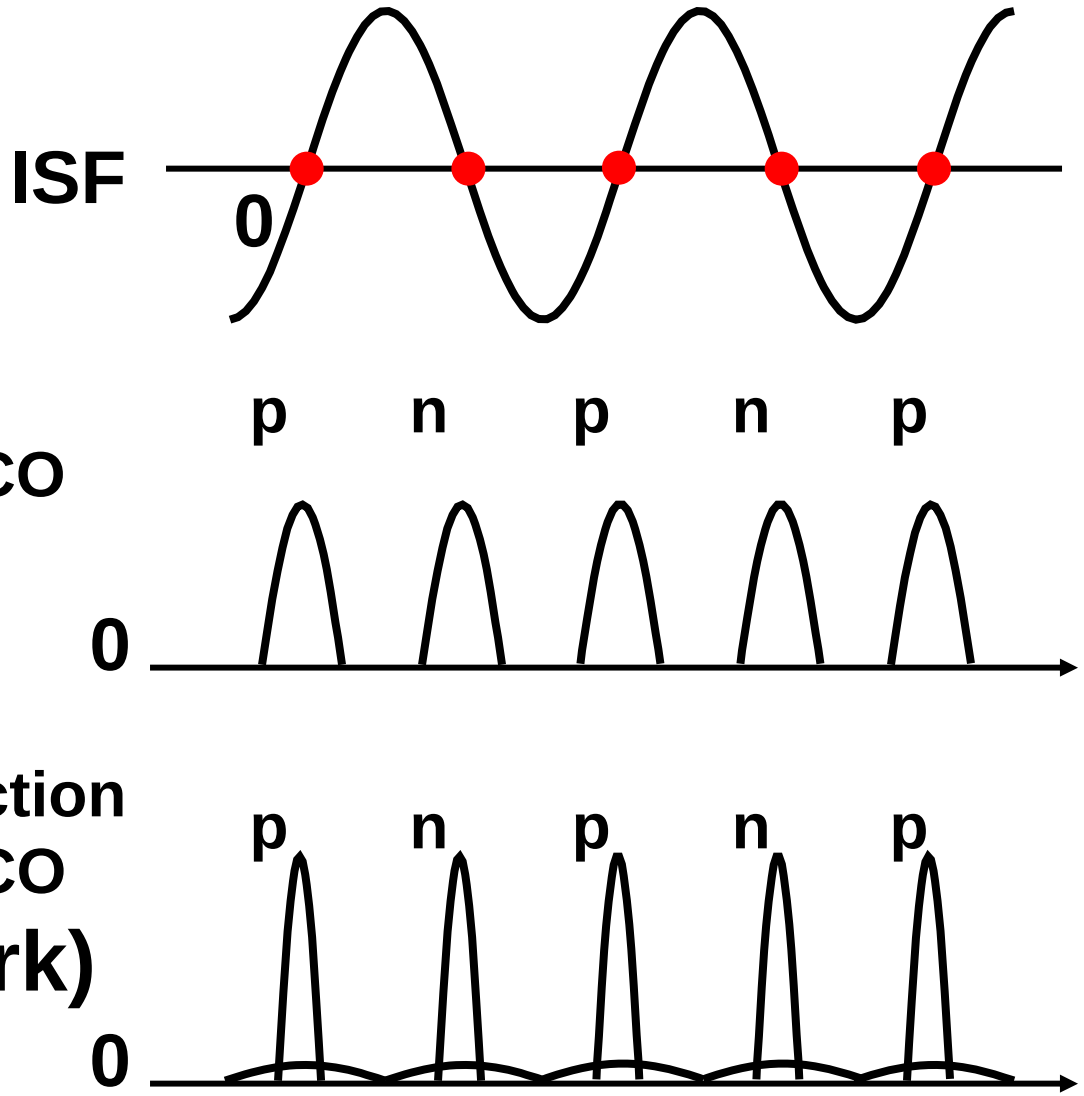
Ideal Current Conduction



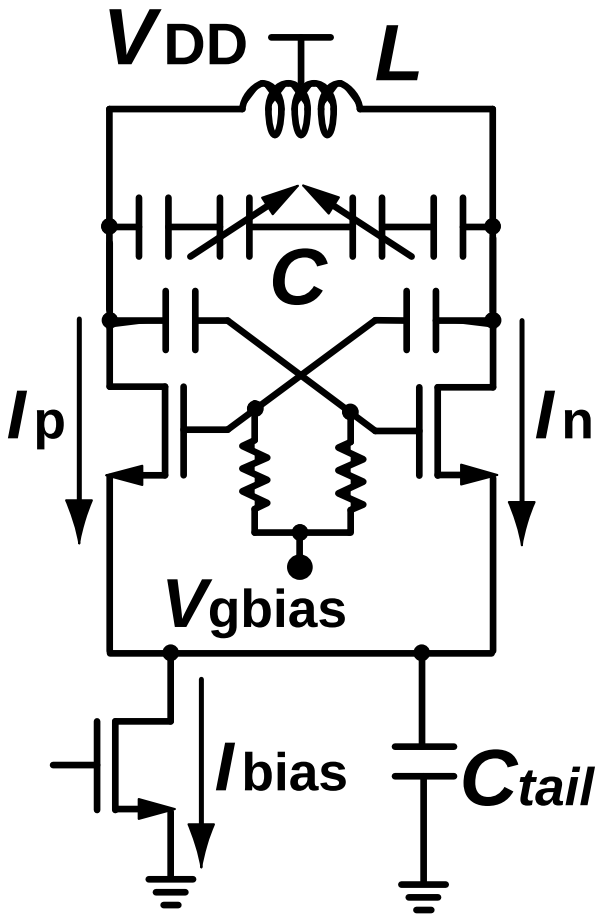
Current Conduction of Class-C VCOs

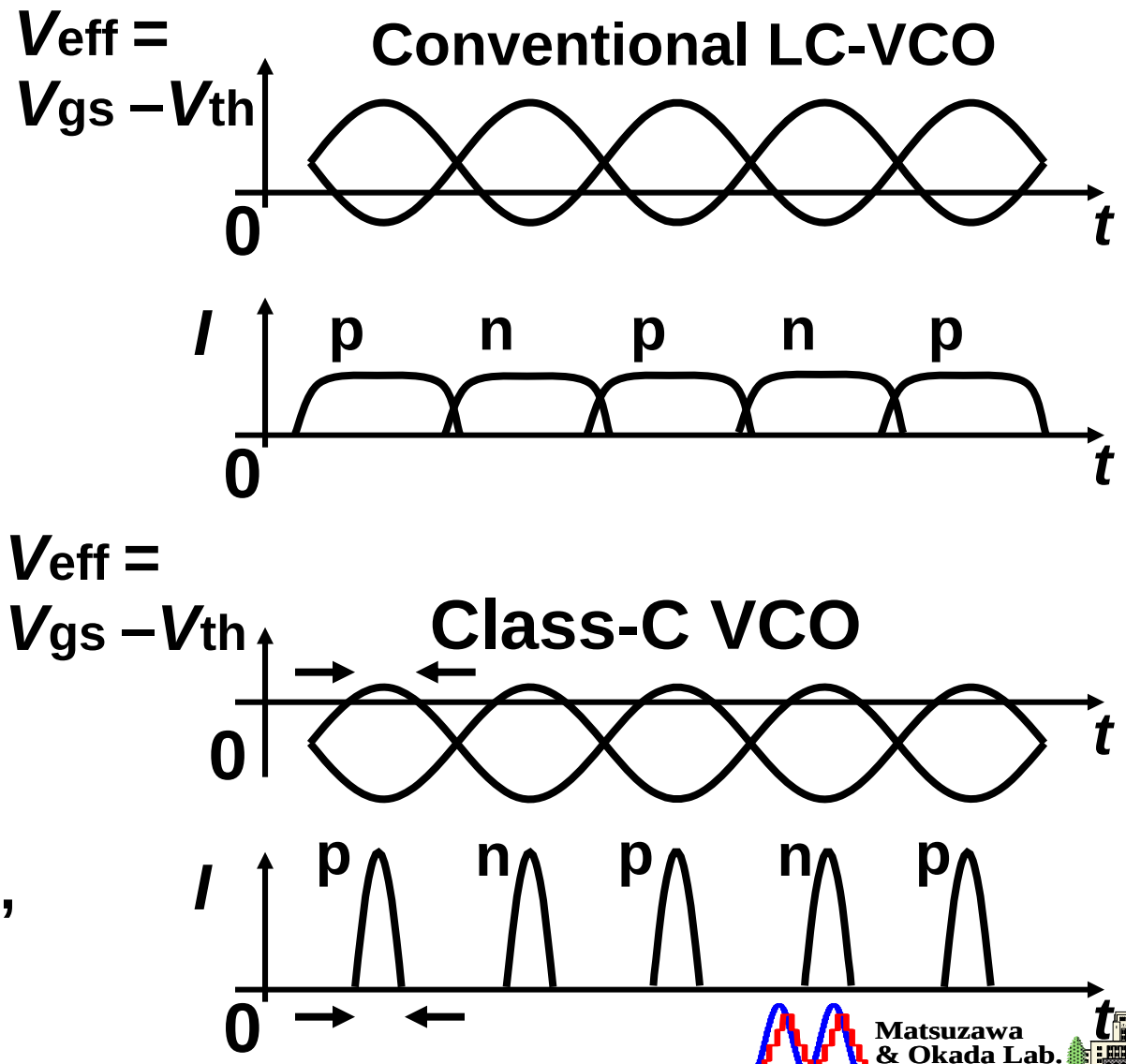


Current Conduction of Class-C VCOs



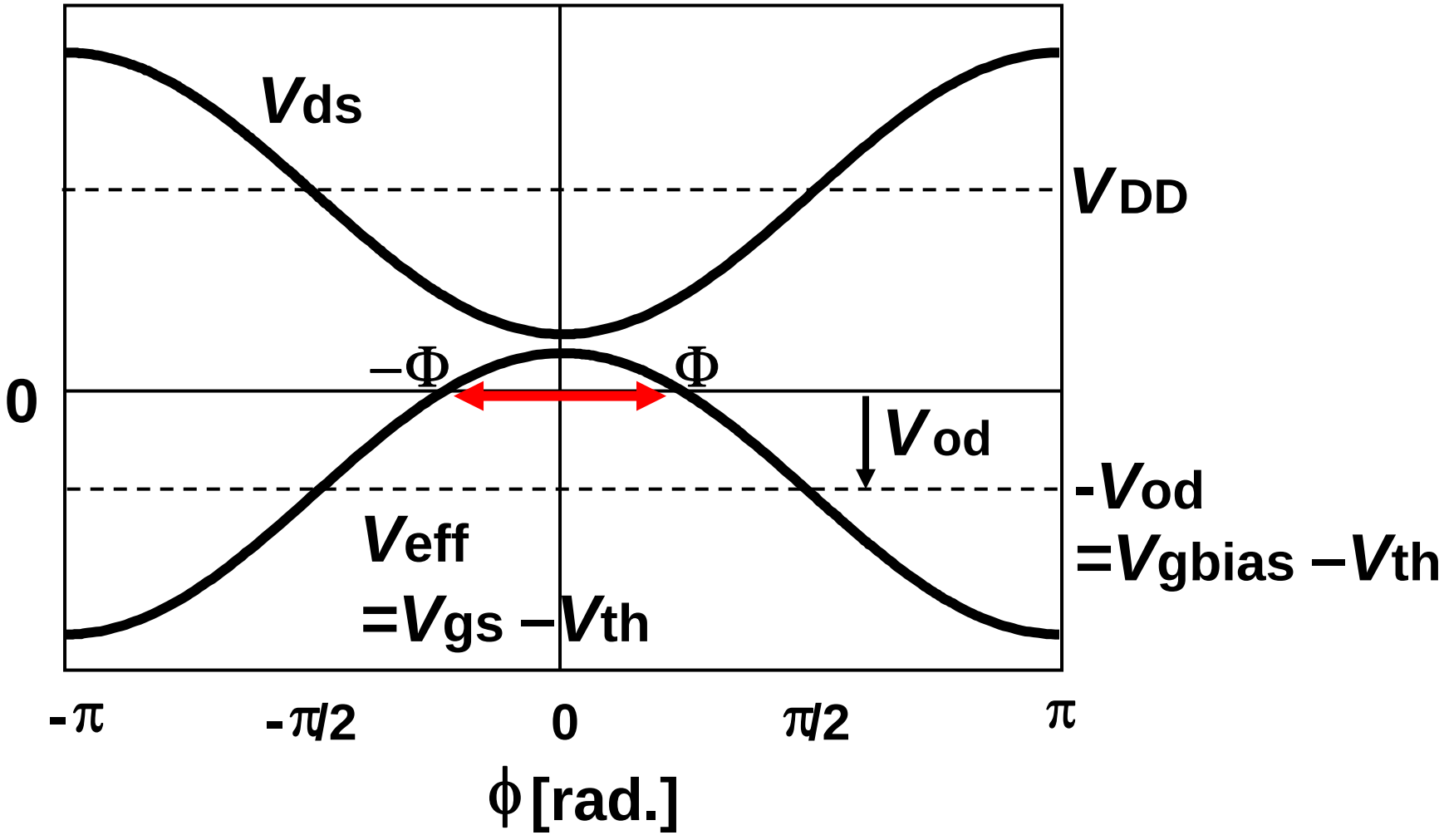
Class-C VCO[2]





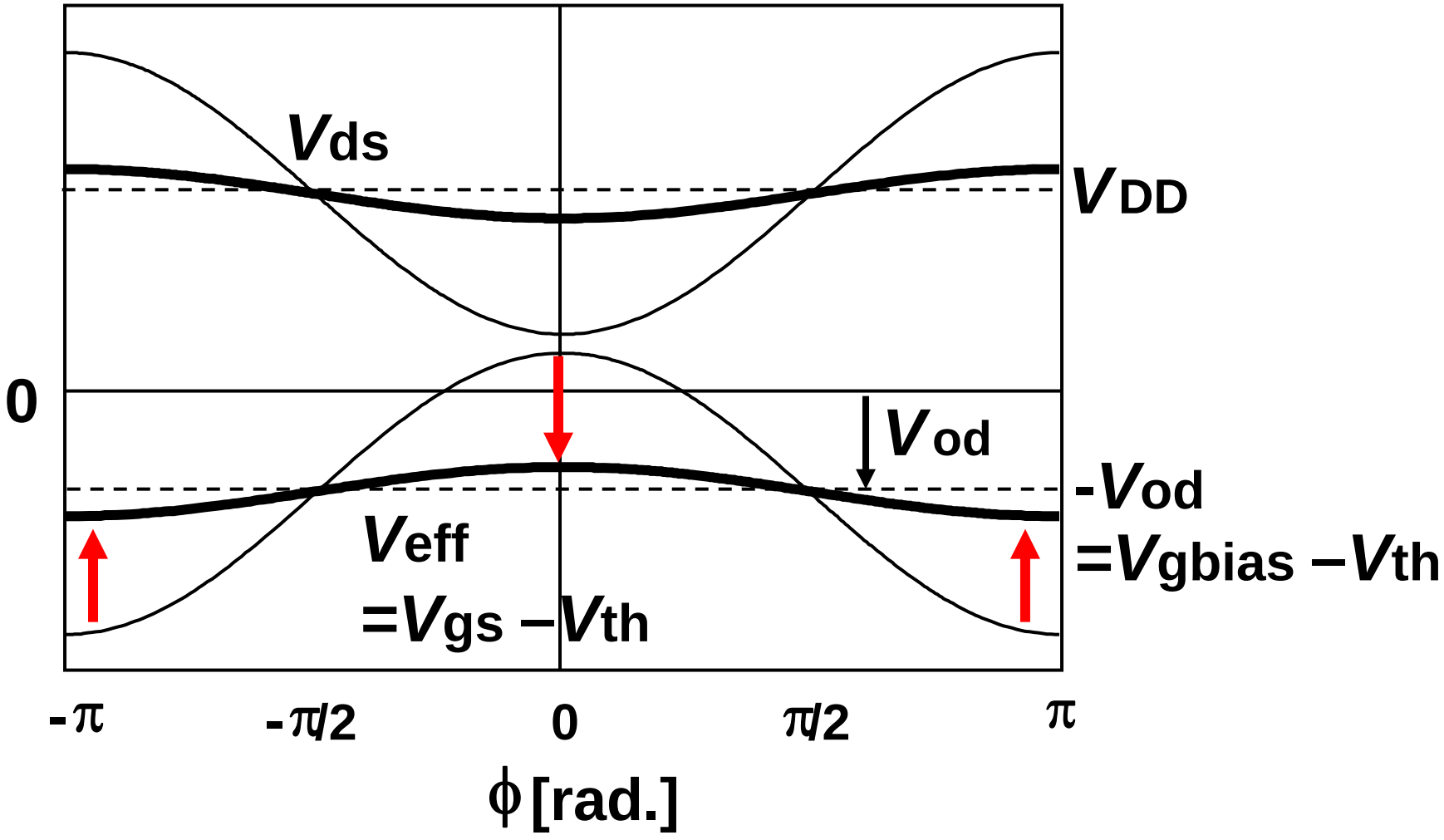
[2] A. Mazzanti, *et al*., JSSC 2008

Condition for Class-C Operation



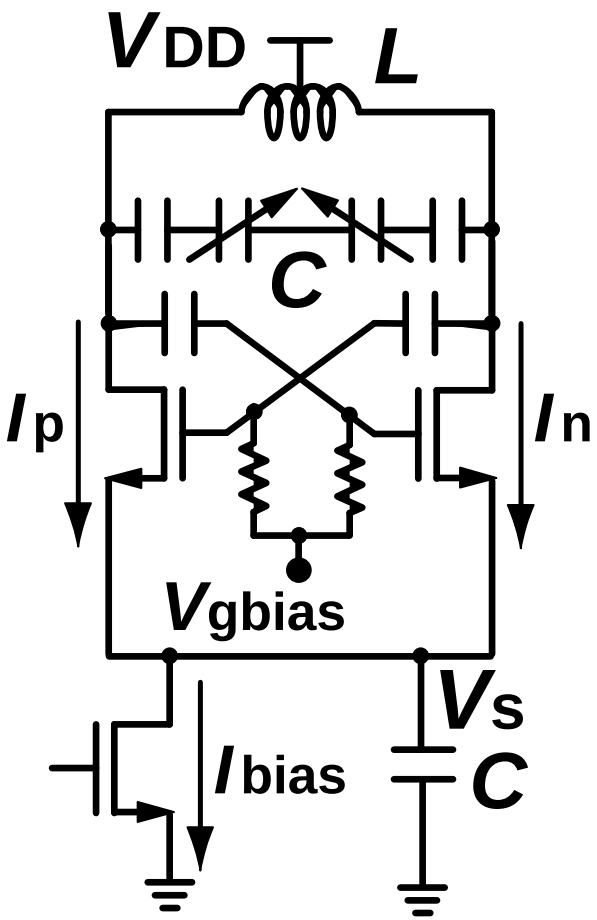
Active region: $V_{ds} > V_{eff}$

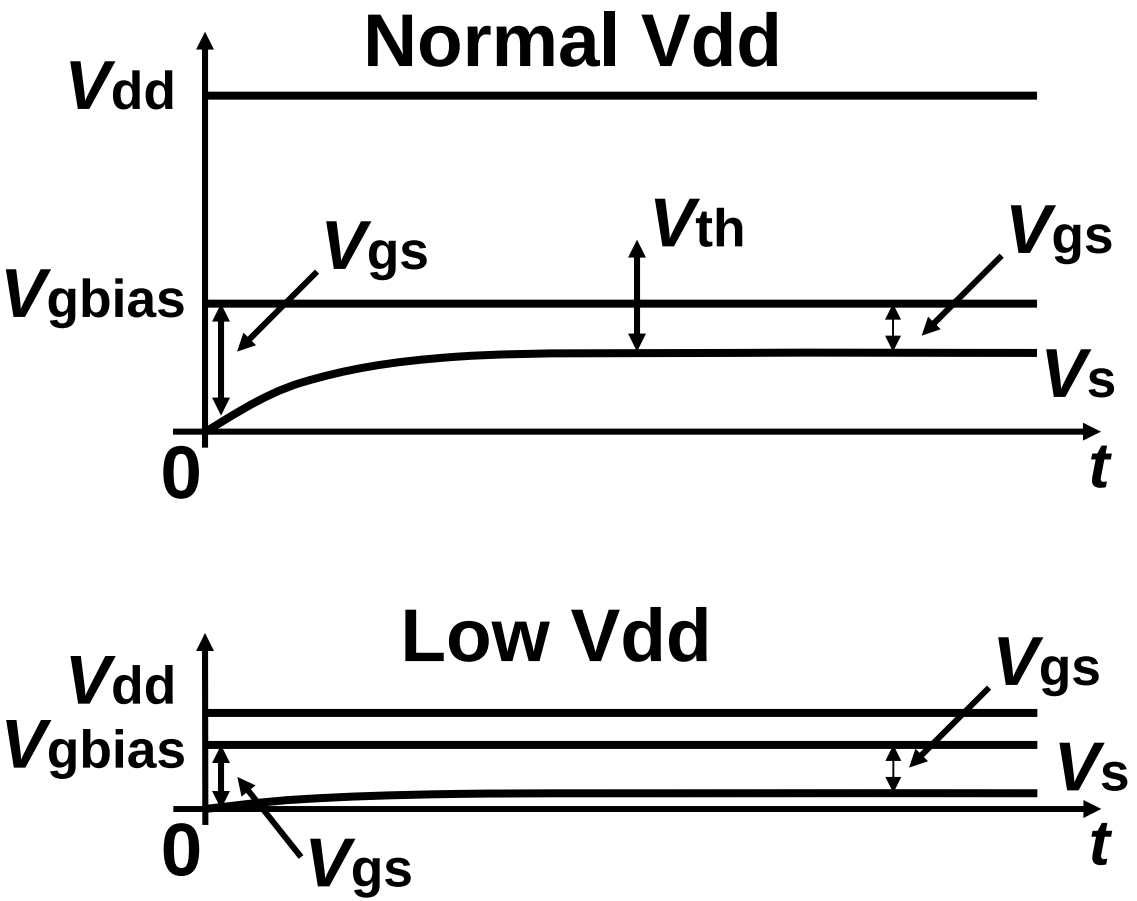
Issue of Class-C VCO for Low Vdd



V_{od} has to be small due to the start-up problem, so conduction angle cannot be reduced.

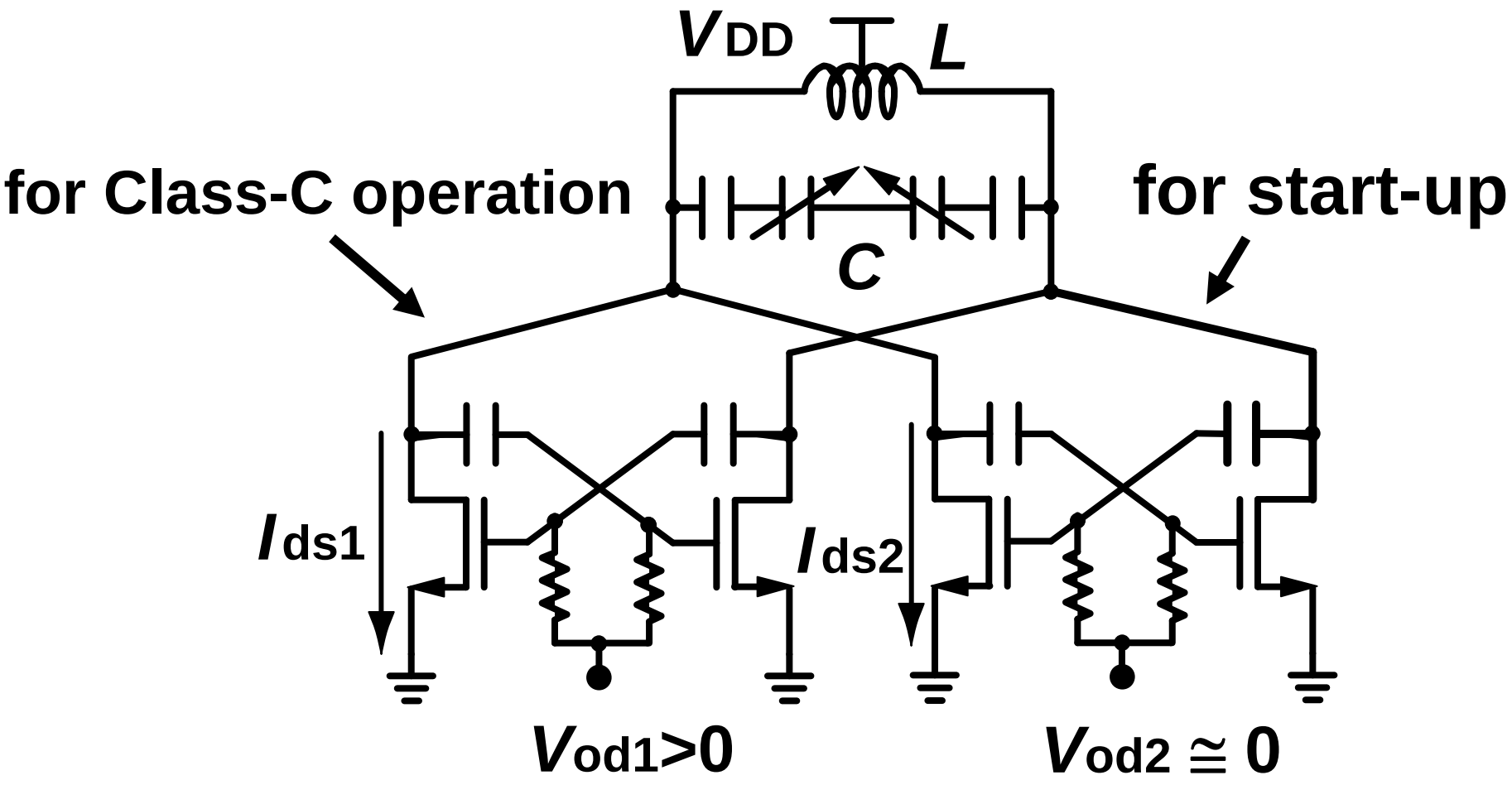
Initial Boosting of Gate Bias



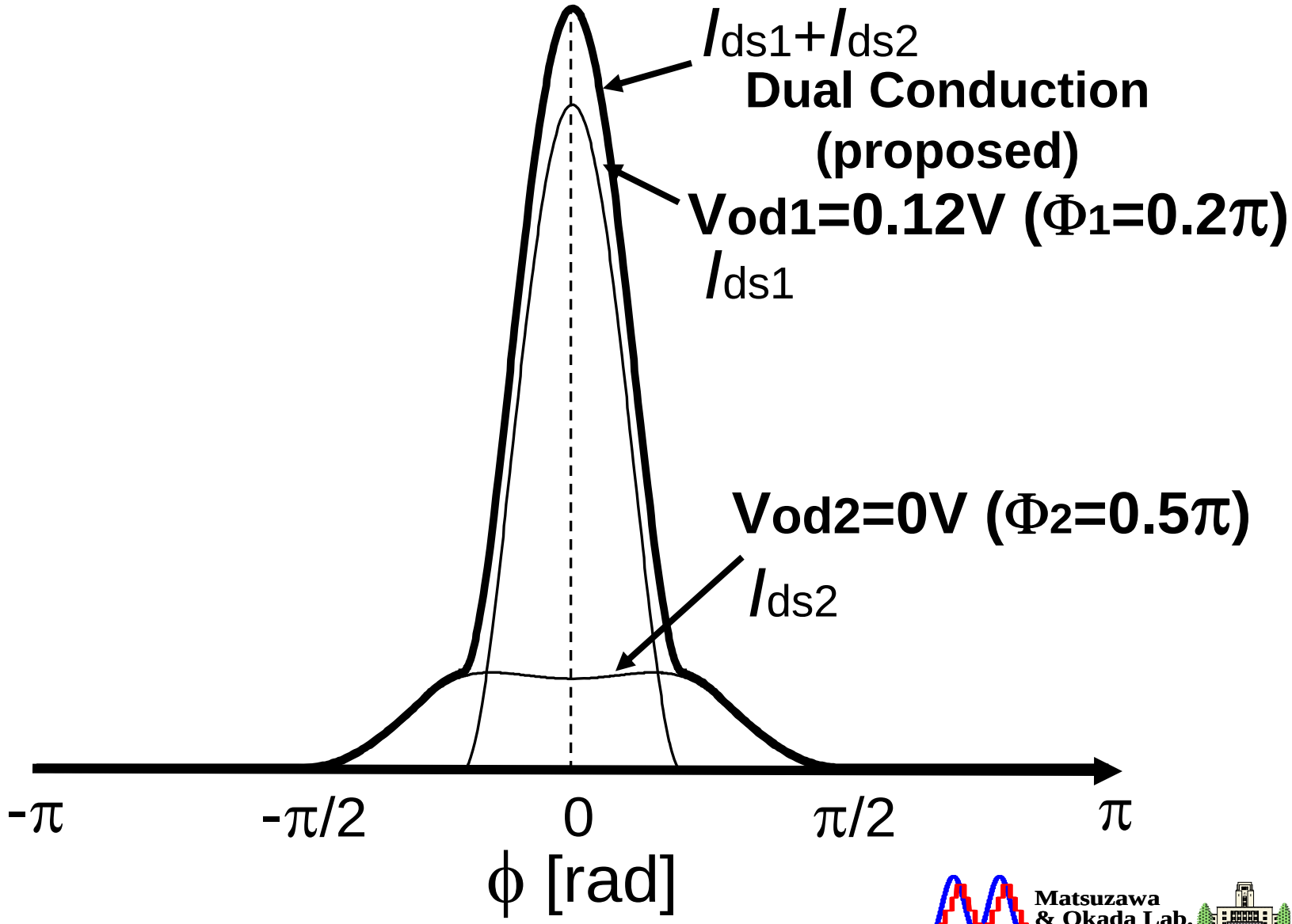


Initial Vgs boosting cannot be expected in a low-Vdd design.

Dual-Conduction Class-C VCO (Proposed)



Dual-Conduction Current Waveform



Comparison of Current Waveforms

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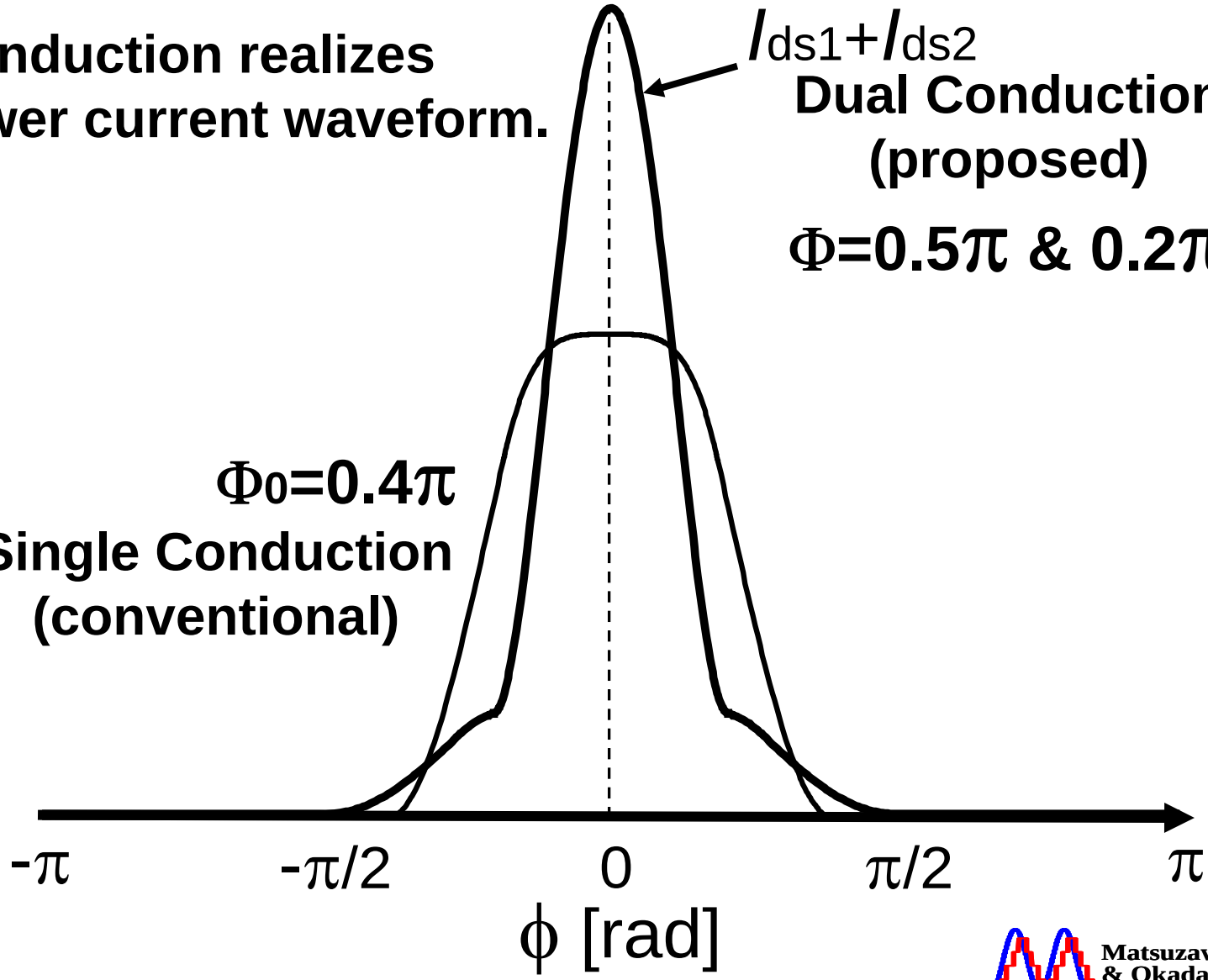
Dual Conduction realizes a narrower current waveform.



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Analytical Comparison

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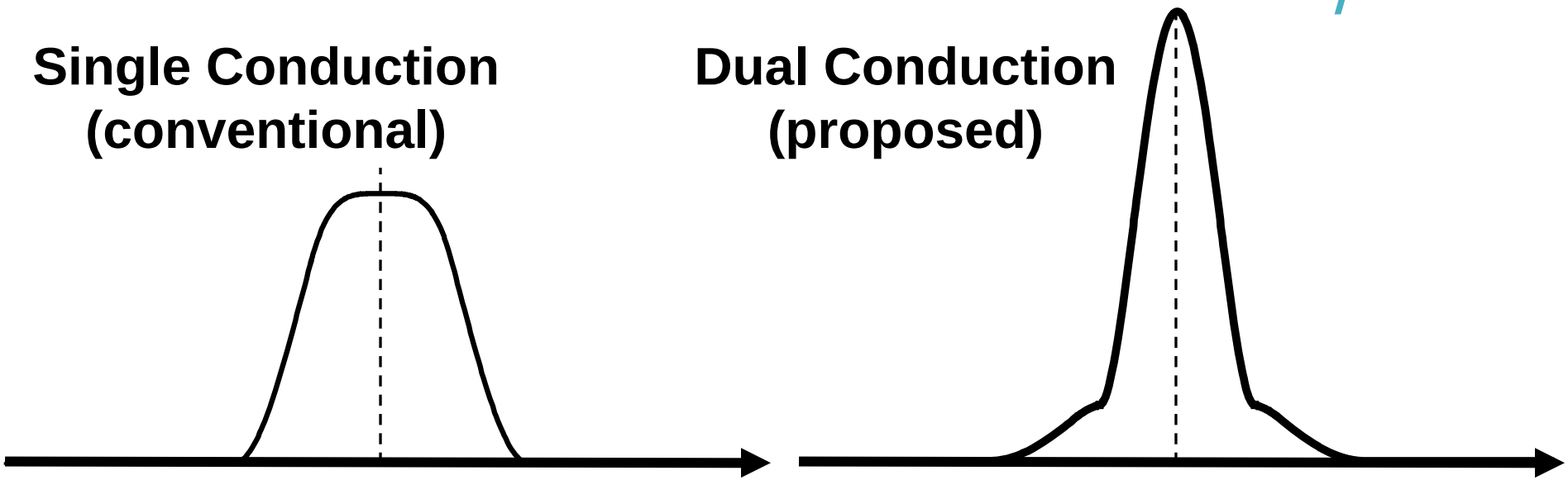
Single Conduction (conventional)

Dual Conduction (proposed)



V_{od}=0.05V (Φ_0=0.4π)

PN: -106dBc/Hz-1MHz

Pdc: 168μW

FoM: 188dBc/Hz

V_{od1}=0.12V (Φ_1=0.2π)

V_{od2}=0V (Φ_2=0.5π)

PN: -109dBc/Hz-1MHz

Pdc: 162μW

FoM: 191dBc/Hz

(*) V_{dd}=0.2V, A=0.15V, V_{th}=0.5V, f_0=5GHz, Q=10

Phase Noise *vs* *V*od

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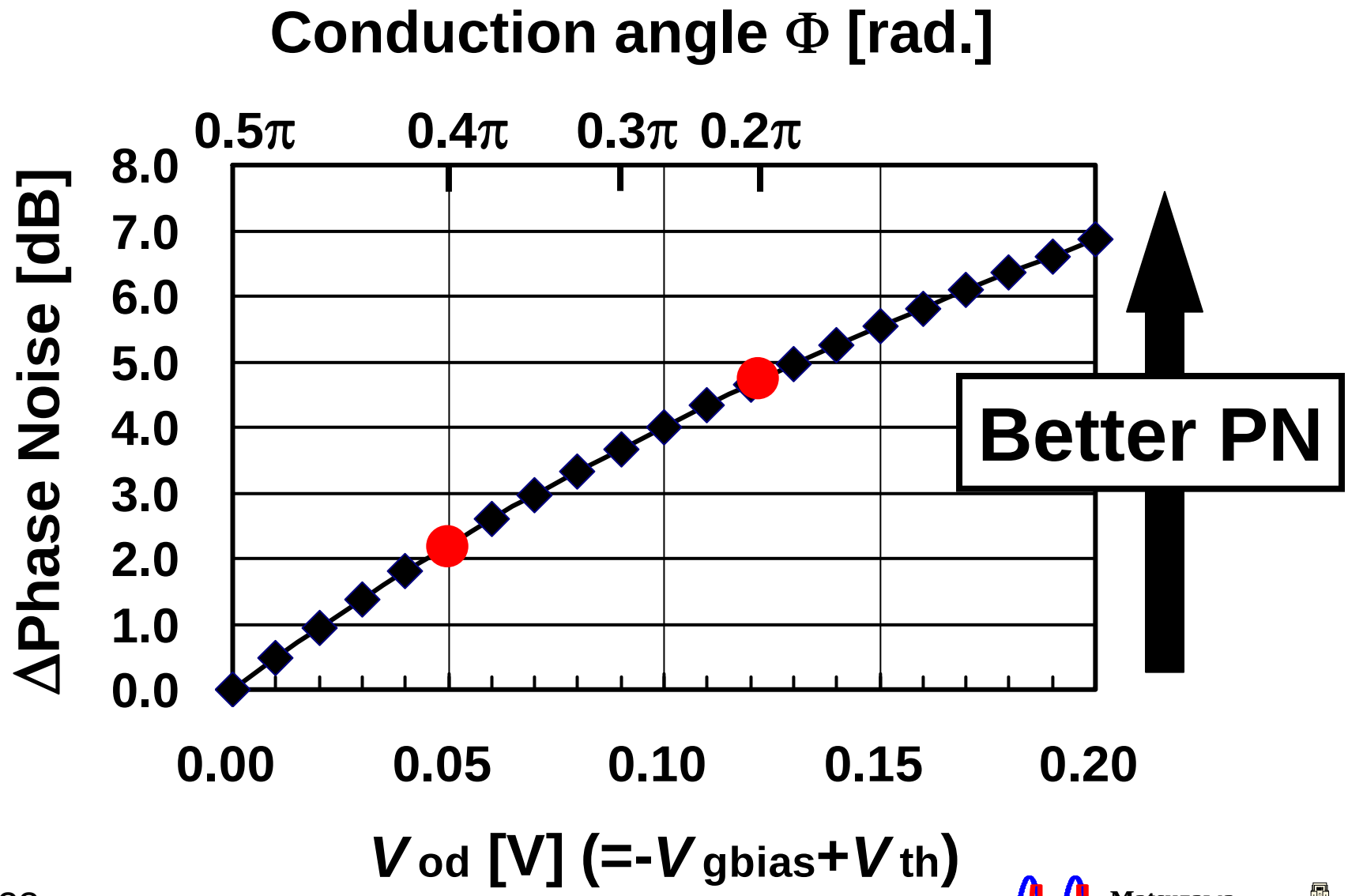

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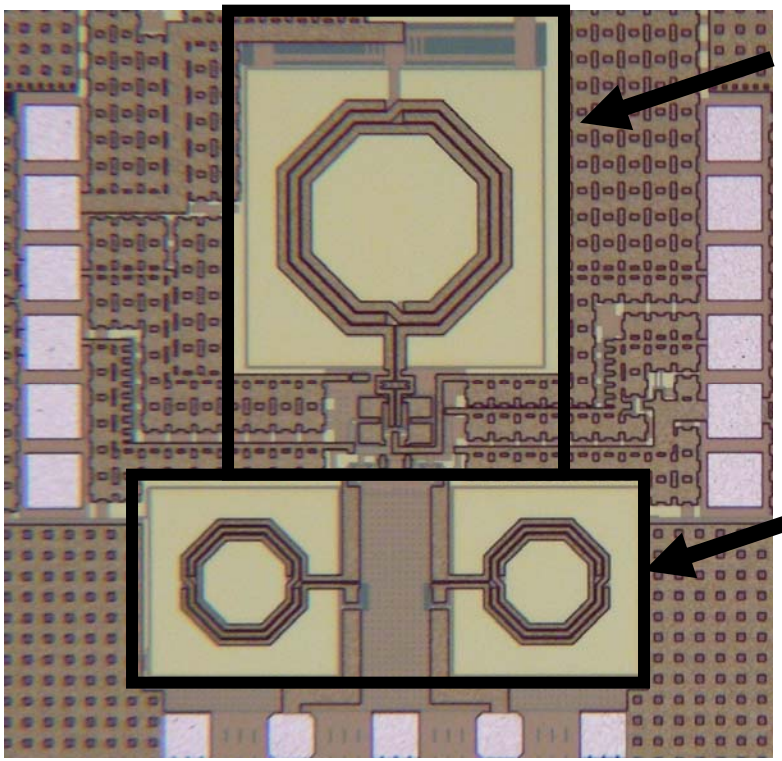
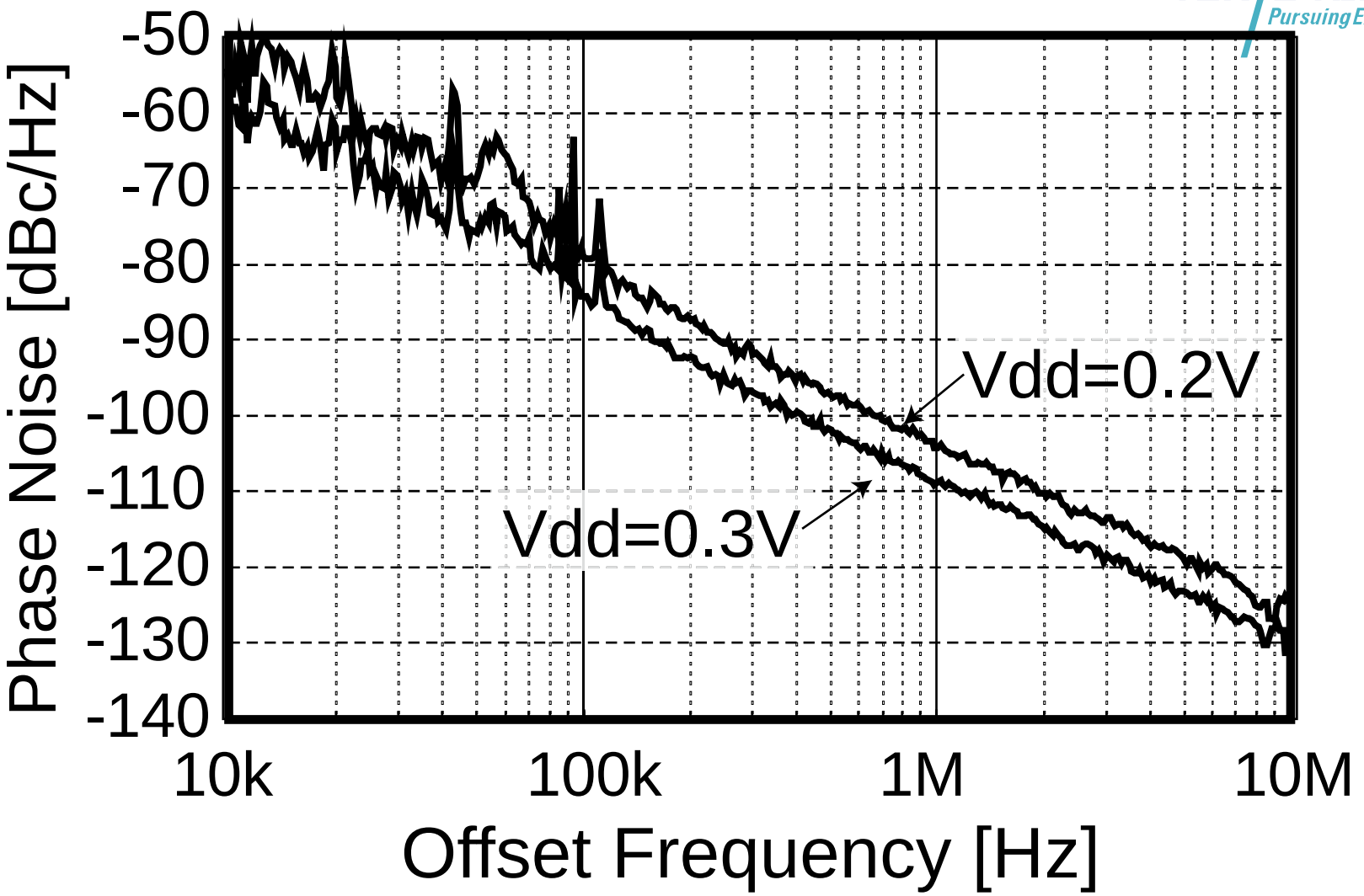
Chip Micrograph



- 0.18μm CMOS process
- 670μm x 440μm for core area

Phase Noise Measurement



V_{gbias1}=0.45, V_{gbias2}=0.55

f_0=4.5GHz

-104dBc/Hz@1MHz for 0.2V

-109dBc/Hz@1MHz for 0.3V

Performance Comparison

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	[2]	[1]		This work	
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	
Vdd [V]	1.0	0.5	0.35	**0.3**	**0.2**
P_{DC} [mW]	1.3	0.57	1.46	**0.159**	**0.114**
f_0 [GHz]	4.9	3.8	1.4	4.5	4.5
Phase noise [dBc/Hz]	-130 @3MHz	-119 @1MHz	-129 @1MHz	-109 @1MHz	-104 @1MHz
FoM [dBc/Hz]	196	193	190	190	187
Topology	Class-C (single)	Transformer feedback		Class-C (dual)	

[1] K. Kwok, *et al*., JSSC 2005 [2] A. Mazzanti, *et al*., JSSC 2008

結論

- 0.5V駆動LSIの実現に向けて、クロックジッタの問題を明らかにした。
- リング型よりもLC型の方が低電圧・低電力動作に有利であることを示した。
- Dual-Conduction構成のClass-C VCOを新規提案した。
- 従来の低電圧VCOの1/10の消費電力で動作した。0.2V電源電圧までの動作が可能であった。
- 通信用のみならず、クロック発生においてもLC型のVCOが今後益々重要となる。