High speed and low power ADC design with dynamic analog circuits

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Outline

- Overview of high speed CMOS ADCs
- ENOB and FoM of Flash ADCs
- Mismatch compensation and noise of dynamic comparators
- Summary

Overview of high speed CMOS ADCs

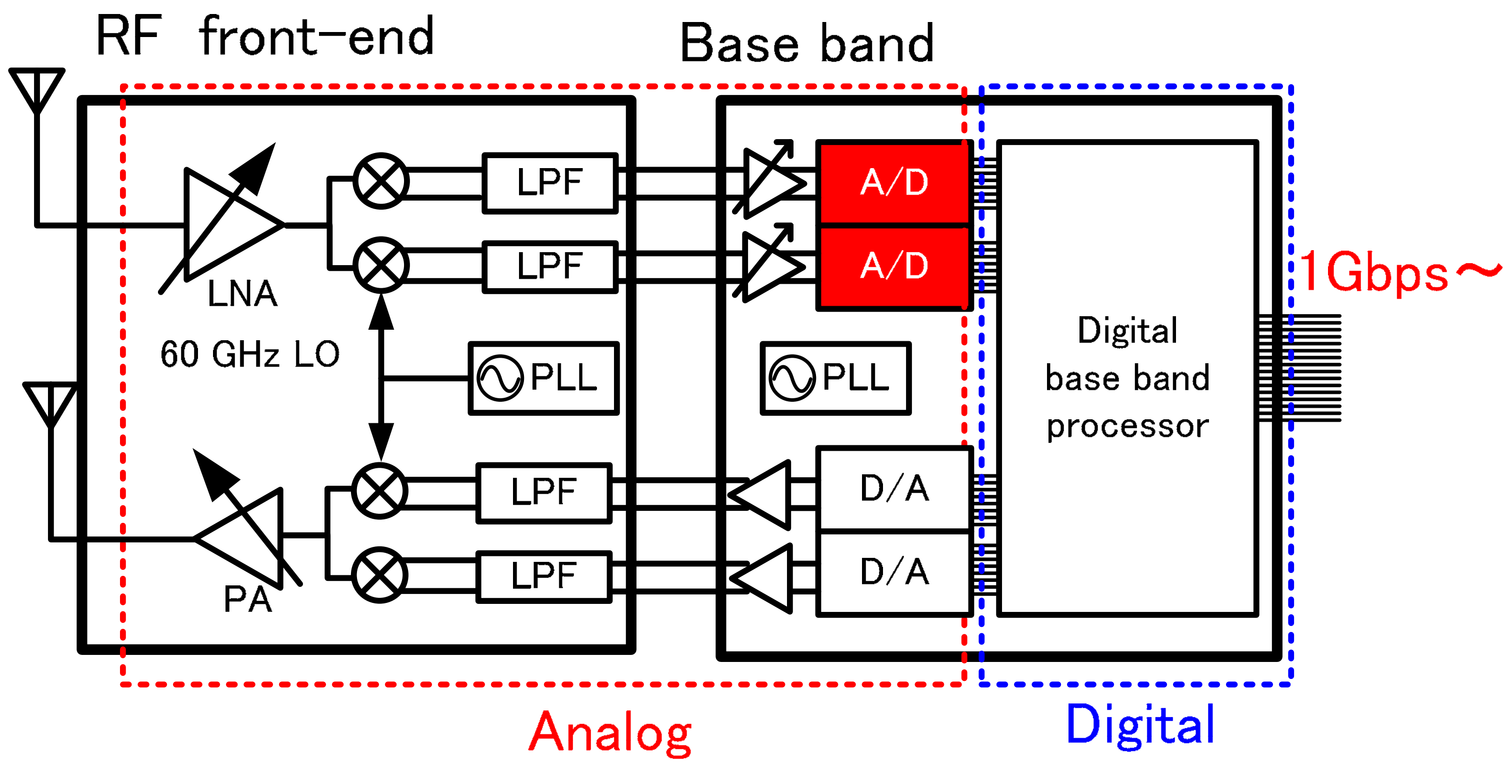
Demands for high speed and low power ADCs

Millimeter wave transceivers, optical or wire line communication systems, high speed data storage systems need high speed ADCs.

For example

Millimeter wave transceiver

5-6bit 3GSps -- 10GSps converters P_d <30mW--50mW



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Recent published high speed CMOS ADCs

- Freq. Flash: 4GS/s, Interleaving: 24GS/s
- FoM: 8pJ→400fJ→50fJ (1GHz, 2mW)
- Area： 4.4mm^2〜0.02mm^2 (Single)

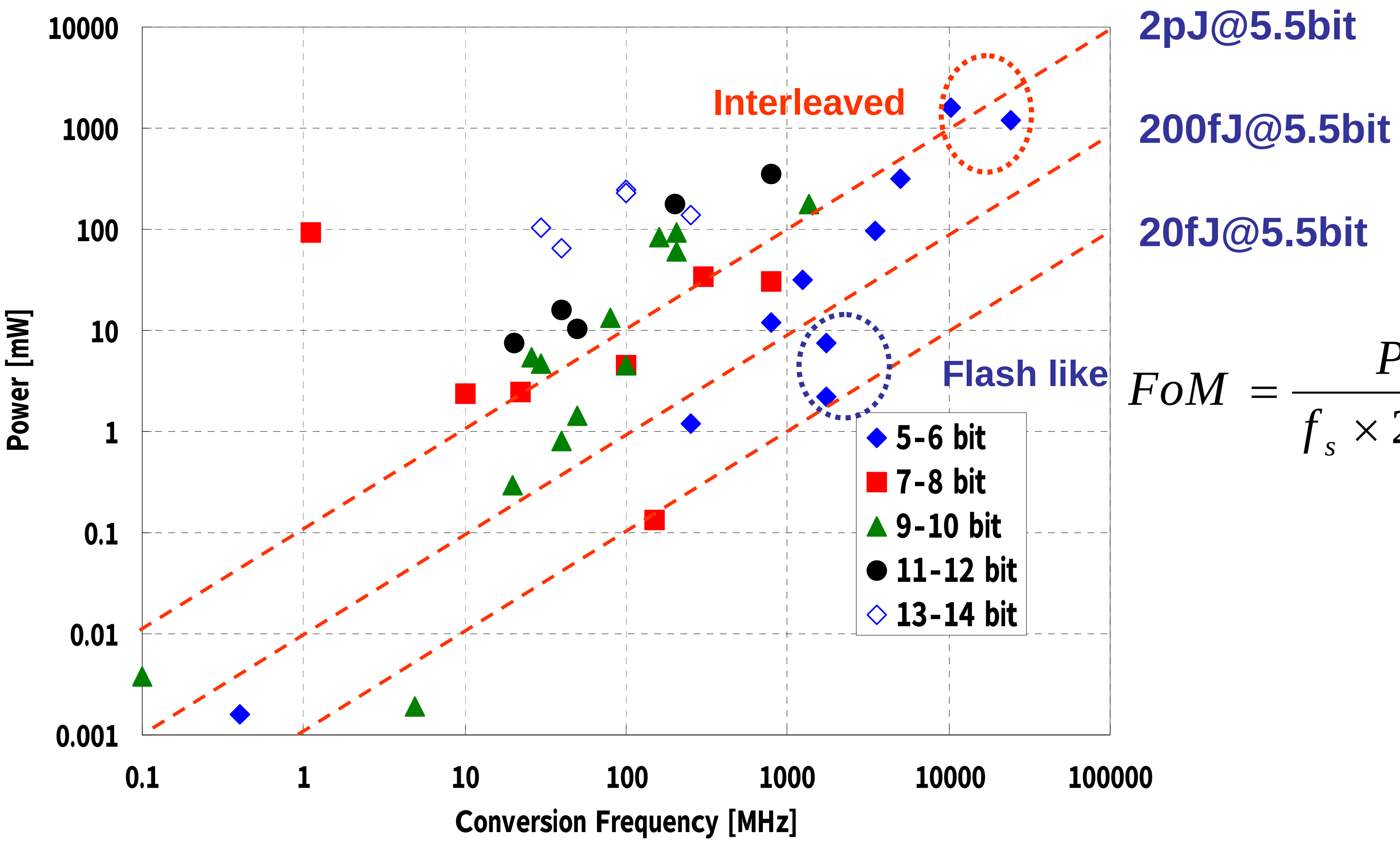
(5bit and 6bit only)

Table 1

No.	Res.	Fs (GS/s)	Pd (mW)	FoM (pJ)	Area (mm^2)	Tech. (nm)	Architecture	Feature	Publish
1	6	4.0	182.0	1.30	0.20	130	Flash	Ref CAL.	ESSCIRC 03
2	6	4.0	990.0	7.73	4.40	130	Flash		VLSI 04
3	5	4.2	180.0	2.80	0.16	130	Flash	Averaging	CICC 2007
4	6	3.5	98.0	0.90	0.15	90	Flash	Averaging	VLSI 07
5	6	1.3	32.0	0.80	0.09	130	2b-SAR	2b	ISSCC 08
6	5	1.8	2.2	0.05	0.02	90	1b_Fold+Flash	R-CAL	ISSCC 08
7	6	24.0	1200.0	2.00	16.00	90	SAR	160x Interleaving	ISSCC 08
8	6	0.8	12.0	0.40	0.13	65	Flash	Ref CAL.	VLSI 08
9	6	5.0	320.0	1.82	0.30	65	Flash	Averasing	VLSI 08
10	6	10.3	1600.0	4.85	?	90	Pipeline	10x Interleaving	VLSI 08
11	5	1.8	7.6	0.15	0.03	90	Flash	R-CAL	VLSI 08
12	6	2.0	170.0	3.80	0.20	130	Flash	Load-CAL	A-SSCC 08
13	6	1.2	75.0	2.17	0.43	130	Flash	Averaging	A-SSCC 08

Conversion speed and power

FoM of 5 and 6 bit Flash ADCs are lowest (100fJ/conv.)
However, FoM of Interleaved ADC is very large (2pJ/conv.)

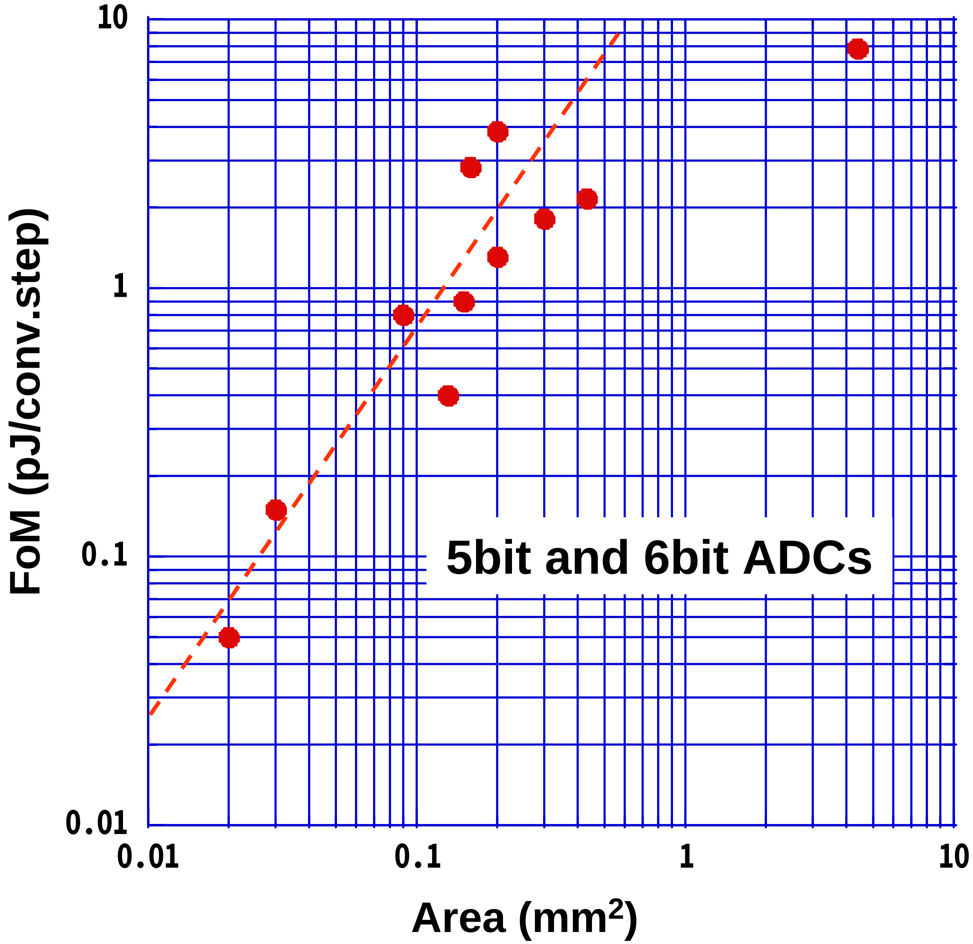


$$FoM = \frac{P_d}{f_s \times 2^{ENOB}}$$

FoM vs. Area

Occupied area should be reduced to lower the FoM.

We must pay much attention to the occupied area.



$$E_c \propto C \propto Area$$

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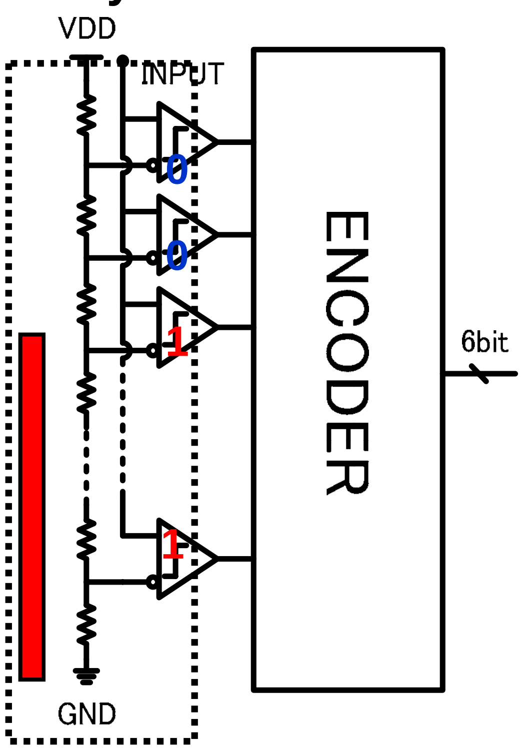
ENOB and FoM of Flash ADCs

Flash ADC architecture

- Expecting highest speed
- Comparator determines the ADC performance

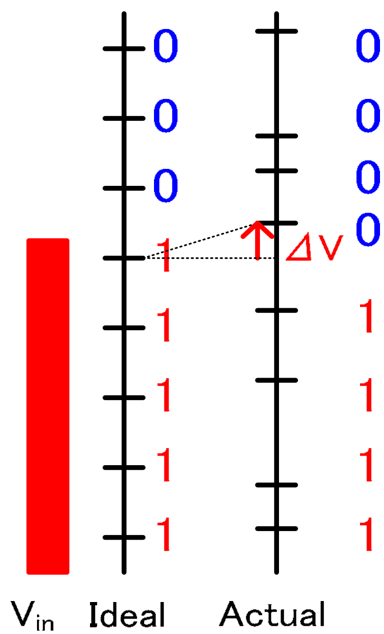
Flash ADC

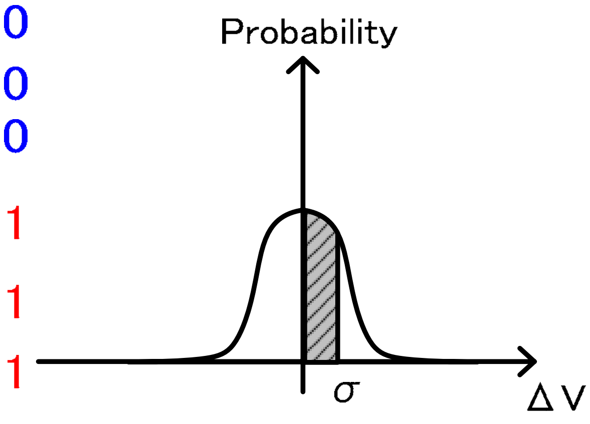
Comparator Array **6b: 63**



$$V_q = \frac{V_{FS}}{2^N}$$

V_q=16mV, Mismatch <3mV

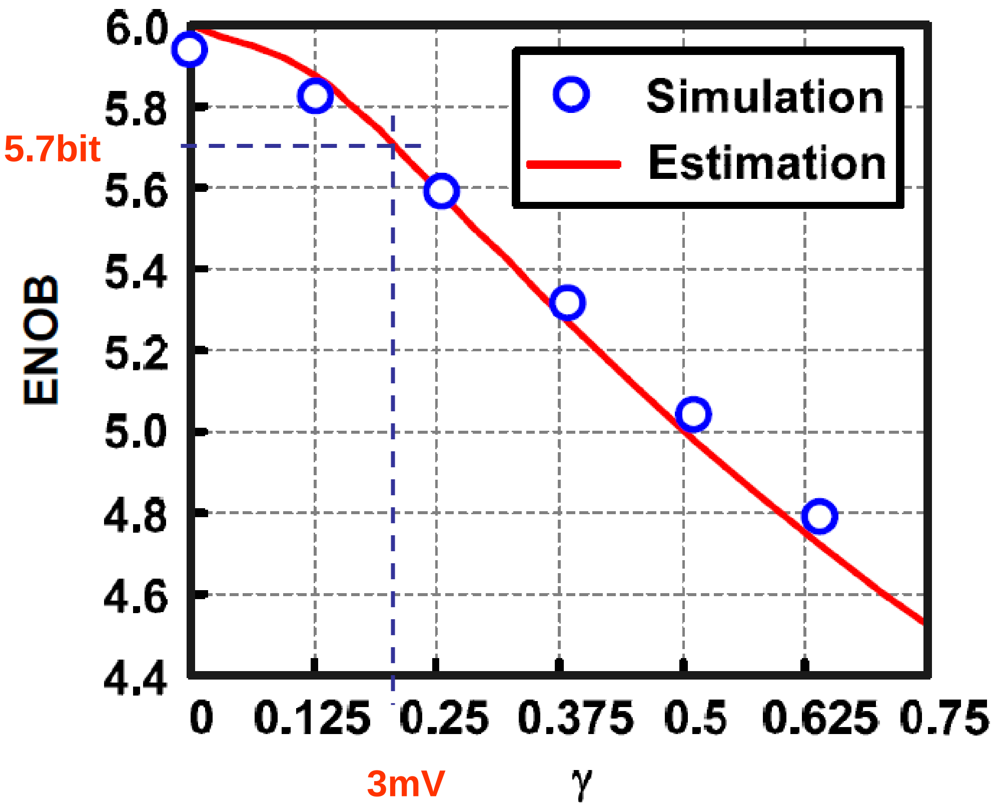




Offset mismatch

Degradation of ENOB

Degradation of ENOB in flash ADC is basically determined by offset mismatch and thermal noise of comparators.



For example; 6bit ADC, ENOB=5.7bit
V_q=16mV, V_{off}<3mV

$$\Delta ENOB = \frac{1}{2}\log_2\left(1+12\gamma^2\right)$$

$$\gamma^2 = \left(\frac{V_{off}(\sigma)}{V_q}\right)^2 + \left(\frac{V_n(\sigma)}{V_q}\right)^2$$

$V_{off}(\sigma)$: *Distribution of offset*

$V_n(\sigma)$: *Distribution of noise*

FoM of Flash ADC

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FoM of flash ADC is determined by energy consumption of unit comparator and the degradation of effective bit.

Reduction of consumed energy and increase of ENOB are very important

$$FoM = \frac{P_d}{f_s \times 2^{ENOB}} \approx \frac{E_c \cdot f_s \cdot 2^N}{f_s \times 2^{N-\Delta ENOB}} = E_c \cdot 2^{\Delta ENOB}$$

E_c: Energy/Comparator

$$E_c = CV_{DD}^2$$

E_c is basically proportional to the capacitance

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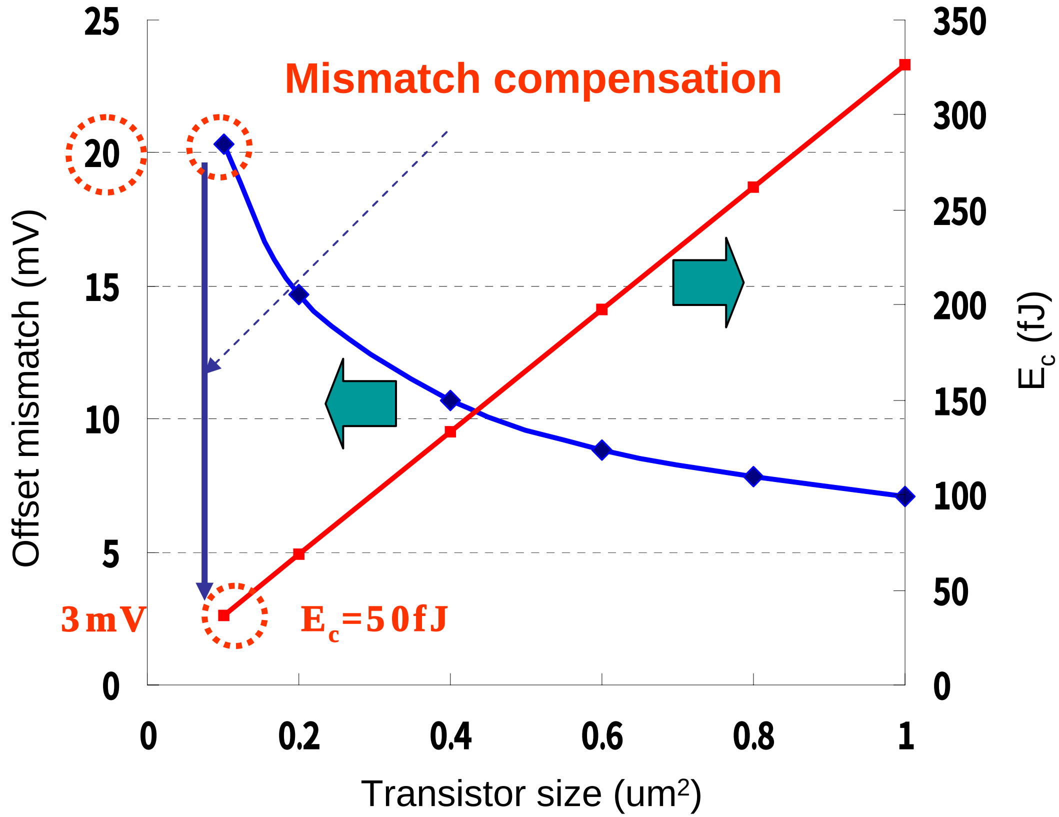
Tradeoff: mismatch and energy consumption

There is a serious tradeoff between mismatch of transistor and gate area.

Larger transistor is required to reduce mismatch voltage
and results in increase of gate area and consumed power.



Example

6bit ADC: V_{off}<3mV
E_C<50fJ→0.1um^2→V_{off}=20mV
Needs mismatch compensation
20mV →3mV

$$V_{offset}(\sigma) \propto \frac{1}{\sqrt{LW}}$$

$$E_c \propto C_c \propto LW$$

$$E_c \propto \frac{1}{V_{offset}^2(\sigma)}$$

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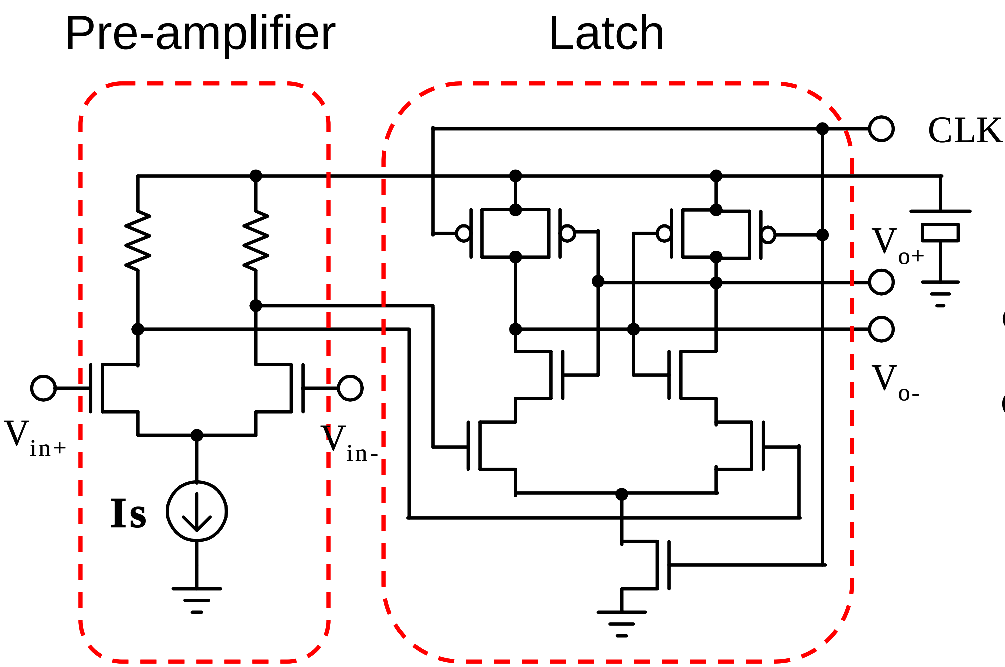
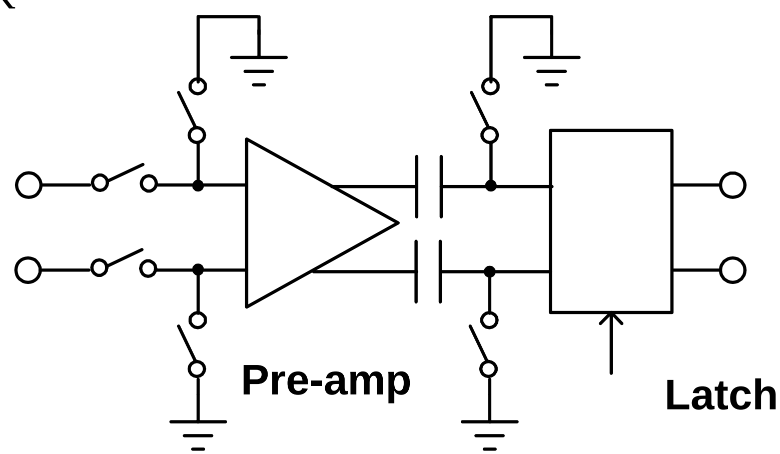
Mismatch compensation and noise of dynamic comparators

Conventional comparator

A conventional comparator flows static current.
It is not suitable for ultimate low power ADCs.
Also, analog offset cancelling technique can't be used in dynamic comparators.



Offset cancelled comparator

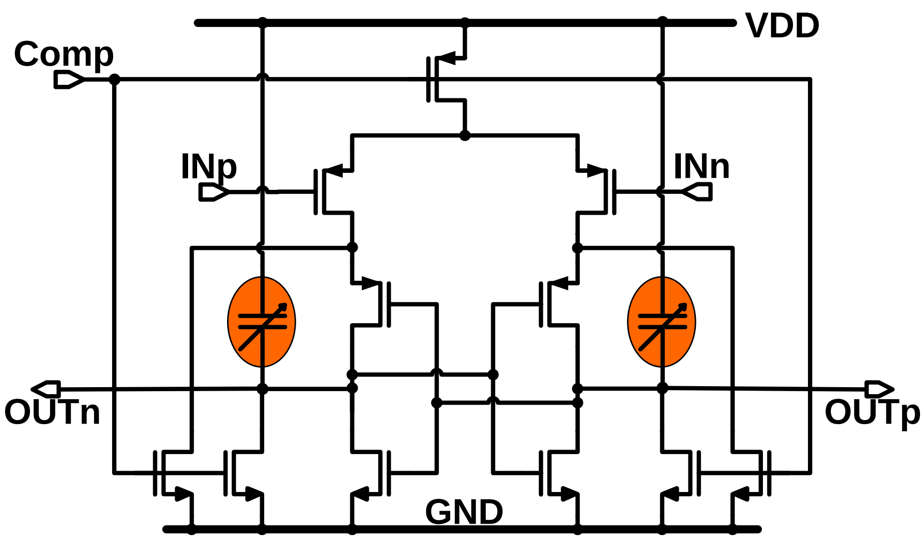


Static current flows
Limited power reduction

This offset cancelling technique
Can't be used in dynamic comparators

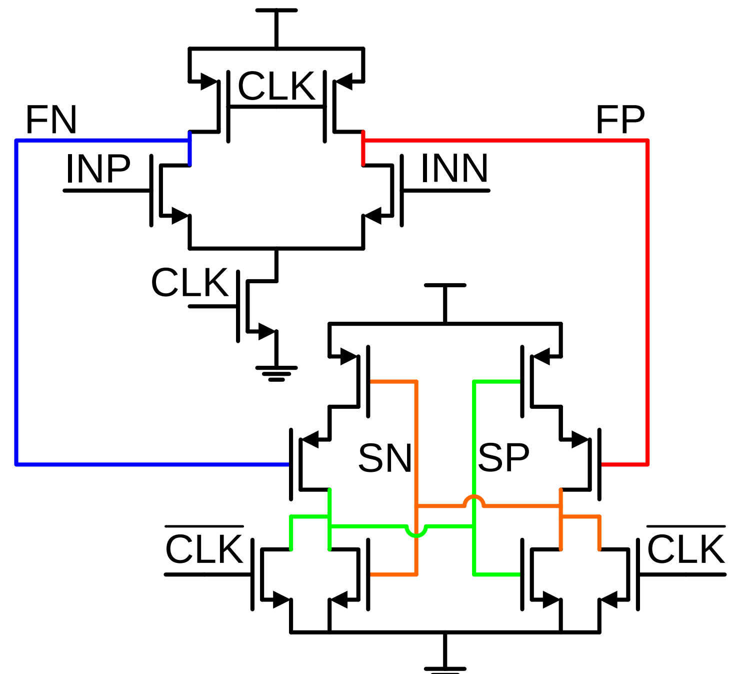
Direction of comparator circuits

Dynamic comparators use the fast voltage falls depended on input voltage difference and consumes no static power, however afraid of large mismatch voltage.



V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, “An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

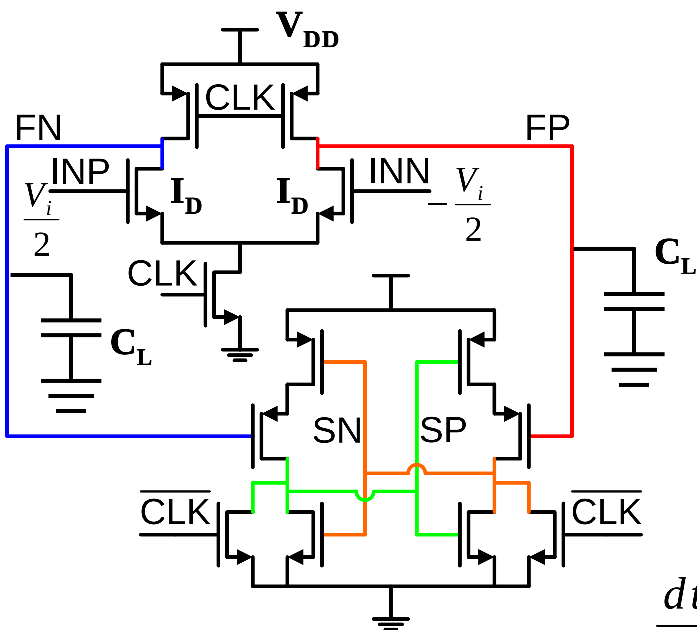
Double-tail latch comparator



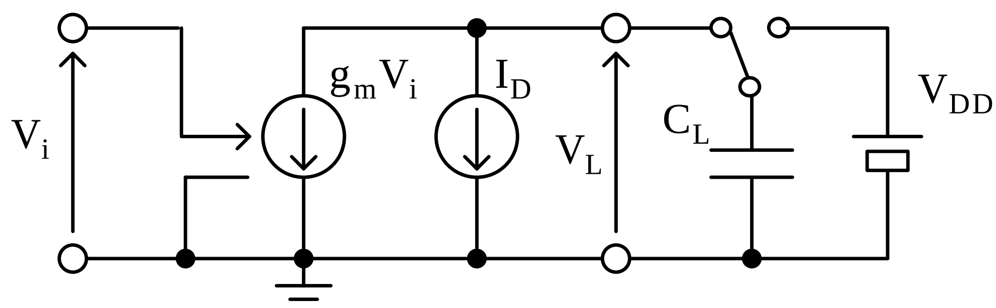
M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, “A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Mismatch compensation method

The mismatch can be compensated by capacitance and current.



Equivalent circuit of the first stage.

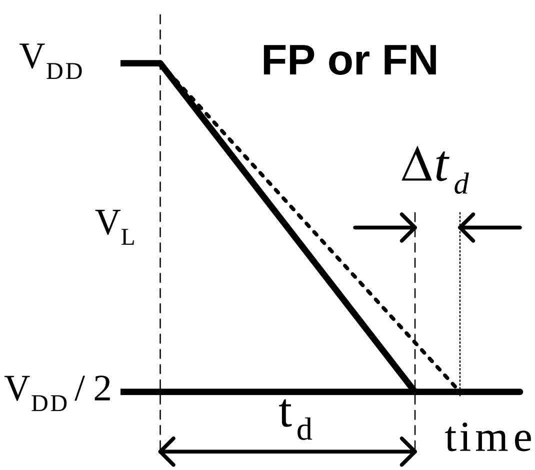


Delay time $t_d = \dfrac{V_{DD} C_L}{2 I_D}$

$$I_D \propto \left(V_{gs} - V_T\right)^{\alpha} = V_{eff}^{\alpha}$$

$$g_m = \frac{dI_D}{V_{eff}} = \alpha \frac{I_D}{V_{eff}}$$

$$\frac{dt_d}{dV_i} = \frac{dt_d}{dI_D} \cdot \frac{dI_D}{dV_i} = -\frac{V_{DD} C_L}{2 I_D} \frac{g_m}{I_D} = -t_d \frac{\alpha}{V_{eff}} \qquad \therefore \frac{g_m}{I_D} = \frac{\alpha}{V_{eff}}$$



$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}} \qquad \frac{\Delta t_d}{t_d} = \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D}\right)$$

$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}} \qquad \boxed{\Delta V_i = \frac{V_{eff}}{\alpha}\left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D}\right)}$$

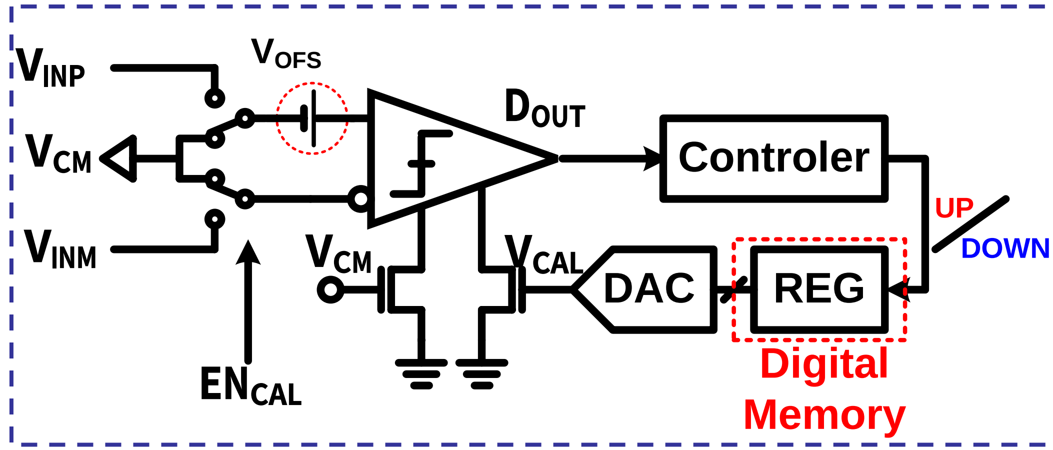
Memory for mismatch compensation

There are two memory types for mismatch compensation.

Digital memory type

Pros. No need of refresh

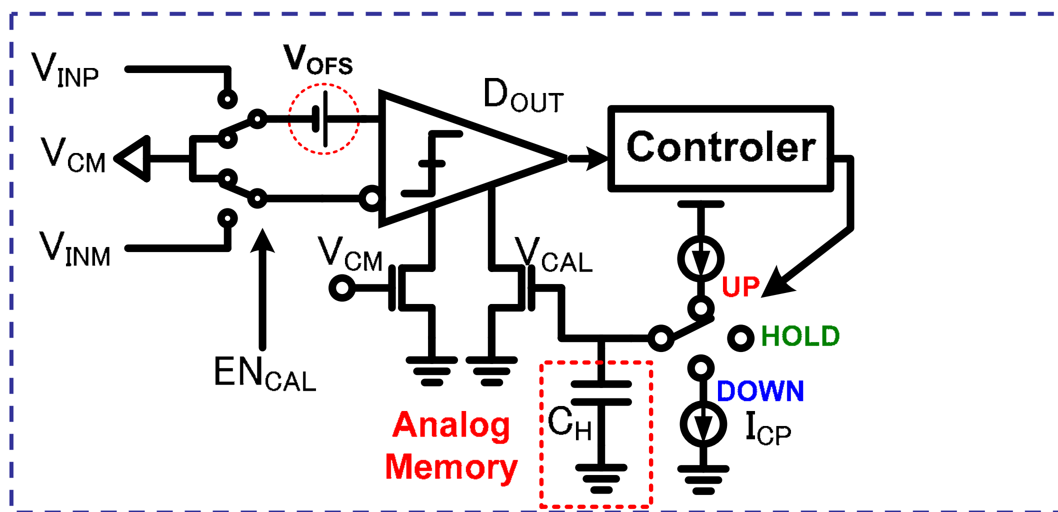
Cons. Limited resolution



Analog memory type

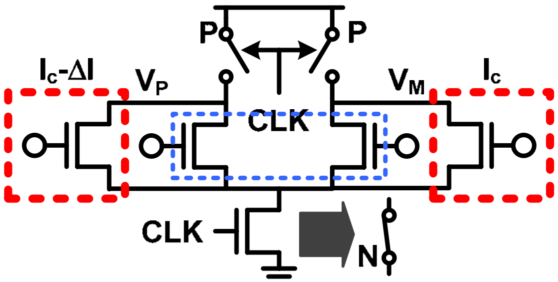
Pros. High resolution

Cons. Needs refresh



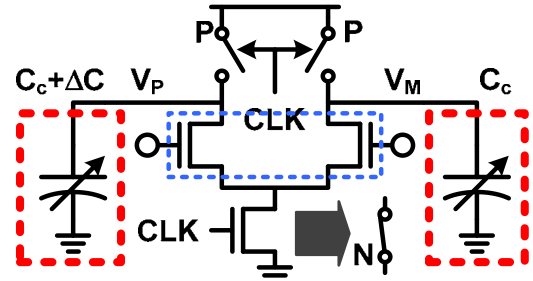
Digital memory type

Resistor ladder type

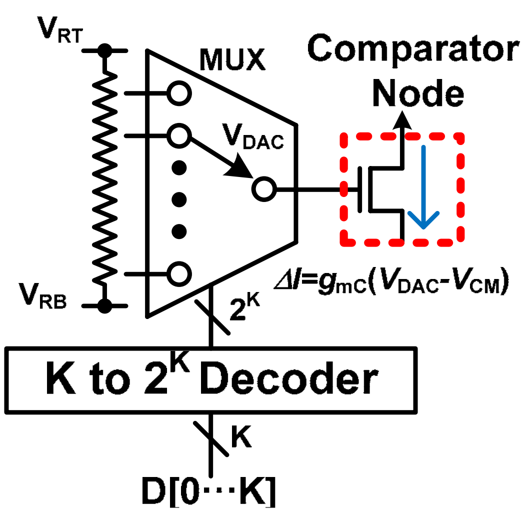


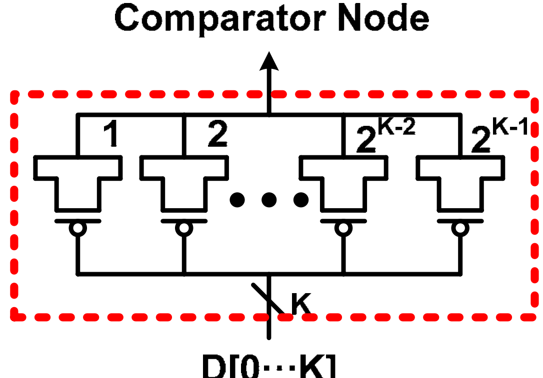
Current calibration

Capacitor array type



Capacitance calibration





Binary weighted capacitor array

Analog memory type

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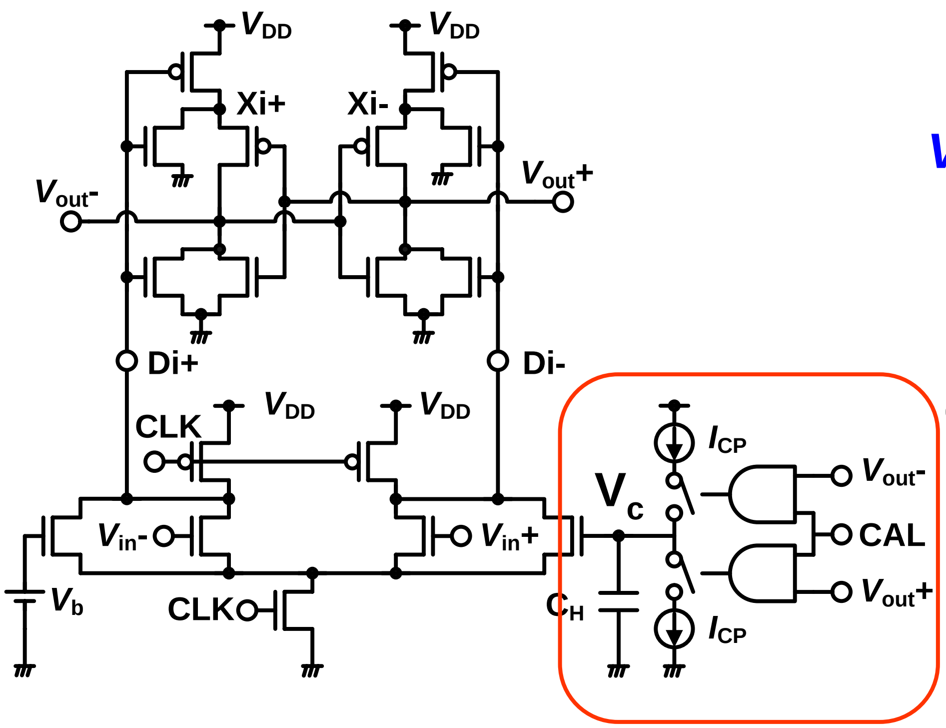
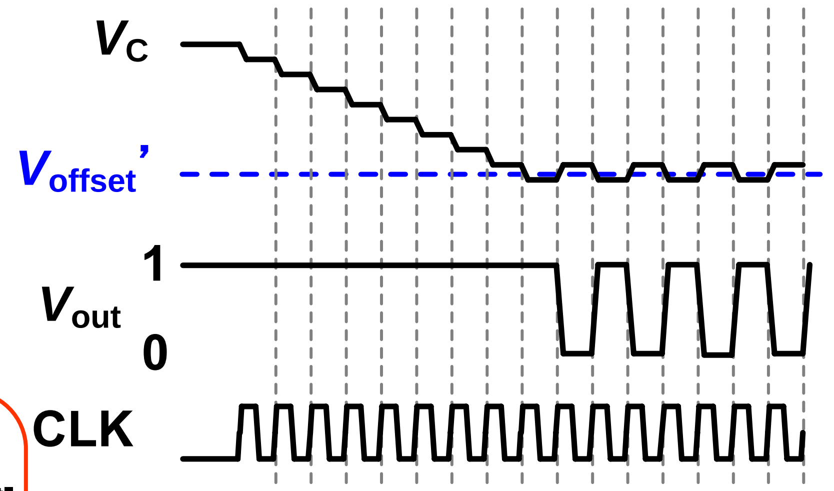
We developed analog memory type mismatch compensation, by using charge pump circuits.



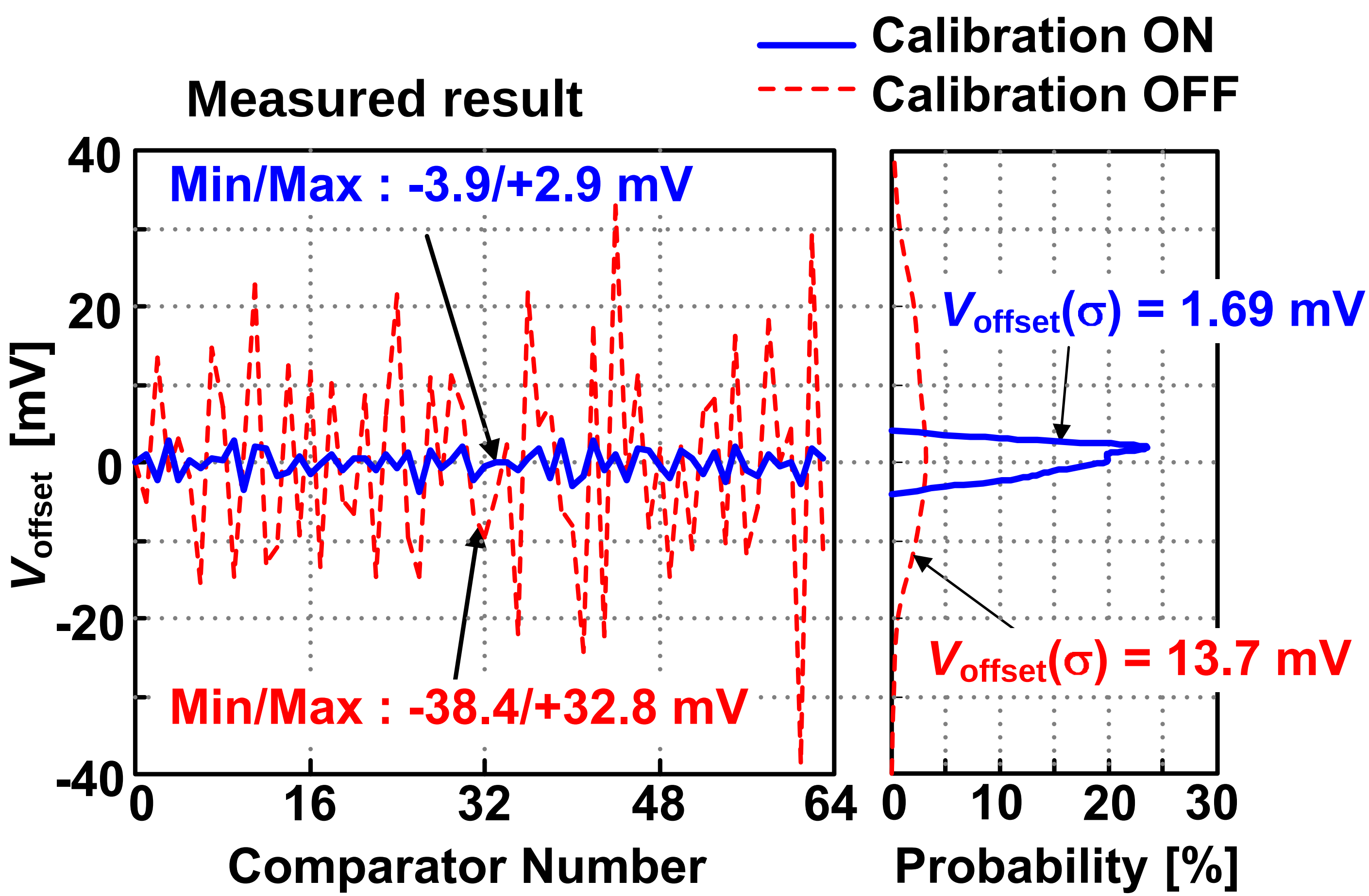


M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Matsuzawa & Okada Lab.

Effect of analog mismatch compensation

We can reduce the mismatch voltage form 14mV to 1.7mV at sigma.

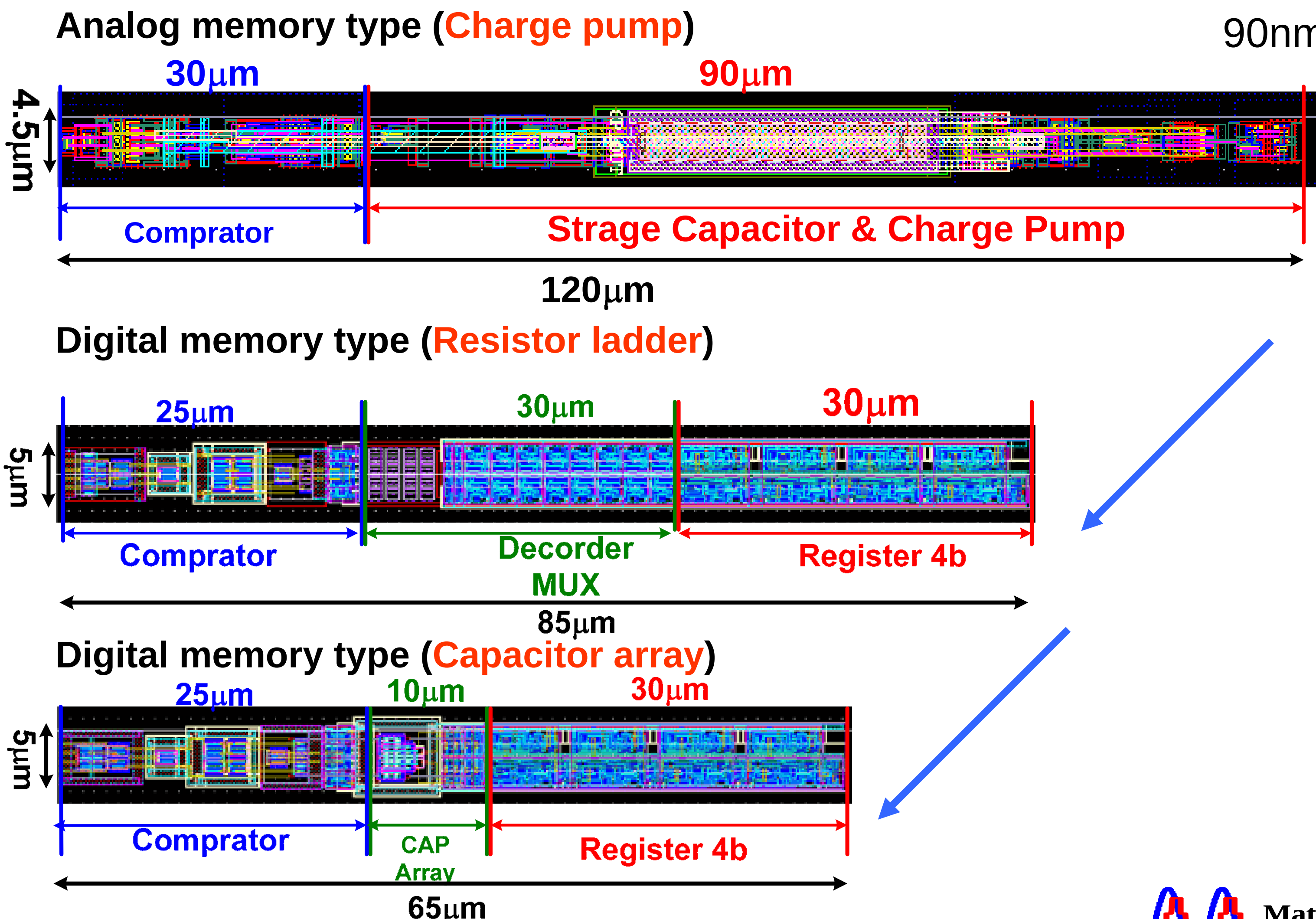


M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Area comparison

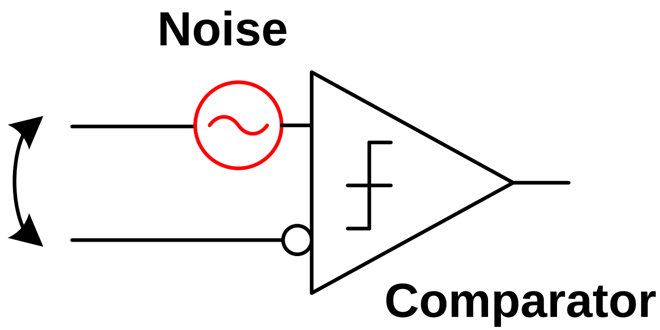
Capacitor array type looks smaller.

90nm CMOS



Noise in comparator

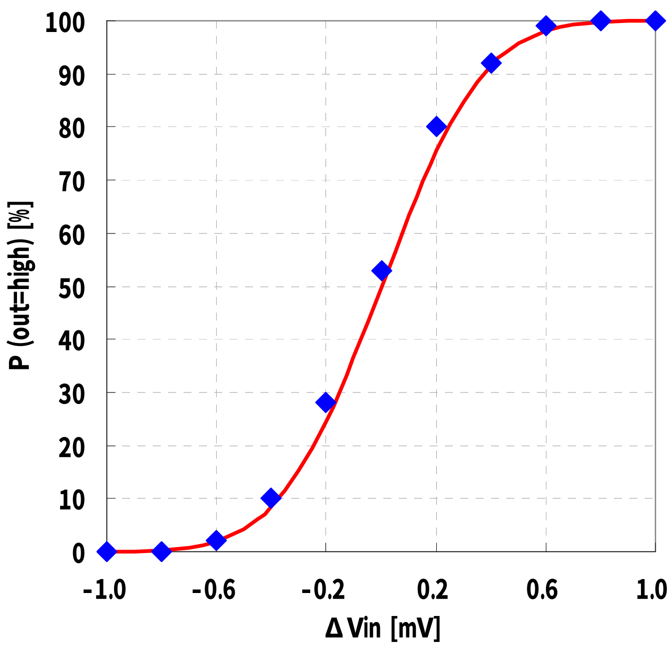
Comparator has noise and it reduces ENOB.



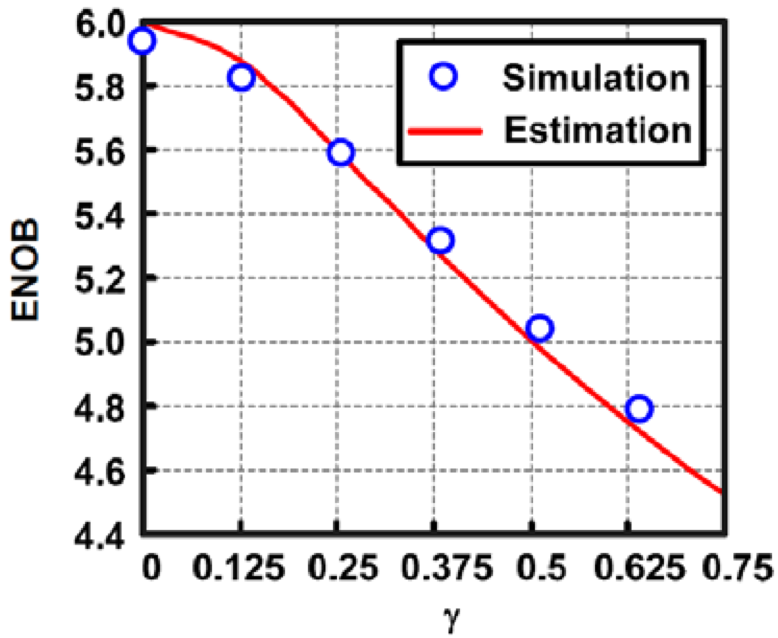
$$ENOB = N - \frac{1}{2}\log_2\left(1 + 12\gamma^2\right)$$

$$\gamma = \frac{V_n(\sigma)}{V_q}$$

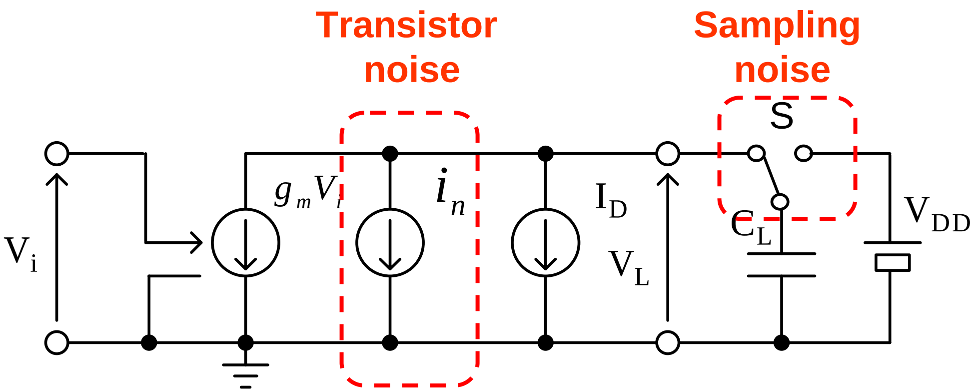
Probability of output code



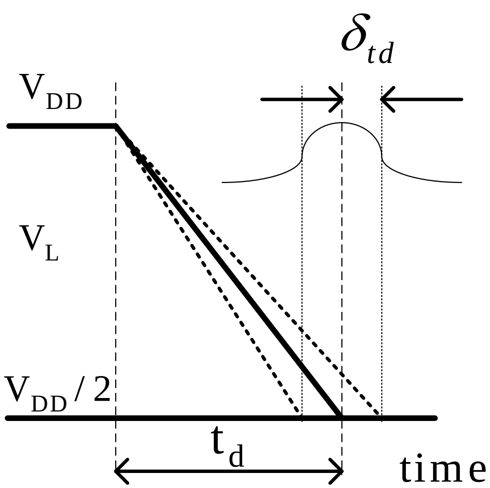
$$ENOB\ vs.\ \gamma$$



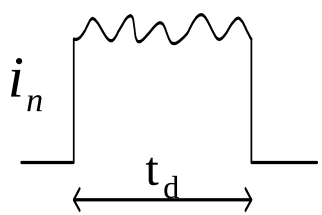
Deducing noise equation



Equivalent circuit



Voltage and timing



TR noise

1) Sampling noise of Switch

$$\langle v_n^2 \rangle = \frac{kT}{C_L}, \quad \delta_{t_d}^2 = \frac{\langle v_n^2 \rangle}{\left(\frac{I_D}{C_L}\right)^2} = \frac{kTC_L}{I_D^2}$$

Timing fluctuation

2) Transistor noise

$$\delta t = \frac{C_L}{I_D} \delta v$$

Noise voltage of output by current noise

$$v_n = \frac{1}{C_L} \int_0^{t_d} i_n dt \qquad \delta_{t_d}^2 = \frac{C_L^2}{I_D^2} \delta_{vn}^2 = \frac{1}{I_D^2} \left\langle \left(\int_0^{t_d} i_n dt \right)^2 \right\rangle$$

$$\left\langle \left(\int_0^{t_d} i_n dt \right)^2 \right\rangle = 2 t_d \gamma k T g_m \qquad \therefore \delta_{t_d}^2 = \frac{2t_d}{I_D^2} \gamma k T g_m$$

$$I_D \propto \left(V_{gs} - V_T\right)^{\alpha} \qquad g_m = \alpha \frac{I_D}{V_{eff}}$$

$$\therefore \delta_{t_d}^2 = \frac{2kT\alpha\gamma}{I_D V_{eff}} t_d = \frac{kTC_L \alpha\gamma V_{DD}}{I_D^2 V_{eff}} \quad \because t_d = \frac{C_L V_{DD}}{2 I_D}$$

Deduced noise equation

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$$\delta V_{in}^{2} = \frac{4kTV_{eff}^{2}}{\alpha^{2} C_{L} V_{DD}^{2}} \left(\alpha\gamma \frac{V_{DD}}{V_{eff}} + 1 \right) \approx \frac{4kTV_{eff}}{\alpha C_{L} V_{DD}}$$

1) Sampling noise $\delta_{t_d}^{2} = \frac{kTC_L}{I_D^2}$

2) Transistor noise $\delta_{t_d}^{2} = \frac{kTC_L \alpha\gamma V_{DD}}{I_D^2 V_{eff}}$

Delay fluctuation by noises

$$\delta_{t_d}^{2} = \frac{kTC_L}{I_{ds}^2} \left(\alpha\gamma \frac{V_{dd}}{V_{eff}} + 1 \right)$$

$I_{ds} \propto V_{eff}^{\alpha}, \quad 1 < \alpha < 2$

$\gamma : noise\ factor$

Input referred input voltage fluctuation

$$\frac{\delta_{t_d}}{t_d} = \frac{\delta_{I_D}}{I_D} = \frac{V_{in} g_m}{I_D} \qquad \therefore V_{in} = \frac{\delta_{t_d}}{t_d} \frac{I_D}{g_m} \qquad \because t_d = \frac{C_L V_{DD}}{2 I_D}$$

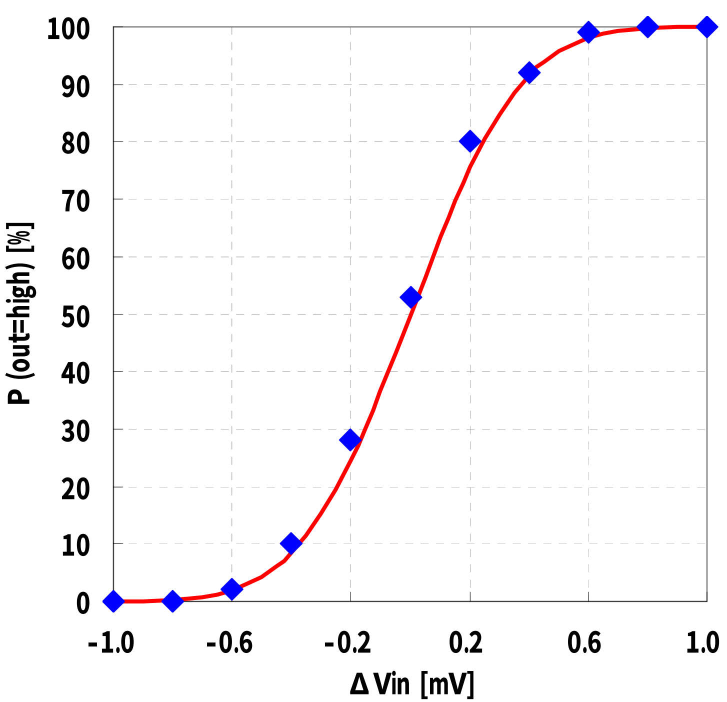
$$\delta V_{in}^{2} = \left(\frac{V_{eff}}{\alpha} \frac{\delta_{td}}{t_d} \right)^2 = \left(\frac{V_{eff}}{\alpha t_d} \right)^2 \frac{kTC_L}{I_{ds}^2} \left(\gamma \frac{V_{dd}}{V_{eff}} + 1 \right) = \frac{4kTV_{eff}^{2}}{\alpha^2 C_L V_{dd}^2} \left(\alpha\gamma \frac{V_{dd}}{V_{eff}} + 1 \right)$$

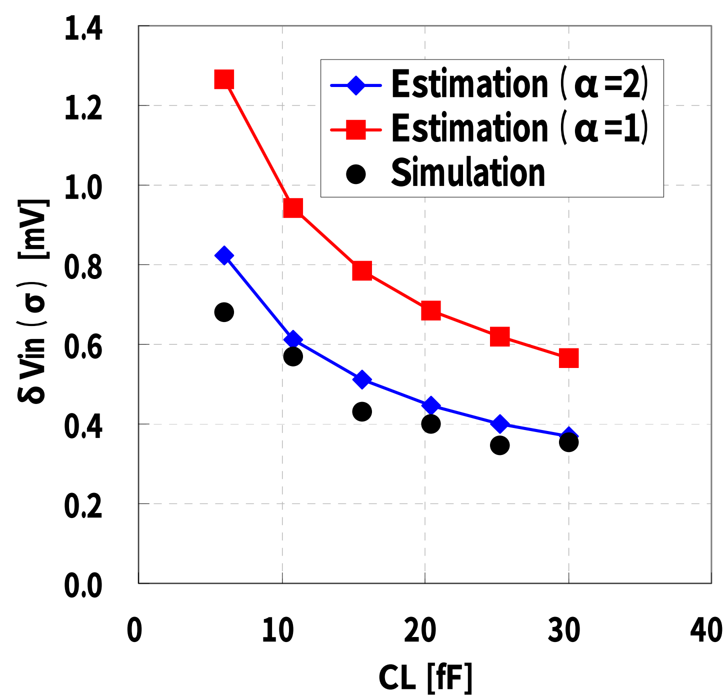
Match with noise simulation

The deduced equation has a good match with simulation.

Increase of node capacitances and decrease of effective gate voltage are required to reduce comparator noise.

$$\delta V_{in} \approx 2\sqrt{\frac{kTV_{eff}}{\alpha C_L V_{DD}}}$$

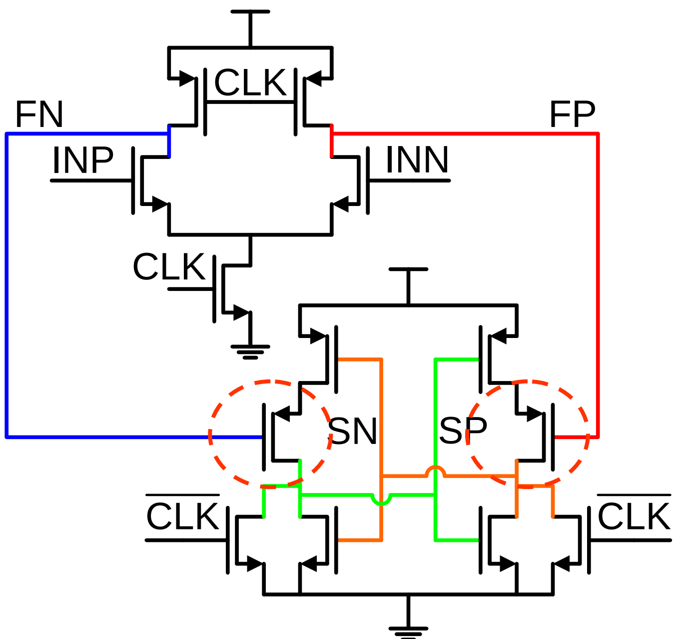




Comparison of comparators

Double clock

NMOS Single gm

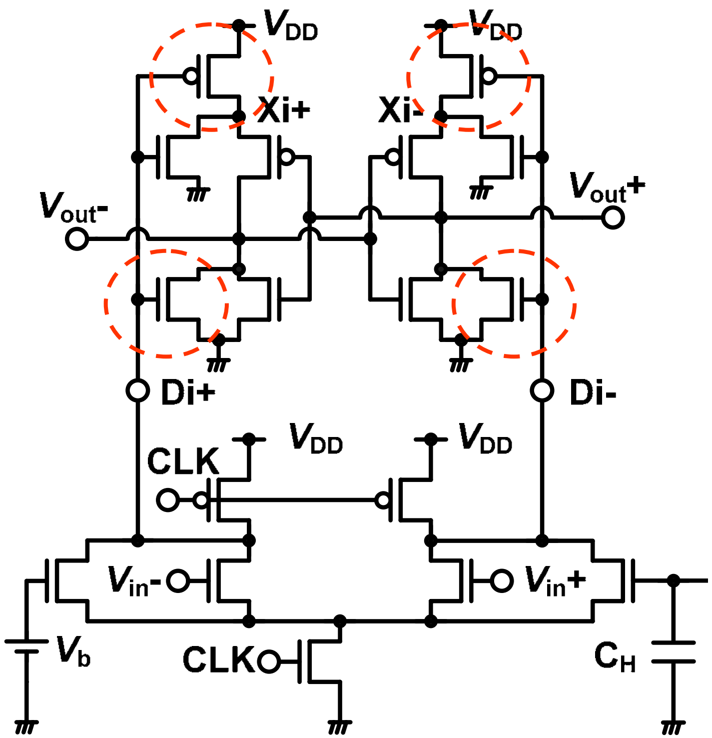


Conventional

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, “A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Single clock

NMOS+PMOS Double gm



Our proposed

M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

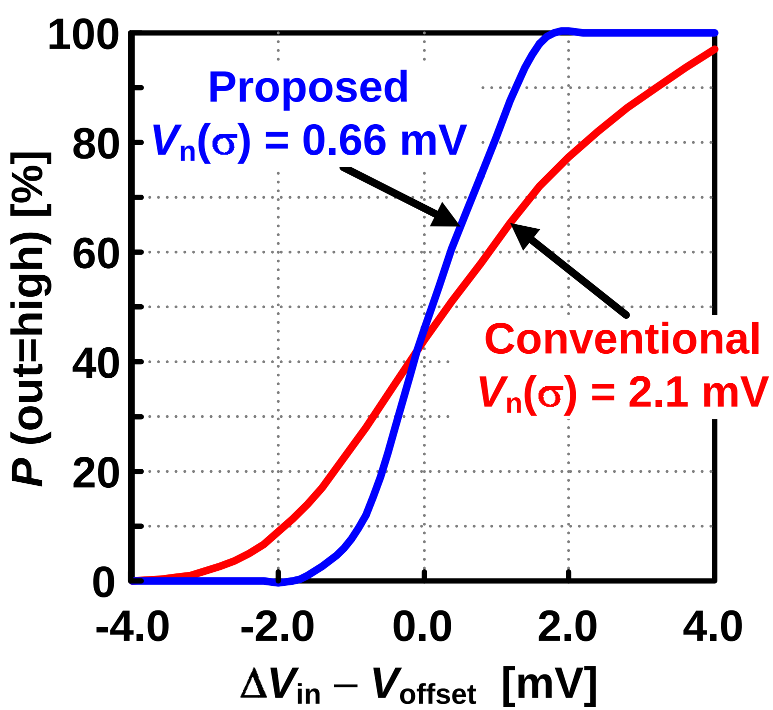
Noise reduction of comparator

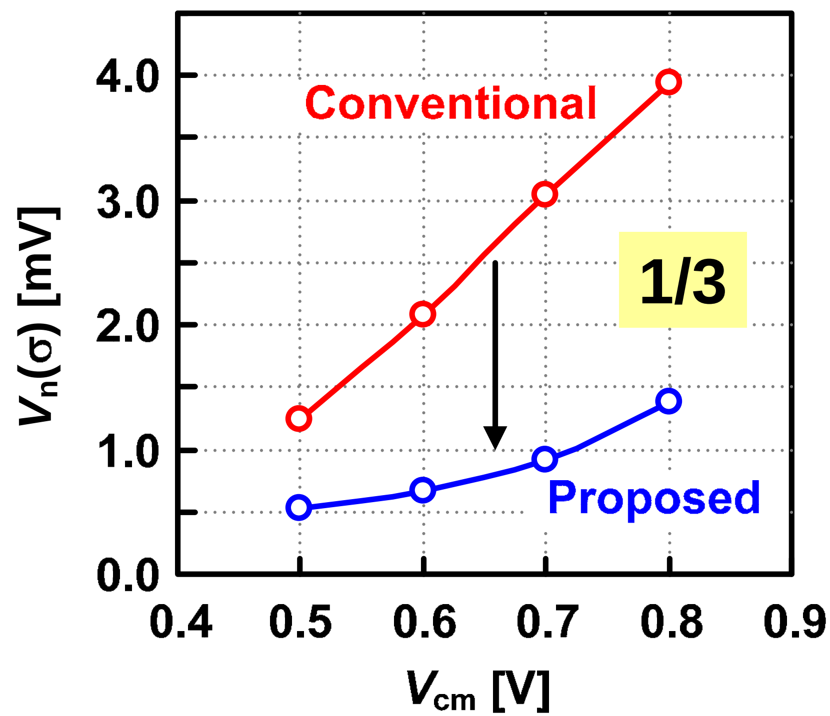
Proposed double-tail latch comparator can reduce noise down to 1/3.

V_{DD} = 1.0 V, Fc = 4 GHz, Transient-Noise simulations.
(Offset calibration is not used.)

M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

@V_{cm} = 0.6 V

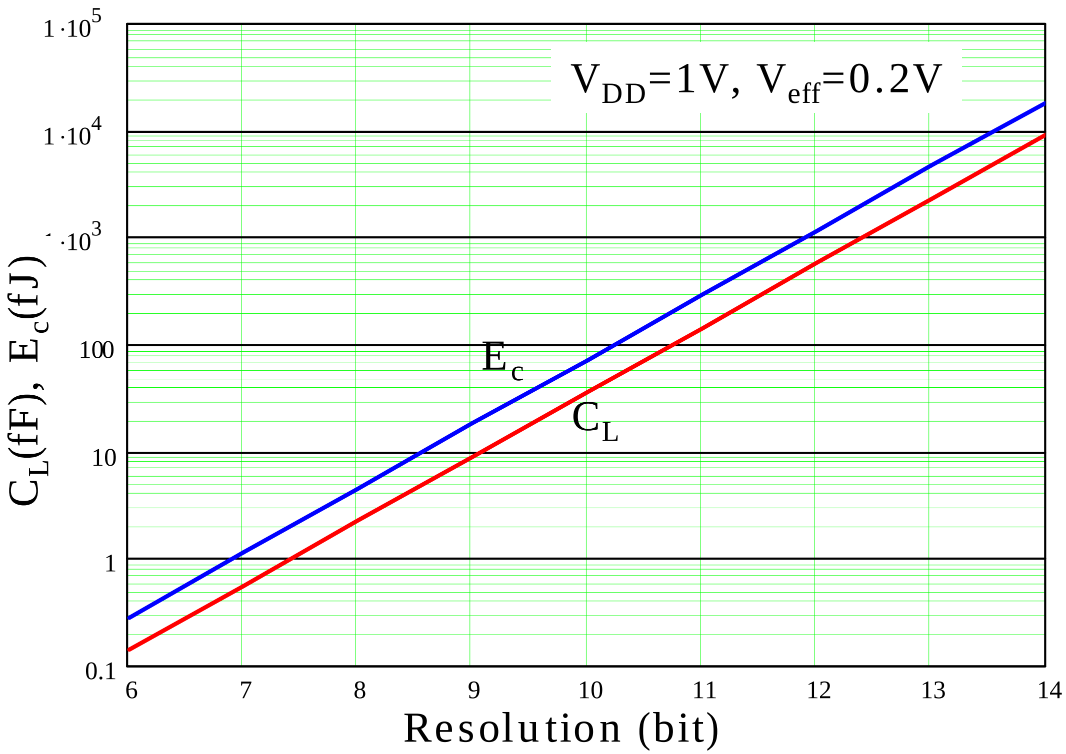




Required capacitance and consumed Energy

Node capacitances should be increased to realize higher ADC resolution.
This results in increase of consumed energy of comparator.

Flash ADC: **Ec determines the minimum FoM**
SAR ADC: **Ec will not be neglected for higher resolution ADC**



2fF & 4fJ @8bit
40fF & 80fJ @10bit
0.6pF & 1pJ @12bit
10pF & 20pJ @14bit

Summary

- Many high seed ADCs have been developed to realize several Gbps communication systems, however FoMs spread widely.
- The FoM has a strong relationship with occupied area.
- To reduce FoM of flash ADC, transistor size and occupied area should be reduced as much as possible.
- The ENOB is mainly determined by offset mismatch and noise of comparator.
- A dynamic comparator is suitable for ultimate low power ADCs.
- Mismatch compensation techniques are vital for use of small MOS transistor and the capacitor array type looks reasonable.
- Noise equation of the double-tail latched comparator has been deduced and node capacitances should be increased to realize higher ADC resolution. However this increases energy consumption.

References of Table 1 (1/2)

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