バラクタと DAC を用いたデジタル制御発振器の検討
A Comparison between Varactor-DAC and Capacitor-Bank DCOs

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1. Introduction

All Digital PLL (ADPLL) posses many advantages over the conventional Charge Pump PLL (CPPLL). These advantages make doing research on them more appealing these days to overcome the challenges in their design. One of the main components of an ADPLL that plays an important role in the overall performance is Digitally Controlled Oscillator (DCO). The DCO layout area and fine-tuning are some of the main aspects that need to be carefully considered and improved. The large layout area is mainly due to the large number of capacitors needed for fine-tuning of the DCO [1]. Achieving a minimum step in the tuning of the DCO can be done by dithering very small capacitors to get a more fine frequency tuning [2]. In this paper, a comparison between fine-tuning the DCO using a capacitor-bank and a varactor-DAC approach are compared and studied.

2. Varactor-DAC *vs* capacitor-bank DCOs

A DCO can be fine-tuned using small-switched capacitor banks or using a varactor-DAC as shown in Fig. 1. A comparison between two structures was made by using a 0.18μm CMOS process. The varactors are connected to a 6-bit R/2R ladder DAC as shown in Fig. 2. The capacitor-bank was constructed using Metal-Insulator-Metal (MIM) capacitors with a transistor as a switch. To obtain smaller capacitance values, MIM capacitors are connected in series due to capacitance size limitation in the process used. Both structures are matched in terms of capacitance range and are connected to an LC oscillator circuit for comparison. The comparison results are shown in Table 1. Looking at the results it can be seen that using a capacitor-bank to fine-tune the DCO results in a very small improvement in the phase noise and the FOM compared to the varactor-DAC configuration. This is mainly due to a slightly higher resistance seen from simulation across the varactor-DAC terminals together with the noise of about 0.34dB added by the DAC. However, the slight improvement in the phase noise and FOM is paid off with a considerable increase in the layout area. The layout area of a capacitor-bank is about 2.75 times larger then the one for the varactor-DAC. If many switched capacitor-banks are used, which is the case in regular DCO [1], they will lead to a considerable area increase. On the other hand, using the varactor-DAC configuration would save a lot of area on the chip. In addition, increasing the resolution of the DCO tuning only requires the addition of two resistors for each 1-bit increase in the resolution. The limitation of the resolution of the DCO in the case of using a capacitor-bank configuration is bounded by the parasitic capacitance of the transistor switch and interconnects. In the varactor-DAC configuration, the limitation of the resolution is bounded by the degree of mismatch in the resistor values that would result in an error in the output voltage of the DAC. Calibration is needed for both configurations to minimize the effects of the process variation mismatch and to improve performance.

3. Conclusion

DCO fine-tuning can be done using capacitor-bank or varactor-DAC. A capacitor-bank can provide slightly better phase noise performance but at the expense of a larger area. A varactor-DAC is not as good as a capacitor-bank in terms of phase noise but saves a considerable amount of layout area.

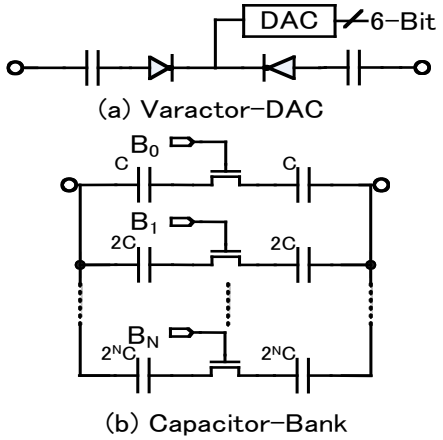

Fig. 1. Fine-tune DCO configurations

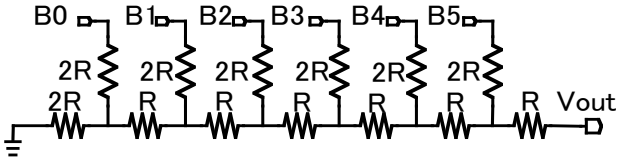

Fig. 2. R/2R ladder DAC.

Table 1. Varactor-DAC Capacitor-Bank Comparison results

	Capacitor-Bank	Varactor-DAC
Process	CMOS 0.18μm	CMOS 0.18μm
Frequency (GHz)	6.01	5.93
Tuning Range (MHz)	470	430
PN@1 MHz (dBc/Hz)	118.5	117
FOM	182	181
Minimum Step (MHz)	4.7	4.4
Area (mm^2)	0.02587	0.00938
Current (mA)	9	8

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References

[1] R. B. Staszewski, *et al.*, IEEE J. Solid-State Circuits vol. 39, pp. 2278–2291, Dec. 2004.
[2] Win Chaivipas, *et al*.,A-SSCC, pp 424-427, Nov. 2007.