Noise Effects Caused by Settling Time Optimization in Switched-Capacitor Circuit

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1 Introduction

Thermal noise represents a major limitation on the performance of most electronic circuits, particularly important in switched-capacitor circuits. In these circuits, the settling time can be improved by optimizing on-resistance of the switch in the feedback path [1]. The purpose of this paper is to present noise effects caused by this settling time optimization method.

2 Settling Time Optimization

Using the model shown in Fig. 1, the settling time of the switched capapacitor amplifier can be reduced by choosing switch resistance as shown in [1]

$$r_{\mathrm{fopt}} = m r_{\mathrm{s}} + \frac{(m+1)}{g_{\mathrm{m}}}. \qquad (1)$$

Fig. 2 shows the step response of the single-stage amplifier as a function of time for $r_{\mathrm{f}} = 200\Omega$ and $r_{\mathrm{f}} = 400\Omega$. The step response in case of $r_{\mathrm{f}} = 400\Omega$ is faster than $r_{\mathrm{f}} = 200\Omega$. Other parameters are listed below in Table 1.

Table 1　Model parameters

r_{s}	g_{m}	m	C_{L}	C_{pi}	C_0
200Ω	10mS	1	1.3pF	100fF	2.0pF

3 Noise effects in a switched-capacitor amplifier

Assuming that the op-amp is properly compensated, the closed-loop transfer fuction can be approximated by the one-pole expression and the output noise may be calculated as follows:

$$\overline{v_{\mathrm{out}}^2} = \int_0^{\infty} \left(\overline{v_{\mathrm{in}}^2}\right) \left(\frac{G_0}{1+s\tau}\right)^2 df = \left(\overline{v_{\mathrm{in}}^2}\right) \left(\frac{G_0}{4\tau}\right) \qquad (2)$$

where G_0 is the dc gain of the stage, $\overline{v_{\mathrm{in}}^2}$ is the input noise, and τ is its settling time constant. Here, smaller settling time produces more noise. As shown in Fig. 3, the output SNR of multiply-by-two circuit with 400 $\mathrm{mV_{p-p}}$ sine wave input decreased 2dB when using optimum on-resistance switch.

4 Conclusion

The noise increase caused by settling time optimization in a switched-capacitor amplifier was investigated. Pole-zero cancellation can be used to reduce the settling time effectively, however it increases total noise. A suggested practical solution is to choose an available settling time with the lowest switch on-resistance.

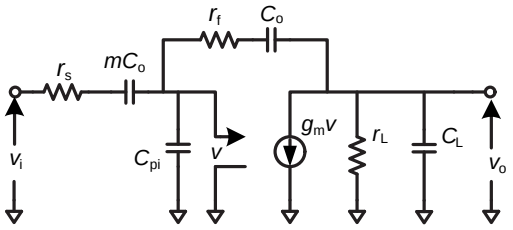

Fig 1　Single-stage amplifier model used for analysis

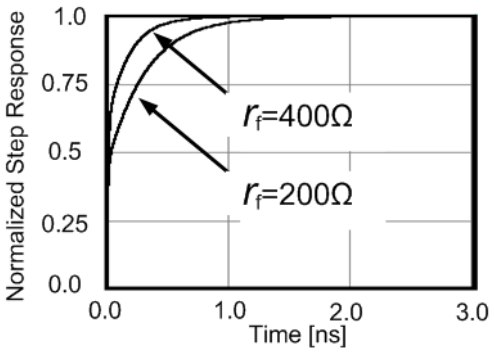

Fig 2　Step response of the single-stage amplifier

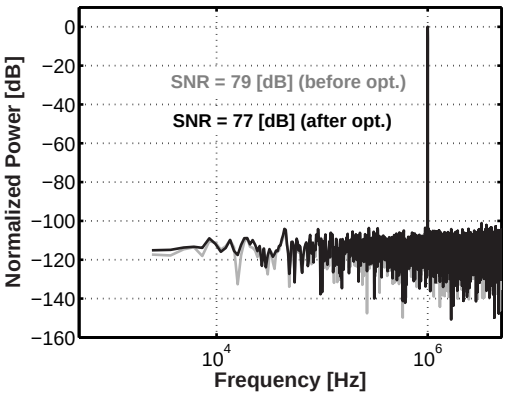

Fig 3　Noise increase caused by settling time optimization

Acknowledgements

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References

[1] M. Miyahara and A. Matsuzawa, “The effects of switch resistances on pipelined adc performances and the optimization for the settling time,” *IEICE Trans. Electron., vol.E90-C, no.6,* pp. 1165–1171, June 2007.