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A 0.027-mm^2 Self-Calibrating Successive Approximation ADC Core in 0.18-μm CMOS

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SUMMARY We present a 10-bit 1-MS/s successive approximation analog-to-digital converter core including a charge redistribution digital-to-analog converter and a comparator. A new linearity calibration technique enables use of a nearly minimum capacitor limited by kT/C noise. The ADC core without digital control blocks has been fabricated in a 0.18-μm CMOS process and consumes 118 μW at 1.8 V power supply. Also, the active area of ADC core is realized to be 0.027 mm^2. The calibration improves the SNDR by 13.4 dB and the SFDR by 21.0 dB. The measured SNDR and SFDR at 1 kHz input are 55.2 dB and 73.2 dB respectively.

key words: *analog to digital converter, charge redistribution type digital to analog converter, successive approximation architecture, calibration technique*

1. Introduction

Modern sub-micrometer CMOS process facilitates the recent trend towards large mixed-signal system-on-chip (SoC) solutions, which include not only digital circuitry but also analog circuitry on the same die. Such systems on a single chip allow the reduction of the size and power consumption, which is especially important for portable devices [1]. In such a trend, analog-to-digital converters (ADC) become increasingly important. As for the power and the area which determine the cost, the implementation of ADCs is a dominant problem on many SoC devices. To adapt it exactly to many applications, many type of ADCs are used and proposed. In these ADCs, successive approximation resister analog-to-digital converter (SAR ADC) enables the implementation of a low power, small area, highly flexible ADC. As for the speed of high resolution SAR ADC, improvements in technology enable SAR ADC to be used in applications that require speed faster than several megahertz and resolutions higher than 9-bit [2]–[5]. For higher frequency applications, a parallel architecture like an interleaved ADC is used [6]–[8]. Additionally high integration of digital circuits enables complex calibration for ADCs. Therefore the interleaved ADCs have been applied to many mixed-signal systems. However, parallel architectures usually require large area and huge cost. Usable area in a LSI limits the speed of interleaved ADC. Additionally, remotely-located ADCs cause timing and gain errors that degrade the resolution of the whole ADC. Therefore the area of a unit ADC must be reduced for high frequency applications by using an interleaved architecture. This paper presents very small size (0.05 mm^2 [9] and 0.027 mm^2) ADC cores using a simple self-calibration technique.

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2. Circuit Design

2.1 Charge Redistribution D/A Converter

A conventional SAR ADC is shown in Fig. 1. The ADC is composed of a simple capacitive DAC with a track-and-hold function which is called as charge redistribution DAC, a comparator and a successive approximation logic. As no components with large static current like an opamp are used, a low power ADC can be realized easily. As for the area in the ADC, the capacitive DAC is dominant. To shrink the area of the ADC, the total capacitance must be decreased as much as possible. However the minimum capacitor of the DAC is determined by a kT/C noise limit. Ideally a total capacitance C_{DAC} of a single DAC is

$$C_{DAC} = \frac{k_b T \cdot 10^{\frac{SNR}{10}}}{V_{FS-rms}^2} \quad (1)$$

where V_{FS-rms} is the root-mean-square value of the full-scale voltage, k_b is the Boltzman constant and T is the temperature. This characteristic is shown in Fig. 2. A desired Signal-to-Noise Ratio (SNR) of the SAR ADC decides the value of the DAC output capacitors. Therefore the total capacitor of the DAC should be designed to be a minimum capacitance that the SNR allows.

Using a fully differential binary N-bit DAC, as many as 2^{N+1} capacitors are needed. Moreover, the input bandwidth and sampling frequency are limited by the total capacitance at the input node. To increase the operating speed and maintain the desired SNR, the capacitance of the unit capacitor must be designed as small as possible in high resolution ADC. Ref. [2] uses 1.5fF unit capacitor with a special topology of metal capacitors. However it is difficult to control the small capacitance under process variations. To avoid these problems, a scaling capacitor technique like a C-2C DAC can be used. When scaling capacitors are used in a DAC, the area is affected by the combination of series and parallel capacitors. To optimize the area, the charge redistribution

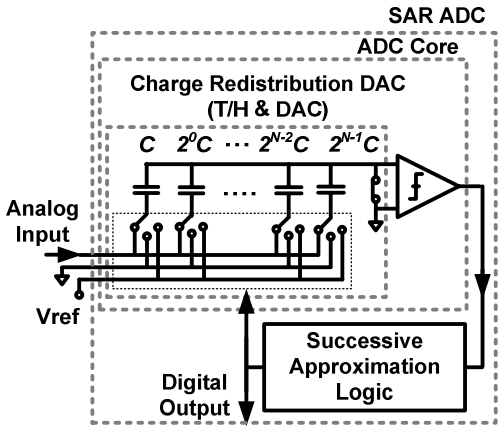


Fig. 1 Successive approximation resister ADC.

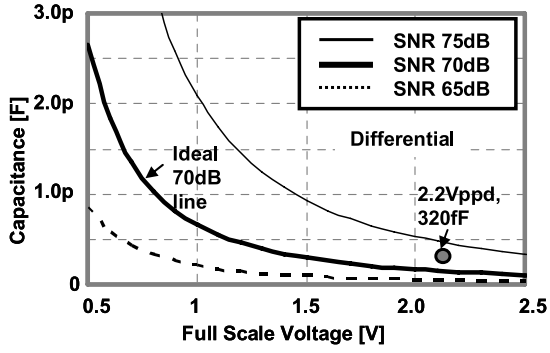


Fig. 2 Minimum capacitance at the input node.

N-bit DAC is divided into K-bit DAC units composed of series and parallel binary capacitors as shown in Fig. 3. Also, satisfying Eq. (1), an upper M-bit DAC is composed of a binary architecture. Leftover bits that cannot be realized by K-bit unit DACs and a binary DAC, L-bit, is expressed as

$$L = (N - M) \bmod K. \tag{2}$$

where $L = 0$ means that a dummy capacitor is directly connected to a unit DAC of the least bit side. The total number of lower bit DAC capacitors, NUM_{cap}, depended on the number of parallel capacitors in the unit DAC is given by

$$\begin{cases} NUM_{cap} = \dfrac{N-M-L}{K}\left(2^K + \dfrac{1}{2^K-1}\right) \\ \qquad\qquad + \dfrac{2^{2L}}{2^L-1} \qquad (L \neq 0), \\ NUM_{cap} = \dfrac{N-M-L}{K}\left(2^K + \dfrac{1}{2^K-1}\right) \\ \qquad\qquad + 1 \qquad (L = 0). \end{cases} \tag{3}$$

The relationship between parallel capacitors and DAC resolutions are indicated in Fig. 4. Thus a DAC with $K = 2$ and $K = 3$ parallel capacitors is effective in solving the area problem. If MIM capacitors are used as series capacitor, a linearity error caused by the bottom capacitance should be considered carefully. DAC's sensitivity to the bottom capacitor depends on the total capacitance at node "A." Figure 5 shows a DAC with parasitic bottom capacitors. The equivalent capacitance of the DAC output must be equal to the next upper bit capacitances, which is ideally C in this case. The gain of the unit DAC is generally designed by considering the bottom capacitor. However, in case of using small unit capacitors, estimation errors concluding process variation cannot be ignored, shown in Fig. 6. Large K values decreases the error of an equivalent capacitance at node "A." Considering the area efficiency and the error caused by the MIM bottom capacitors, 3 bits parallel ($K = 3$) capacitors are used in this paper. As shown in Fig. 7, the lower side in the main 10-bit DAC is composed of cascade connection with 3-bit unit DACs. The unit capacitor size is 20 fF and the full scale voltage is 2.2 V_{pp} (differential). To realize over 70 dB SNR, the total capacitance at the comparator input node is designed to be 320 × 2 fF (differential), which is composed of 4-bit binary.

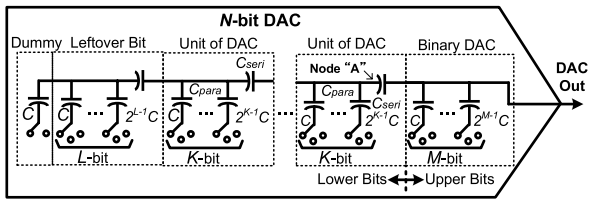


Fig. 3 N bit D/A converter with series capacitor.

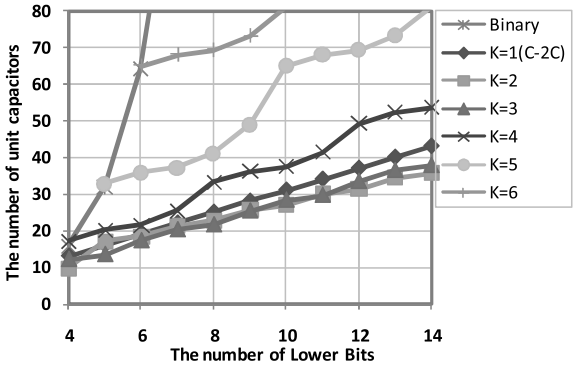


Fig. 4 The number of capacitors for a lower bit DAC.

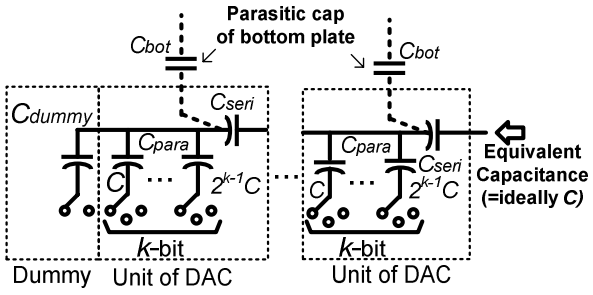


Fig. 5 The gain error caused by the bottom capacitors of series capacitors.

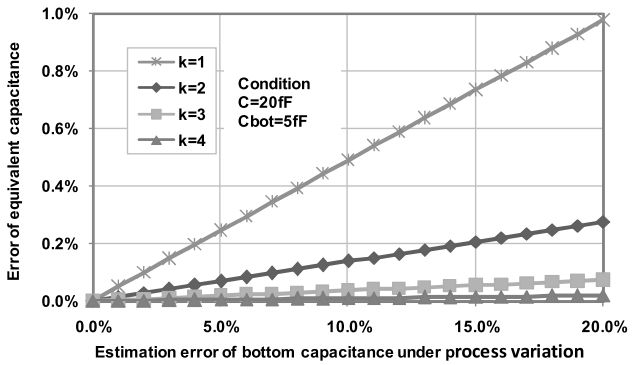


Fig. 6 The error of equivalent capacitance caused by an estimation error.

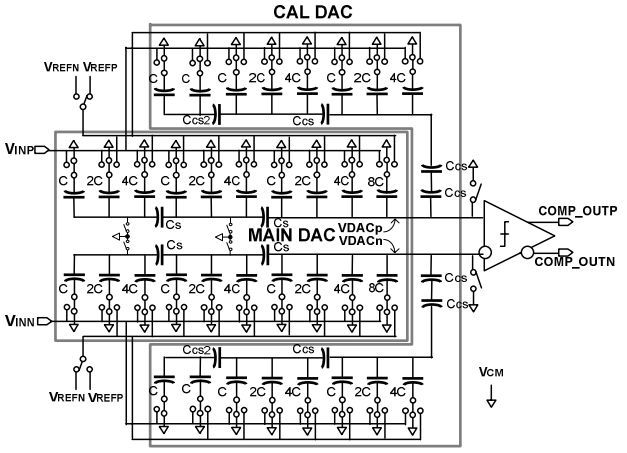


Fig. 7 Small size successive approximation A/D converter core (charge redistribution D/A converter and comparator).

2.2 Calibration

Minimizing the unit capacitance and the total capacitance at the comparator input cause mismatch error that is proportional to 1/W. And the mismatch error causes linearity error to increase. However, in this paper, to shrink the area of the ADC, the dummy capacitors that are aligned around the capacitors of the DAC are removed. Linearity problems are solved with calibration.

One calibration technique is reference voltage tuning using resistor ladder, shown in Ref. [10], [11]. However the resistor ladder needs static current and consumes large area. Another technique is the use of capacitive calibration DAC [12]. This technique has a characteristic of low power. This section describes a new self-calibration technique using a capacitive DAC. The calibration DAC (CAL DAC) is shown in Fig. 7. This CAL DAC is connected to the output of the MAIN DAC. The range of calibration is designed from −16LSB to 16LSB with 1/4LSB step. The calibration system is used for the measurement and the conversion, shown in Fig. 8. The measurements of capacitor mismatch errors are executed as show in Fig. 8(a). In this phase, the measurement controller block sets up the main DAC to output the error caused by mismatch errors of capacitors. The errors are measured by the CAL DAC operating as SAR ADC. Then the measured data are written to the Cal Memory. In the conversion phase, the measured data is retrieved by the main SAR logic and the errors of the main DAC are calibrated by the CAL DAC, as shown in Fig. 8(b).

The details of measurement sequences are as follows. To simply describe the operation, a single mode and binary weighted configuration are used as example, shown in Fig. 9. First, all the capacitors of the main DAC are connected to V_{CM} and discharged to zero. Then, shown in Fig. 9(a), the CAL DAC operates like a SAR ADC and searches the offset voltage, V_{OFFSET}. Using this operation, the offset data, defined as $D_{OFF,}$ can be obtained and is stored in the Cal Memory. The next phase is the measurement of capacitive mismatch errors which cause the linearity errors. Figure 9(b) shows the ath-bit error, ΔC_{a_err}. In this case, the output voltage of the DAC is expressed as follows.

$$\begin{aligned} V_{DAC} &= \frac{V_{REFP}\cdot(C_a+\Delta C_{a\_err}+C_{CALP})}{C_a+\Delta C_{a\_err}+C_{CALP}+C_{CALN}+\sum_{m=1}^{a-1}C_m+C_{dum}+\sum_{m=a+1}^{N}C_m} \\ &+\frac{V_{REFN}\cdot\left(C_{CALN}+\sum_{m=1}^{a-1}C_m+C_{dum}\right)+V_{CM}\cdot\sum_{m=a+1}^{N}C_m}{C_a+\Delta C_{a\_err}+C_{CALP}+C_{CALN}+\sum_{m=1}^{a-1}C_m+C_{dum}+\sum_{m=a+1}^{N}C_m} \end{aligned} \tag{4}$$

In this case, the V_{CM} is the middle of the reference voltage, V_{REFP} and V_{REFN}. So the V_{CM} is expressed as

$$V_{CM}=\frac{V_{REFP}+V_{REFN}}{2}. \tag{5}$$

The weight of the ath-bit is equal to the summation of lower DAC and dummy cap which has the same weight as the LSB weight, so the C_a can be obtained as

$$C_a=\sum_{m=1}^{a-1}C_m+C_{dum} \tag{6}$$

Using (5) and (6), the output voltage V_{DAC} can be modified as

$$\begin{aligned} V_{DAC} &= \frac{V_{CM}\left(2C_a+\sum_{m=a+1}^{N}C_m\right)}{2C_a+\Delta C_{a\_err}+C_{CALP}+C_{CALN}+\sum_{m=a+1}^{N}C_m} \\ &+\frac{V_{REFP}(\Delta C_{a\_err}+C_{CALP})+V_{REFN}C_{CALN}}{2C_a+\Delta C_{a\_err}+C_{CALP}+C_{CALN}+\sum_{m=a+1}^{N}C_m} \end{aligned} \tag{7}$$

Using a binary search algorithm with the comparator and the SAR logic, the V_{DAC} approximates the V_{CM}. In this operation, the error of the C_a can be obtained as

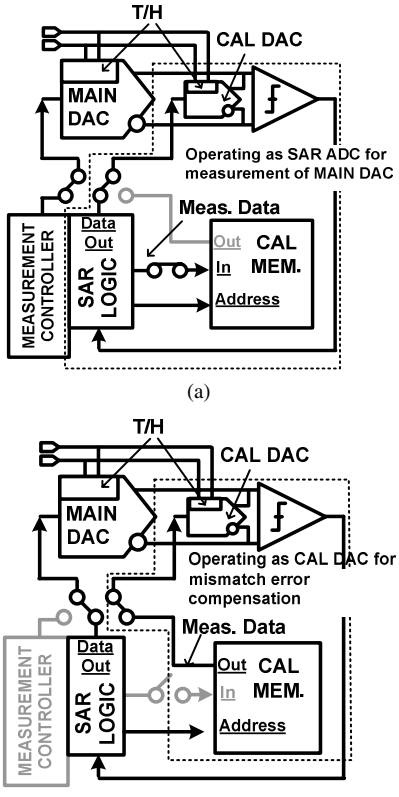


Fig. 8 System configuration (a) measurement mode (b) conversion mode.

$$\Delta C_{a\_err} = C_{CALN} - C_{CALP}. \tag{8}$$

And this data is defined as D_a. The same operation is sequentially executed from $(a + 1)$-bit to N-bit. These measured data are also defined as $D_{a+1}, \ldots, D_N$. However these data contain the data of the previous sequence. So the data must be separated before a conversion sequence begins.

$$\begin{aligned} D_{calk} &= D_a - D_{OFF} \\ D_{cal\_(a+1)} &= D_{a+1} - D_a \\ &\vdots \\ D_{cal\_N} &= D_N - D_{N-1} \end{aligned} \tag{9}$$

where the $D_{cal\_a}, \ldots., D_{cal\_N}$ is the true calibration data of the capacitive mismatch. The separations are executed in the last sequences. The separated data are stored in the Cal Memory. In this paper, the upper 6 bits are executed. In the conversion sequence, the address is accessed and added to the previous accessed data when a certain bit is called by the SAR logic.

2.3 Comparator

The block diagram of the comparator is show in Fig. 10(a). It is composed of the input switch matrix, two gain stages with output offset cancel circuits, the latch stage and the timing generator. The preamplifier has PMOS diode loads and

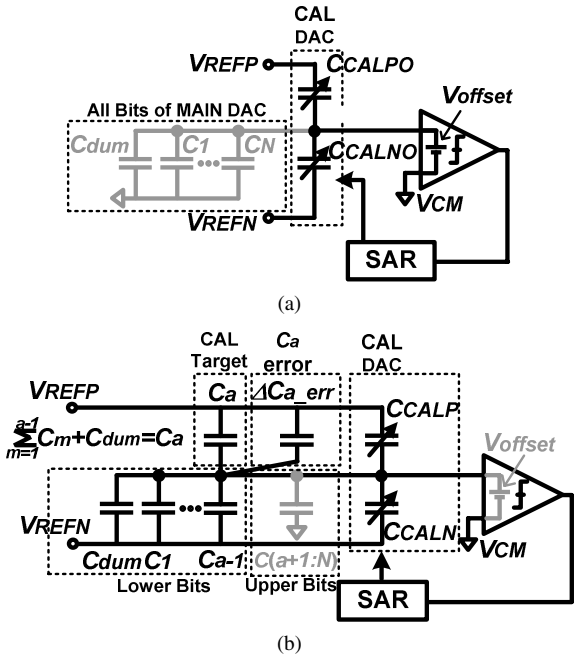


Fig. 9 Error measurement (a) comparator offset (b) linearity.

cascode connection to decrease the mirror capacitance and to isolate the input from the output (Fig. 10(b)). The total effective gain for a duration of 500 ps is designed to be about 18 dB. And the latch (Fig. 10(c)) has 240 ps propagation delay at a 1/2 LSB input. The timing generator generates the latch clock and the reset clock with non-overlapping control so as to minimize the propagation delay.

Some conventional latches generate a large kickback noise when the latch goes to the ON or OFF state. The kickback noise influences the output of the preamplifier, especially in the OFF state. The output of the amplifier must be recovered before the next bit-cycle goes to the ON state. However, using a high-speed bit-cycle, the output of the amplifier cannot be recovered and the latch makes a wrong judgment. To decrease the differential mode kickback noise, the drain of the differential pair is connected first. Then the latch turns to OFF state. This timing is generated by the series connection of two inverters. Using this technique, the differential noise is suppressed effectively, from 8.0 mV to 330 μV under typical conditions with the SPECTRE simulation.

2.4 Control Logic

The SAR logic of the conversion cycle uses a conventional SAR algorithm. The total number of clock cycles is 12 clock cycles (1 sample, 11 conversions). The control logic is needed to be flexibly programmable, therefore the SAR logic, the calibration logic, memory and other control circuits are realized by using an off chip FPGA. In this system, the conversion speed depends on the speed of the external FPGA. The Sequence Controller is composed of several counters operating as bit cycles control and calibration

cycles management. The Main DAC Setup Controller sets the main DAC to operate as either a calibration mode or a conversion mode. The SAR Logic operates for both operation modes. It is composed of temporary memories, DFF and several logic circuits. The CAL Memory block has 6×8 bits memories, and the data is added to previous latched data by the Adder, shown in Fig. 11. These data and control signals are selected by the MUX and shifted to a 1.8 V CMOS Logic level. In consideration of on chip implementation, the area of the control logic is estimated in the Table 1. The area of logic components is standard size using 0.18 μm CMOS technology. The area of the control logic using a internal logic is estimated at 0.007 mm^2. If the digital circuits are implemented on-chip, this SAR ADC is expected to operate at 28 MS/s according to SPECTRE simulation.

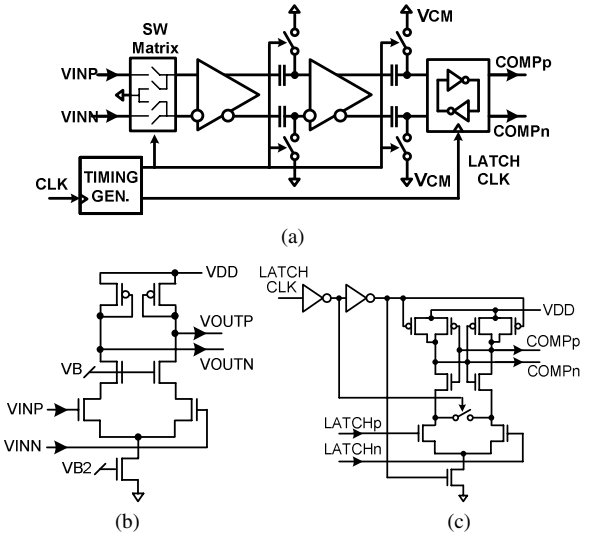


Fig. 10 Latched comparator (a) whole circuit (b) preamplifier (c) latch.

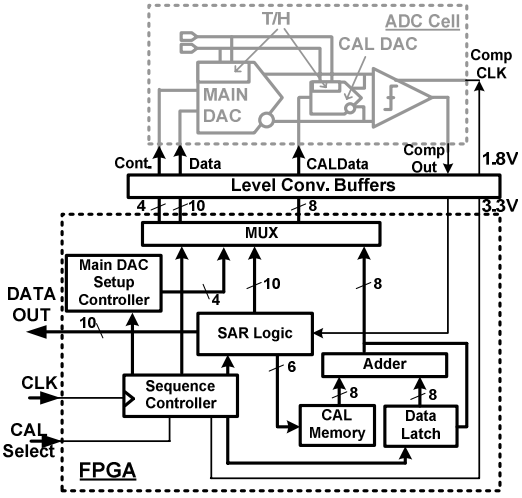


Fig. 11 Control logic.

Table 1 Estimated area of control logic circuits using internal logic components.

Used items [Standard size in 0.18um tech.]	The number of logic components	Area [mm^2]
Flip Flop[10umx5um]	90	0.0045
Full Adder [15umx5um]	7	0.00053
Multiplexer[5umx5um]	22	0.00055
Others(Based on NAND) [2umx5um]	140	0.0014
	Total	0.0070

3. Measurements Results

The chip of ADC core was fabricated in 0.18 μm CMOS process. The die photograph of the ADC core is shown in Fig. 12. The active area of the ADC core is 85 μm $\times$ 320 μm, 0.027 mm^2. Using 12 MHz system clock (1 MS/s), the ADC Core consumes 118 μW in 1.8 V power supply. The conversion speed is limited by the control logic composed of the external FPGA. Figure 13 shows the measured spectrums at 1 kHz input. Using the proposed calibration technique, the harmonic distortion are reduced by -21.0 dB. Thus the linearity is improved significantly. The calibrated ADC exhibits an SNDR and SFDR (@Nyquist) of 53.8 dB and 72.1 dB, respectively, as shown in Fig. 14 and Fig. 15. With the calibration it achieves 13.4-dB improvement of SNDR. At the nyquist frequency, 12.8-dB improvement can be achieved. Though the CAL DAC has calibrated resolution under 1 LSB, the SNDR for low-frequency input signal is 55.2 dB. The accuracy is limited by underestimated sensitivity of the comparator. Finally, the measurements are summarized in Table 2.

4. Conclusion

A new self-calibrating ADC core is proposed in this paper. Using the area optimization of the Main DAC and the self-calibrating system, the active area of the ADC core can

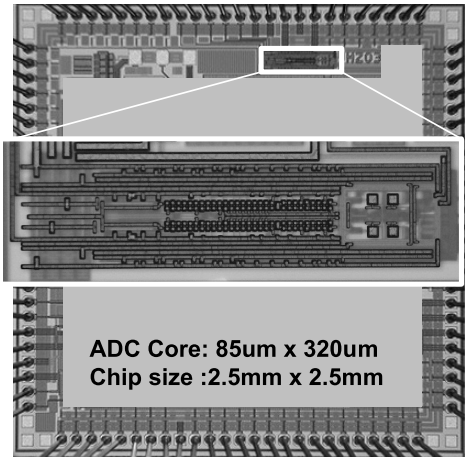
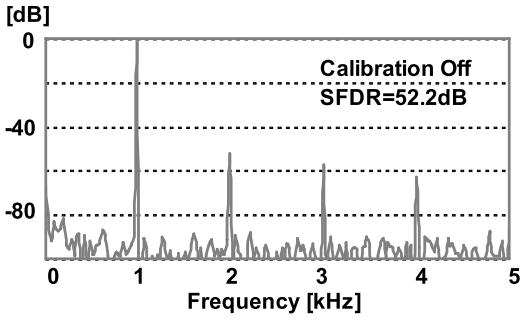
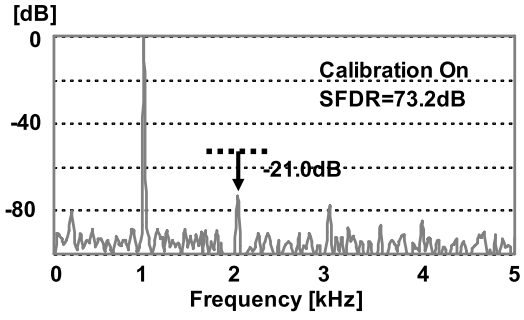


Fig. 12 Die photo.



(a)



(b)

Fig. 13 Measured spectrums (Fs = 1 MSps, 1 kHz input). (a) Calibration off (b) Calibration on.

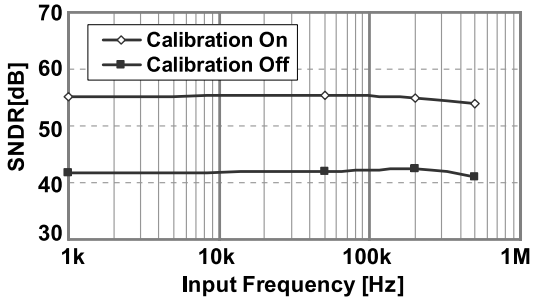


Fig. 14 Measured SNDR versus input frequency.

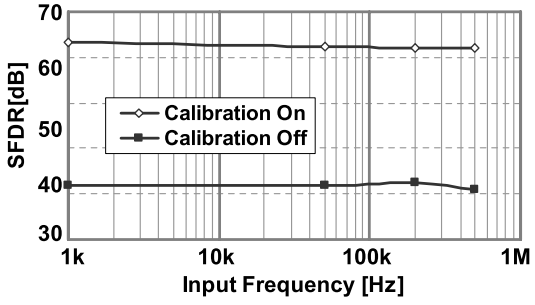


Fig. 15 Measured SFDR versus input frequency.

be 85 μm × 320 μm. With 12 MHz system clock (1 MS/s), the ADC consumes 118 μW. The calibrated ADC exhibits an SNDR and SFDR (@Nyquist) of 53.8 dB and 72.1 dB, respectively. With the calibration it achieves 13.4-dB improvement of SNDR and 21.0-dB improvement of SFDR. The ADC chip was fabricated in a 0.18 μm CMOS process.

Table 2 Summary of measurements.

Process	0.18mm, 1 poly, 6metal CMOS
Resolution	10bits
Active Area	85um x320um, 0.027mm^2
Sampling Rate	1MSps(12MHz Clock)
Analog Power	118μW @1.8V
SNDR @nyquist	53.8dB
SNDR @1kHz	55.2dB
SFDR @nyquist	72.1dB
SFDR @1kHz	73.2dB

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