社団法人 電子情報通信学会
THE INSTITUTE OF ELECTRONICS,
INFORMATION AND COMMUNICATION ENGINEERS

信学技報
TECHNICAL REPORT OF IEICE

セットリング時間最適設計技術を適用した スイッチトキャパシタ回路におけるノイズ評価

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あらまし　スイッチトキャパシタ回路において、スイッチのオン抵抗はセットリング時間に影響を与えると共に、熱雑音により精度を劣化させるため詳細な解析が求められる。精度についてはサンプリング容量を増やすことでノイズ電力を減らすことが可能であるが、速度を維持するためにはより高速動作可能なオペアンプが要求され消費電力の増加を招く。この問題に対し、スイッチのオン抵抗を考慮したポール・ゼロキャンセル法を用いることで消費電力を増加させずにセットリング時間を大幅に改善できる手法が提案されている。本論文ではこのセットリング時間最適設計技術を適用したスイッチトキャパシタ回路におけるノイズ評価を行った。その結果、最適設計技術を用いた場合、帯域の増加分と追加した抵抗によりノイズは増加することが明らかとなった。しかしながらノイズの増加よりも帯域の増加の割合のほうが大きくなるため、最適設計技術は電力効率に優れていることが明らかとなった。

キーワード　スイッチトキャパシタ回路、スイッチオン抵抗、熱雑音

Thermal Noise Effects Caused by Settling Time Optimization in Switched-Capacitor Circuits

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Abstract　Switch thermal noise represents a major limitation on the performance of switched-capacitor circuits. In these circuits, the total noise power can be reduced by increasing the sampling capacitance of the circuits. However, it also increases the settling time, hence requires high-performance opamps. This leads to larger power dissipation. A pole-zero cancellation method can be used to improve the settling time while maintaining the power consumption. This paper describes the noise effects caused by this settling time optimization technique in switched-capacitor amplifiers. Theory and simulation results show that the pole-zero cancellation is highly power-efficient technique, even though it increases the noise power.

Keyword　switched-capacitor circuit, switch on-resistance, thermal noise

1. Introduction

Switched-Capacitor (SC) circuits are basic building blocks in the design of analog and mixed-signal circuits. The reduction in supply voltage that accompanies the aggressive scaling of feature sizes in modern CMOS technologies increases drastically the switch on-resistance. Switch sizing is an important issue which affects the overall performance of SC circuits. Small size switches have large on-resistances that increase the settling time of the SC circuits. The incomplete transfer of charge produces gain error and distortion at the output of the circuits. On the other hand, large size switches may suffer from undesirable channel charge injection and clock feed-through due to parasitic capacitances. It is also very difficult to drive large switches under low-voltage environment. The traditional switch design techniques use the minimum size that allows proper settling time.

A pole-zero cancellation technique for fast settling in pipelined ADC's multiplying digital-to-analog converter has been reported [1]. The key point of this work is that they optimize the switch on-resistance in the feedback path to cancel out the dominant pole. This optimization may alleviate the power consumption issue that is normally associated with high-speed design technique. However, the noise effects caused by this technique have not been discussed. It is also meaningful to explore the possibilities of the use of the pole-zero cancellation technique in other switched-capacitor circuits, such as SC integrators in ΣΔADC. In this paper, the effects of thermal noise on the performance of charge-redistribution switched-capacitor amplifiers will be discussed. By evaluating the noise effects in SC amplifiers, we demonstrate that the pole-zero cancellation technique is an effective way to achieve a broad bandwidth without sacrificing power consumption.

In section 2, the pole-zero cancellation technique is reviewed and employed in a charge-redistribution SC amplifier. Section 3 compares the noise performance of the SC amplifier with the added resistance in the feedback path to the conventional structure during the hold phase as a continuous-time system. Section 4 describes the overall noise performances

of the amplifier. In section 5, we evaluate the efficiency of the pole-zero cancellation technique. In Section 6, we end up with some conclusions.

2. SC Amplifier Settling Optimization

Fig. 1 shows the implementation of the classical charge-redistribution SC amplifier. We have inserted a resistance r_f in the feedback path of the amplifier to employ the pole-zero cancellation technique. In Fig. 1, ϕ_1 and ϕ_2 are non-overlapping clocks. During the ϕ_1 phase ($\phi_1 = 1$), the voltage across the sampling capacitor C_s tracks the input voltage v_{in} and C_s stores a charge $q_1(n) = C_s\, v_{in}(n)\,(1-\varepsilon)$ at the end of the phase. Here, ε is the settling error, determined by the required charging accuracy. Assuming that the two series switches have the same on-resistance r_{on}, the settling time is given by

$$t_{set} = 2r_{on}C_s \ln\frac{1}{\varepsilon}. \tag{1}$$

The settling time in the sampling phase, therefore, can be reduced by decreasing the switch on-resistance r_{on} or the sampling capacitor C_s.

During the ϕ_2 phase, C_s discharges q_1 into the virtual ground created by the opamp, and hence, it changes the charge stored in C_i. The settling time in the hold phase can be calculated by using a continuous-time transfer function model. The following discussion illustrates how the pole-zero cancellation technique improves the settling time of the system.

2.1. Pole-Zero Cancellation

Fig. 2 shows the equivalent circuit of the SC amplifier during the hold phase. In this analysis, we assume that all switches have the same on-resistance r_{on} and the opamp is properly compensated, so that the effects of the second pole of the opamp can be neglected. Here, C_o is the unit capacitance (where $C_f = C_o$、 $C_s = mC_o$), C_{pi} is the opamp parasitic input capacitance, g_m is the transconductance of the device, r_L is output impedance of the opamp, and C_{po} is the opamp parasitic output capacitance.

To simplify the calculation, it is reasonable to assume that $C_{pi} << C_o$ and $g_m r_L >> 1$. Under this condition, the closed-loop transfer function is found as

$$H(s) = \frac{s + z_1}{(s + p_1)(s + p_2)} \tag{2}$$

where

$$z_1 = \frac{g_m}{C_o(-1 + g_m r_f)} \tag{3}$$

$$p_1 = \alpha - \sqrt{\alpha^2 - \frac{g_m}{mC_oC_{po}(2r_{on} + r_f)}} \tag{4}$$

$$p_2 = \alpha + \sqrt{\alpha^2 - \frac{g_m}{mC_oC_{po}(2r_{on} + r_f)}} \tag{5}$$

$$\alpha = \frac{mC_o(1 + 2g_m r_{on}) + C_L(m+1)}{2mC_oC_{po}(2r_{on} + r_f)}. \tag{6}$$

For $p_1 = z_1$ where the dominant pole and the zero are at the same location, this gives

$$r_f = 2mr_{on} + \frac{(m+1)}{g_m}. \tag{7}$$

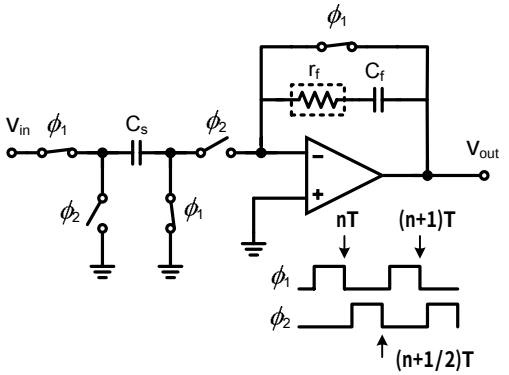

Fig. 1 A charge-redistribution SC amplifier with an added resistance.

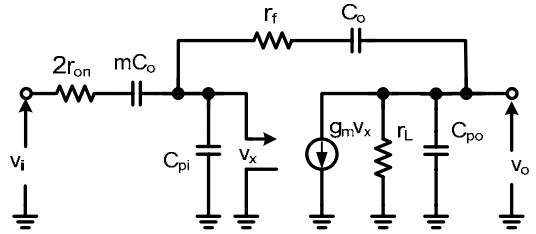

Fig. 2 Equivalent circuit of the SC amplifier during the hold phase.

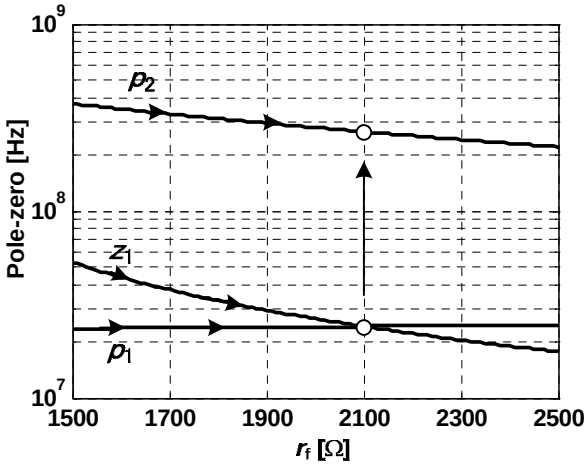

Fig. 3 Pole-zero of the closed-loop system vs. the feedback resistance.

Table 1 Model parameters.

r_{on}	g_m	m	C_o	C_{pi}	C_{po}
50 Ω	1 mS	1	6 pF	100 fF	300 fF

If the condition (7) is satisfied, p_1 and z_1 cancel each other out and p_2 becomes the dominant pole of the closed-loop transfer function as shown in Fig. 3. All parameters are given in Table 1.

2.2. SC Amplifier Settling

In this section, we confirm the settling time improved by employing the pole-zero cancellation technique. Under the condition (7), the dominant pole of the closed-loop system becomes

$$p_{dom} = \frac{g_m}{(m+1)C_{po}}. \tag{8}$$

As Fig. 3 shows, the dominant pole is shifted to higher frequency. Thus, the

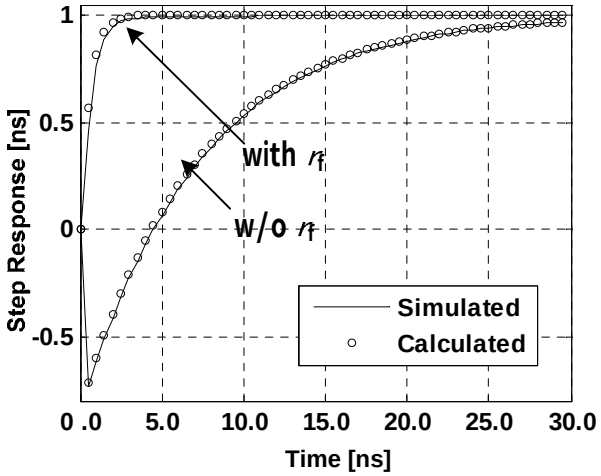

Fig. 4 Step response of the closed-loop system with and without resistance r_f.

settling time is improved. Fig. 4 shows the step response of the amplifier with and without the feedback resistance. Adding the resistance r_f reduces the 1% error settling time from 38.0 ns to 4.1 ns, that is 9.3 times faster. The analysis is calculated with symbolic analysis tool MAPLE and simulated by CADENCE SPECTRE.

We now examine the possibility to increase p_{dom} to further improve the settling time. It is clearly seen that an increase of g_m, which requires larger power consumption, reduces the settling time. Another way to increase p_{dom} is to decrease the gain coefficient m. Generally speaking, the sampling capacitance is determined by the kT / C noise to ensure the required dynamic range [9]. Therefore, smaller m yields a larger capacitance in the feedback path. For a circuit whose area is dominated by its capacitors, this condition corresponds to large area. A compromise is made here between speed and area, confirms tradeoffs among speed, power, and area.

Finally, it is useful to consider the effect of slewing. When slewing occurs, the settling time will increase. Typically, a given application will require specified settling error and settling time, corresponding to the required dynamic range and sampling frequency. The traditional design uses the minimum current that satisfies the settling time requirement. However, for some circuits, the outputs of the opamps (e.g., ΣΔADC) may be scaled down to desired values by scaling the coefficients of the circuits [7], and hence, the slewing may be prevented.

3. Thermal Noise in SC Amplifier during Hold Phase

This section compares the noise performance of the SC amplifier with the added resistance in the feedback path to the traditional structure during the hold phase. For a low-power design, opamp dominates both the bandwidth and the noise, while the switches on-resistances may be negligible. As illustrated below, employing the pole-zero cancellation technique further increases the opamp noise bandwidth. Moreover, the additional resistance itself produces noise. Therefore, the output SNR is degraded due to the increase of the noise power.

3.1. Opamp Thermal Noise

We now discuss the increase of the output noise power due to the opamp thermal noise. To simplify the calculations, the power spectrum density (PSD) of the opamp input-referred noise is approximately given by [2]

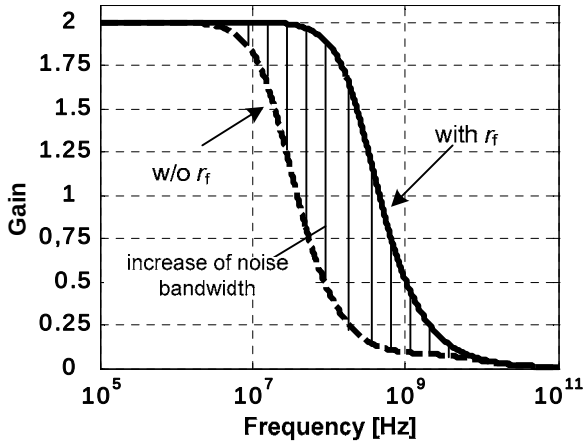

Fig. 5 Frequency responses of the opamp noise transfer function.

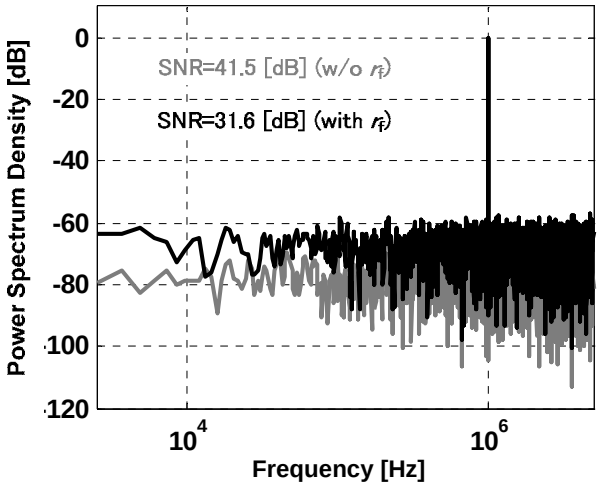

Fig.6 Output spectrum of the SC amplifier with 10mVpp sine input.

$$\overline{v_{op}^2} = \frac{16kT}{3g_m} \tag{9}$$

where k is the Boltzmann constant, k = 1.38 × 10^{-23} J/K, T is the absolute temperature in degrees Kelvin, and g_m is the transconductance of the device. Note that for the transient noise simulation, the opamp noise should be modeled by a noise current at the output to create a virtual ground at the input of opamp. The noise voltage transfer function from the input of the opamp to the output of the integrator is found to be

$$H_{op}(s) = \frac{mg_mC_0(2r_{on}+r_f)s + g_m(m+1)}{mC_0C_{po}(2r_{on}+r_f)s^2 + [mC_0(1+2g_mr_{on}) + C_{po}(m+1)]s + g_m} . \tag{10}$$

The PSD of the output noise due to the opamp noise is then calculated by

$$P_{op}^2(f) = \overline{v_{op}^2} \cdot \left| H_{op}(j2\pi f) \right|^2 . \tag{11}$$

Fig. 5 shows the frequency responses of the opamp noise transfer function (10). As shown, when the pole-zero cancellation technique is employed, the opamp noise bandwidth increases drastically. The increase of the output noise power degrades the SNR performance. This SNR degradation may be calculated by integrating the shaped PSD from dc to infinity frequency

$$\Delta = 10\log\left(\int_0^\infty \overline{v_{in}^2}\cdot\left|H_{op\_opt}(j2\pi f)\right|^2 df\right) - 10\log\left(\int_0^\infty \overline{v_{in}^2}\cdot\left|H_{op}(j2\pi f)\right|^2 df\right)$$

$$= 10\log\left(\int_0^\infty \left|\frac{H_{op\_opt}(j2\pi f)}{H_{op}(j2\pi f)}\right|^2 df\right). \quad (12)$$

Notice that the SNR degradation due to the opamp noise is independent of the opamp input-referred noise. This is because the noise increase (in dB) is determined by how wider the opamp noise bandwidth becomes. Since the settling time is 9.3 times faster, the output SNR decrease is predicted to be 10log (9.3) = 9.7 dB. This result has been verified by means of simulation (Fig. 6) and calculation from (12). Note that the transient noise simulation, which can not be done with the interested bandwidth from dc to infinity, is a time consumer with large noise bandwidth (i.e., large noisefmax). It is often useful to know the noise bandwidth, which can be easily calculated or simulated by SPECTRE noise analysis, to ensure the accuracy of the simulation results.

3.2. Added Resistance Thermal Noise

The PSD of the added resistance thermal noise is approximately given by

$$\overline{v_{rf}^2} = 4kT\cdot r_f \quad (13)$$

where r_f is given by (7).

The noise voltage transfer function from the added resistance to the output of the integrator is given by

$$H_{rf}(s) = \frac{mC_0(2r_{on}g_m+1)s+g_m}{mC_0C_{po}(2r_{on}+r_f)s^2+[mC_0(1+2g_mr_{on})+C_{po}(m+1)]s+g_m}. \quad (14)$$

The PSD of the output noise due to the added resistance thermal noise is then given by

$$P_{rf}^2(f) = \overline{v_{rf}^2}\cdot\left|H_{rf}(j2\pi f)\right|^2. \quad (15)$$

Equation (7) suggests that in order to reduce the added resistance thermal noise without increasing the power consumption, m or r_{on} should be decreased. However, as discussed above, decreasing the coefficient m increases the area, and minimizing the switches on-resistances r_{on} is still an issue in scaled CMOS. Therefore, the specifications of the whole system should be taken into consideration in making tradeoffs among noise, power, and area.

3.3. Switches On-resistances Thermal Noise

Assuming that all switches have the same r_{on}, the combined switch resistance is $2r_{on}$ and the PSD of the associated noise voltage is given by

$$\overline{v_{sw}^2} = 4kT\cdot(2r_{on}). \quad (16)$$

The noise voltage transfer function from the switches on-resistances to the output of the amplifier is given by

$$H_{sw}(s) = \frac{mC_0(r_f g_m-1)s+mg_m}{mC_0C_{po}(2r_{on}+r_f)s^2+[mC_0(1+2g_mr_{on})+C_{po}(m+1)]s+g_m}. \quad (17)$$

The PSD of the output noise due to the added resistance thermal noise is then given by

$$P_{sw}^2(f) = \overline{v_{sw}^2}\cdot\left|H_{sw}(j2\pi f)\right|^2. \quad (18)$$

Note that for a low kT/C noise (i.e. large C) and low power (i.e. small g_m) design, the zero of the closed-loop system is located at low frequency, as indicated in (3). Because the switches noise transfer function is the same as the transfer function of the system, the pole-zero cancellation technique also improves the switches noise bandwidth (as depicted in Fig. 7). The integrated noise power of the switches on-resistances with and without r_f are -81.3 dBV and -91.7 dBV, while those of the opamp are -83.9 dBV and -74.4 dBV, respectively. Therefore, adding r_f in the feedback path not only improves the settling time of the system, but also reduces the switches noise bandwidth. It is important to remember that the integrated noise power depends on both the noise level and the noise bandwidth. As will be illustrated, for a low power design, the switches on-resistances noise level is comparably lower than that of the opamp. Thus, when the resistance is added in feedback path, the noise effects of switches become negligible compared to that of the opamp, which agrees with the calculated results above.

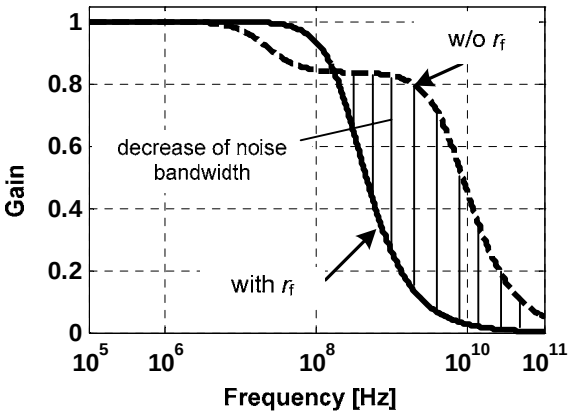

Fig. 7 Frequency responses of the switches noise transfer function.

3.4. Total Thermal Noise

Consider next the total noise power presented at the output of the SC amplifier during the hold phase. Since the three noise voltages given in (11), (15), and (18) are uncorrelated, their powers are added. Hence, the total power noise is

$$P_h^2 = P_{op}^2 + P_{rf}^2 + P_{sw}^2. \quad (19)$$

Fig. 8 shows the calculated and simulated output noise power given in (19), where the parameters were given in Table 1. Since all noise contributors have the same bandwidth, the relative opamp noise contribution can be simply calculated by using DC noise level as follows:

$$\frac{P_{op}^2(0)}{P_h^2(0)} = \frac{4(m+1)}{4m+7+6mg_mr_{on}} = \frac{8}{11+6x} \quad (20)$$

where $m = 1$ and $x = g_m r_{on}$ was introduced.

Similarly, the relative feedback resistance and switches noise contributions are $(3x + 3) / (11 + 6x)$ and $3x / (11 + 6x)$, respectively. As shown in Fig. 9, for a low-power design, where $1 / g_m >> r_{on}$ (i.e. $x << 1$), the opamp dominates the noise, while the noise contribution of switches may be negligible. It is due to the fact that the input-referred noise of the opamp is inversely proportional to g_m, as (9) shows. It also shows that decreasing the switch on-resistance reduces the noise contribution of the switches. However, it does not reduce the total noise power effectively, as shown in Fig. 10. By contrast, an increase of g_m improves opamp noise performance. Moreover, as (7) shows, larger value of g_m reduces the value of r_f and hence,

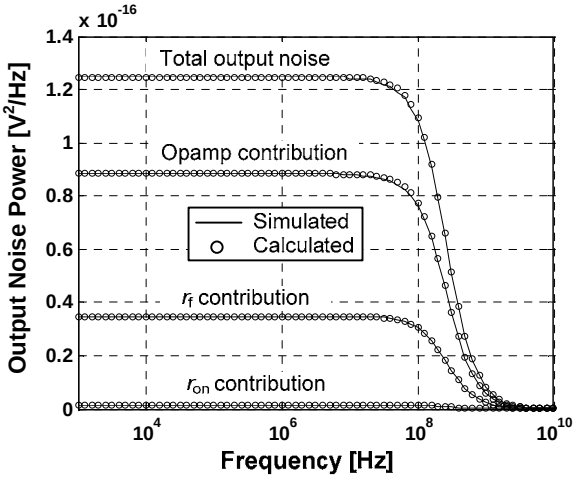

Fig. 8 Output noise power of the SC amplifier during the hold phase.

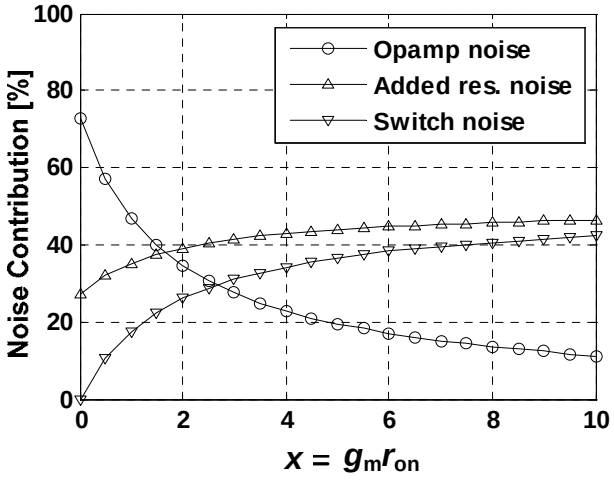

Fig. 9 Relative contributions to the total noise during the hold phase.

reduces the output noise power due to the added resistance r_f. Therefore, increasing g_m reduces the output noise level effectively (Fig. 10). However, an increase of g_m also increases the noise bandwidth. Thus, the overall integrated noise power performance is not improved. Typically, to reduce the integrated noise, the noise level has to be reduced while maintaining the noise bandwidth. It should be done by increasing both g_m and capacitors of the circuits. In general, an optimization should be performed to minimize the power and area for desirable thermal noise level and required signal bandwidth.

Finally, we examine the output SNR degradation of the amplifier during the hold phase. The output-referred noise power can be calculated by integrating the output PSD shown in (19). Calculation and simulation show that the output SNR degrades 6.2 dB (from 36.4 dB to 30.2 dB) when employing the pole-zero cancellation technique.

4. Thermal Noise in SC Amplifiers

The noise effects of the SC amplifier during the hold phase caused by the settling time optimization as a continuous-time noise were discussed. In this section, we investigate the contribution of the noise during the hold phase to the total performance, which includes the noise during the sampling phase.

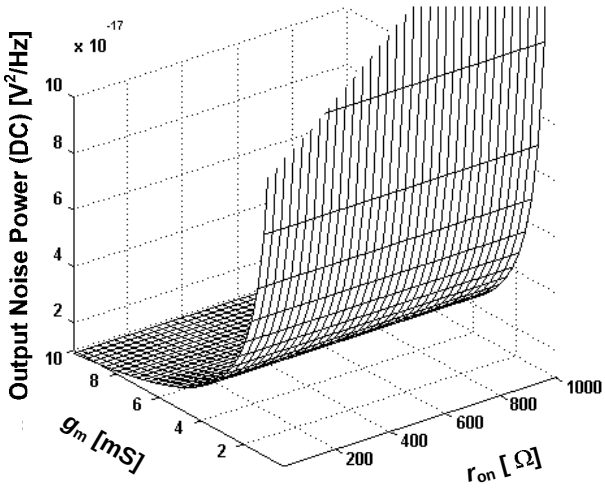

Fig. 10 Total noise power of the SC amplifier during the hold phase.

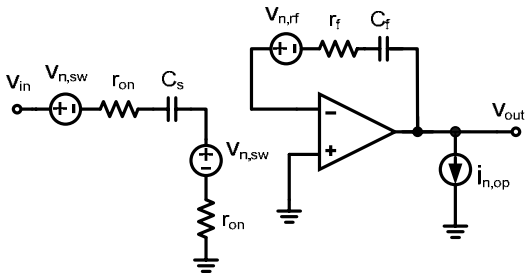

Fig. 11 Equivalent circuit of the SC amplifier during the sampling phase.

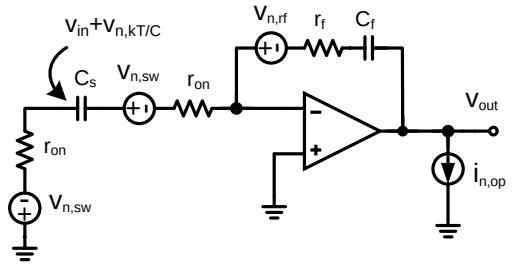

Fig. 12 Equivalent circuit of the SC amplifier during the hold phase.

The equivalent circuits of the SC amplifiers in the sampling phase and the hold phase are shown in Fig. 11 and Fig. 12, respectively. During the sampling phase, the capacitor C_s tracks the input voltage v_{in} and the noise voltage from the switches, and stores a charge $q_1(n) = C_s(v_{in}(n) + v_{n,kT/C}(n))$. The noise power stored in C_s is known as kT / C_s, which is nearly perfectly white from dc to f_s / 2 (f_s is the sampling frequency). In a SC circuits design, the system bandwidth must be much larger than the sampling frequency, in order to enable a total charge transfer. Therefore, this noise will not be filtered by the low-pass filter which has the same transfer function as (17). By contrast, the kT / C_s noise will be amplified by C_s / C_i. Hence, the total output noise power due to kT / C_s noise is

$$P_s^2 = \int_0^{f_s/2} \frac{kT}{C_s} \cdot \frac{1}{f_s/2} \cdot \left(\frac{C_s}{C_i}\right)^2 df = \frac{mkT}{C_o} \cdot \tag{21}$$

Consider next the total output noise during the hold phase. As shown in Fig. 8, when the pole-zero cancellation technique is employed, the PSD of

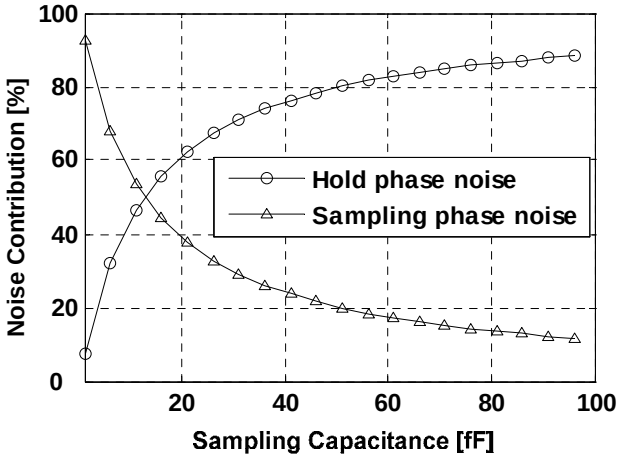

Fig. 13 Relative contributions to the total output noise of the SC amplifier when employing the pole-zero cancellation technique.

the noise during the hold phase is processed by a first-order transfer function that can be found as

$$v_{h\_opt}^2 = \left(\frac{16kT}{3g_m} \cdot (m+1)^2 + 4kT \cdot 2r_{on} \cdot m^2 + 4kT \cdot r_f \right) \cdot \left| \frac{1}{1+s\tau} \right|^2 \quad (22)$$

Here, the time constant $\tau = 1 / (2\pi p_{dom})$, and p_{dom} is given by (8).

Hence, the total noise power in the hold phase can be calculated by integrating the output PSD given in (22) from dc to infinite frequency

$$P_{h\_opt}^2 = \left(\frac{16kT}{3g_m} \cdot (m+1)^2 + 4kT \cdot 2r_{on} \cdot m^2 + 4kT \cdot r_f \right) \cdot \frac{1}{4\tau} \quad (23)$$

The total output noise power is then

$$P_n^2 = P_{h\_opt}^2 + P_s^2 . \quad (24)$$

As shown in Fig. 13, the contribution of the noise during the sampling phase to the total noise is inversely proportional to the sampling capacitance. Therefore, with C_s = 6 pF, the noise during the sampling phase may be ignored. The calculation and simulation show that the output SNR of the SC amplifier with and without resistance r_f are, respectively 36.4 dB and 30.1, nearly the same as the results in section 3.4. Note that, the noise during the hold phase is independent of the sampling capacitance. It is due to the fact that the dominant pole and zero of the system are cancelled out. It also shows that the minimum value of sampling capacitance can be obtained for a desirable thermal noise level.

5. Figure of Merit

We now evaluate the efficiency of the pole-zero cancellation technique. The figure-of-merit (FoM) may be defined as follows:

$$\text{FoM} = \frac{P}{f_B \times SNR} \quad (25)$$

where f_B is the signal bandwidth and P is the power consumption. The FoM is a measure of the power efficiency, taking signal bandwidth and signal-to-noise ratio into consideration. Smaller FoM means higher power efficiency.

As illustrated above, employing the pole-zero cancellation improves by 9.3 times the settling time and hence, nearly 9.3 times the bandwidth. However, SNR decreases 6.3 dB, or 4.3 times smaller due to the increase of total noise power. The FoM is then improved by 1 / 2 by using pole-zero cancellation. The attractive results show the potential of the use of the pole-zero cancellation technique in the future, such as ΣΔADC.

6. Conclusion

The effects of thermal noise caused by the pole-zero cancellation on the performance of the SC were analyzed. The settling time of SC amplifiers was shown that it can be improved effectively by using the pole-zero cancellation, up to 9 times smaller. The noise caused by employing the pole-zero cancellation technique is carefully calculated and simulated in the hold phase. By comparing the bandwidth improvement to the SNR decrease, the pole-zero cancellation is demonstrated to be a highly power-efficient technique.

Acknowledgments

This work was partially supported by MIC, NEDO, JST, and VDEC in collaboration with Cadence Design Systems, Inc.

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