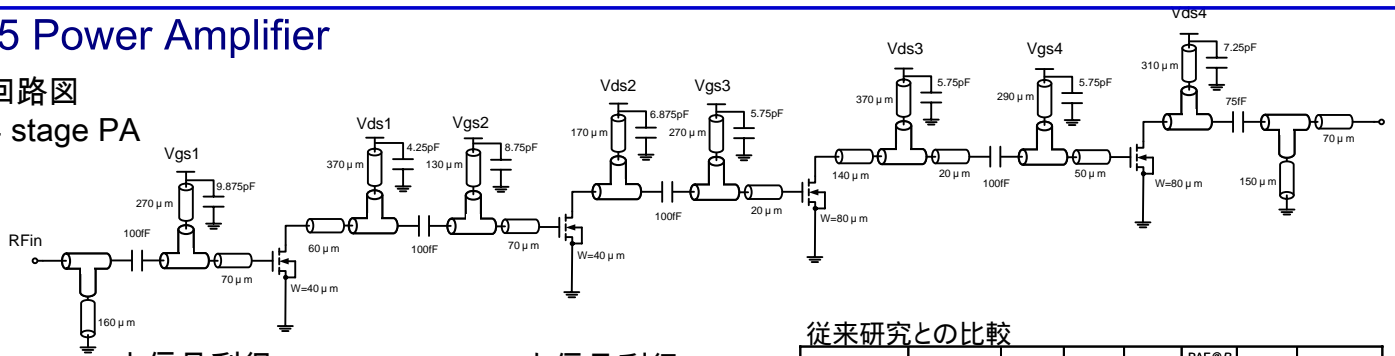


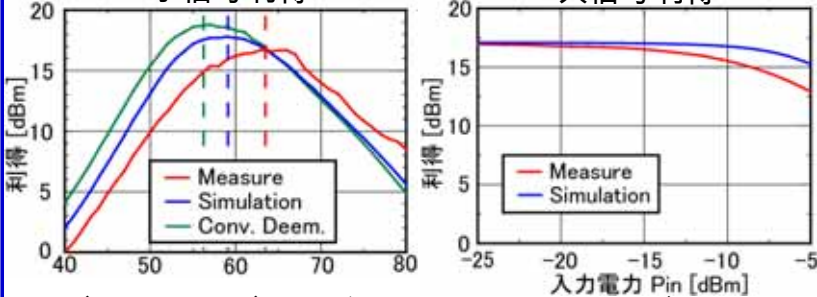
# 5 Power Amplifier

回路図  
4 stage PA



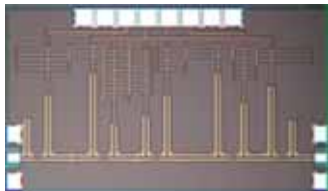
小信号利得

大信号利得



新ディエンベディングにより、周波数のズレを改善

Chip 写真 (CMOS 65nm)



1.5mm  
×  
0.85mm

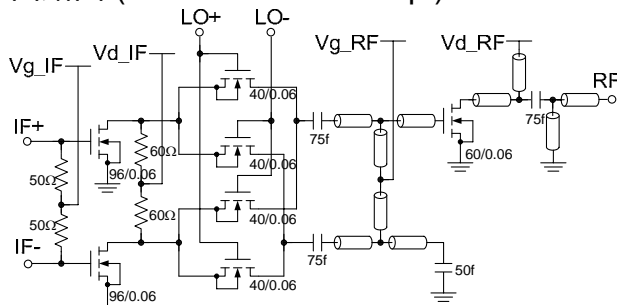
従来研究との比較

Reference	Technology	Freq. [GHz]	Gain [dB]	P <sub>1dB</sub> [dBm]	PAE@P <sub>1dB</sub> [%]	P <sub>dc</sub> [mW]	V <sub>dd</sub> [V]
[1] JSSCC 2007	90nm CMOS	61	5.2	6.4	7.4	21	1.5
[2] RFIC 2008	90nm CMOS	63	14	11	15	81	1.2
[3] ISSCC 2008	90nm CMOS	60	8.2	8.2	2.4	229	1.2
[4] ISSCC 2008	90nm CMOS	60	5.5	9	6	80	1
[5] ISSCC 2008	90nm CMOS	60	13.3	10.5	8	150	1
[6] ISSCC 2009	65nm CMOS	60	15.8	2.5	3.95	43.5	1
[7] ISSCC 2009	45nm CMOS	60	13.8	11	-	-	1.1
[8] MWCL 2009	90nm CMOS	60	30	10.3	6	178	1.8
<b>This work</b>	<b>65nm CMOS</b>	<b>61.5</b>	<b>16.4</b>	<b>4.6</b>	<b>2.3</b>	<b>122</b>	<b>1.2</b>

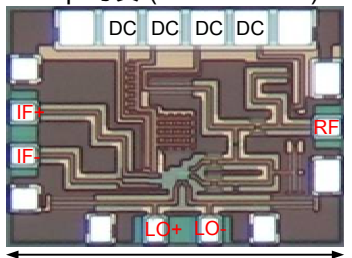
[1] T. Yao, et al., JSSC 2007 (Toronto Univ.) [2] T.L. Rocca, et al., RFIC 2008 (UCLA) [3] T. Suzuki, et al., ISSCC 2008 (Fujitsu)  
[4] D. Chowdhury, et al., ISSCC 2008 (UCB) [5] M. Tanomura, et al., ISSCC 2008 (NEC)  
[6] W.L. Chan, et al., ISSCC 2009 (Delft Univ.) [7] K. Raczkowski, et al., ISSCC 2009 (KU Leuven&IMEC)  
[8] J.-L. Kuo, et al., MWCL 2009 (NTU)

# 6 Up-Conversion Mixer

回路図 (Passive Mixer + Amp.)



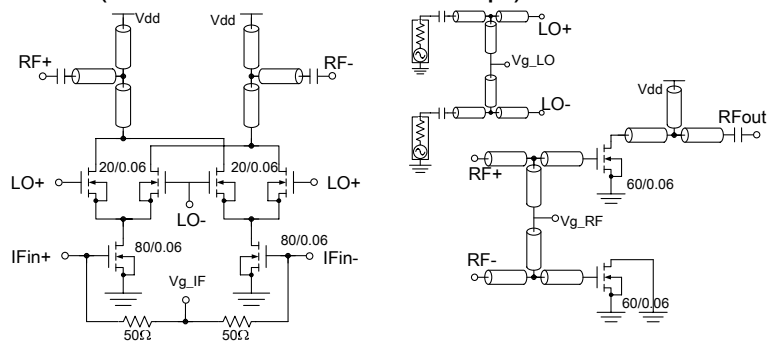
Chip 写真 (CMOS 65nm)



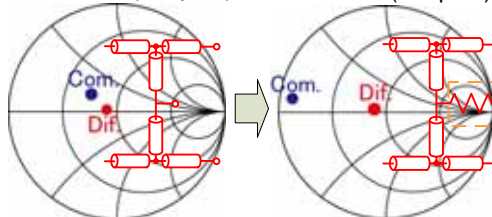
0.76 mm  
×  
0.53 mm

# 7 Up-Conversion Mixer ver.2

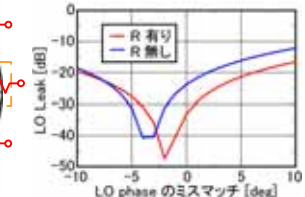
回路図 (Gilbert Cell Mixer + RF Amp.)



Reflection (LO port) Reflection (LO port)



LO Leak の比較



抵抗によって共通モードのインピーダンスをずらし、LO Leakを抑制

測定とSim.との比較

IF:1GHz LO:60GHz(-1dBm)

問題点

- CG、Pout1dBが小さい
- LO Leakが大きい

	Measure	Simulation
CG [dB]	-6.7	-5.7
Pout1dB [dBm]	-14.5	-8.73
Pdc [mW]	49	55
LO Leak [dB]	-21.5	-29.4

従来研究との比較

Reference	CMOS Node	DC Power [mW]	Supply Voltage[V]	RF [GHz]	LO P. [dBm]	CG [dB]	RF Output @1dB [dBm]	LO-RF Isolation [dB]
[1]RFIC2008	65nmCMOS	29	-	60	5	-6.5@IF=10GHz	-5	30
[2]SCAS2007	90nmCMOS	70	1.5	60	-	-4 ~ -7@IF=1GHz	-	-
[3]ESSCIRC2007	65nmCMOS	0	-	60	9	-13.5@IF=2GHz	-19	34
[4]Electronics Letters2008	130nmCMOS	24	1.6	56 ~ 65	0	-8 ~ 4@IF=1GHz	-5.6	37
[5]SCAS2007	90nmCMOS	13.2	-	51	0	-11@IF=11GHz	-12	26.5
<b>This work(Sim.)</b>	<b>65nmCMOS</b>	<b>33</b>	<b>1.2</b>	<b>61</b>	<b>-5</b>	<b>4@IF=1GHz</b>	<b>-6</b>	<b>38.2</b>

[1] Alberto Valdes-Garcia, et al., RFIC 2008 (IBM) [2] S.P. Voinescu, et al., ISCAS 2008 (Univ. of Toronto) [3] Mikko Varonen, et al., ESSCIRC 2007 (Helsinki Univ. of Tech)  
[4] F. Zhang, et al., EL 2008 (Univ. of Melbourne) [5] I. C. H. Lai, et al., ISCAS 2007 (The Univ. of Tokyo)

# 8 結論

新しいディエンベディング方法を用いることにより、PAのMeas.と実測とのズレを改善した60GHz帯、16QAMの無線通信に必要なスペックを満たすPA、Up-Mixerを設計した