A Low-Offset Latched Comparator Using Zero-Static Power Dynamic Offset Cancellation Technique

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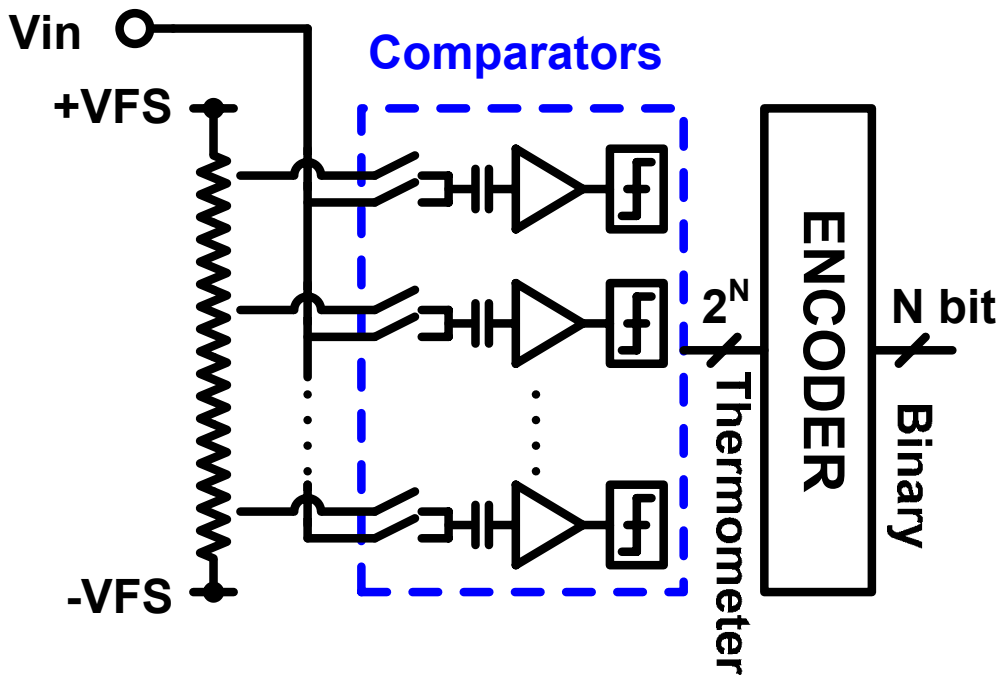
Outline

- Motivation
- Design Concept
- Proposed Comparator
- Measurement Results
- Conclusions

Motivation

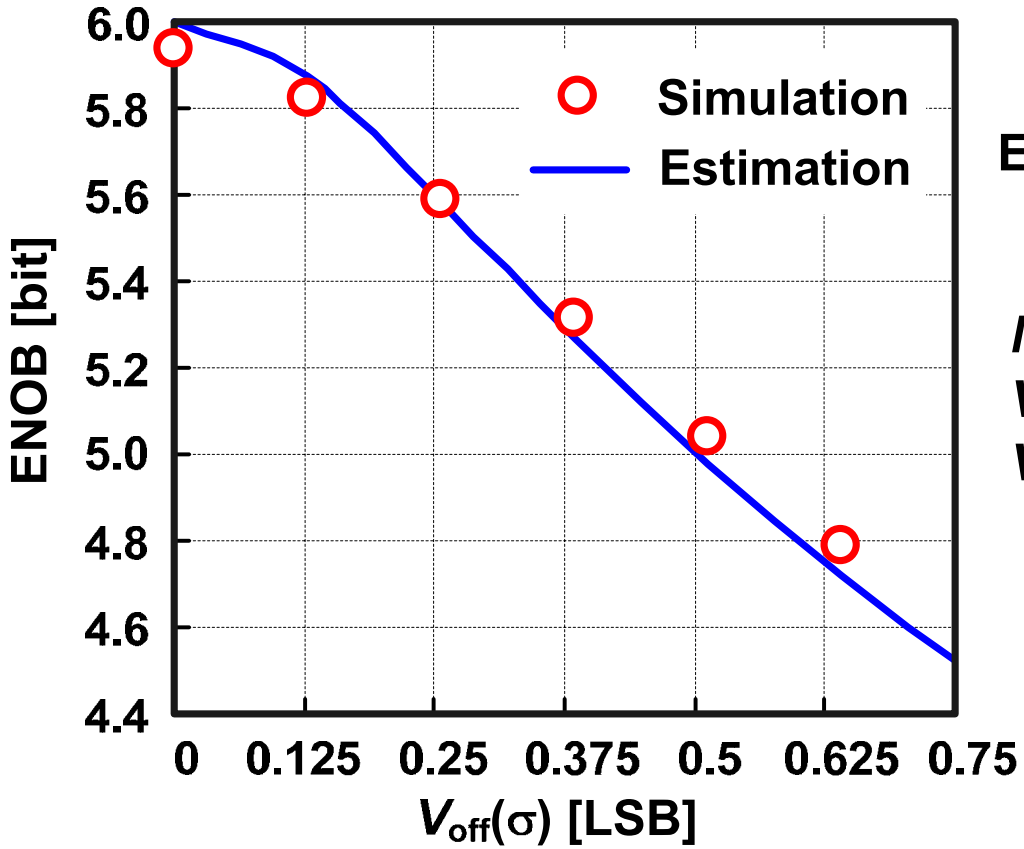
Comparator performance is important in comparator based ADCs.



Comparator offset
$\Rightarrow$Low linearity, Low SNDR

Influence of the offset voltage

ENOB is deteriorated by the offset voltage.



$$ENOB = N - \frac{1}{2}\log_2\left[1 + 12\left(\frac{V_{off}(\sigma)}{V_q}\right)^2\right]$$

N : Resolution [bit]
$V_{off}(\sigma)$: Offset voltage @ 1sigma
V_q : 1 LSB ideal voltage

V_q=15.6 mV @ 1Vp-p

$V_{off}(\sigma)$ < 3.9 mV
(ENOB > 5.6 bit)

1bit down @$V_{off}(\sigma)$ = 1/2 LSB

Conventional Offset Cancellation

- **Using pre-amplifiers with offset cancellation techniques**
  - **High voltage gain, wide bandwidth amplifier is needed**
  - **Consume static power**
- **Digital calibration techniques [2]**
  - **Dynamic circuit, no static power**
  - **Accuracy is limited by the resolution of calibration DAC**
  - **Calibration is executed before operation**

We propose the zero static power dynamic offset cancellation technique.

[2] G. Van der Plas, et al., ISSCC 2006.

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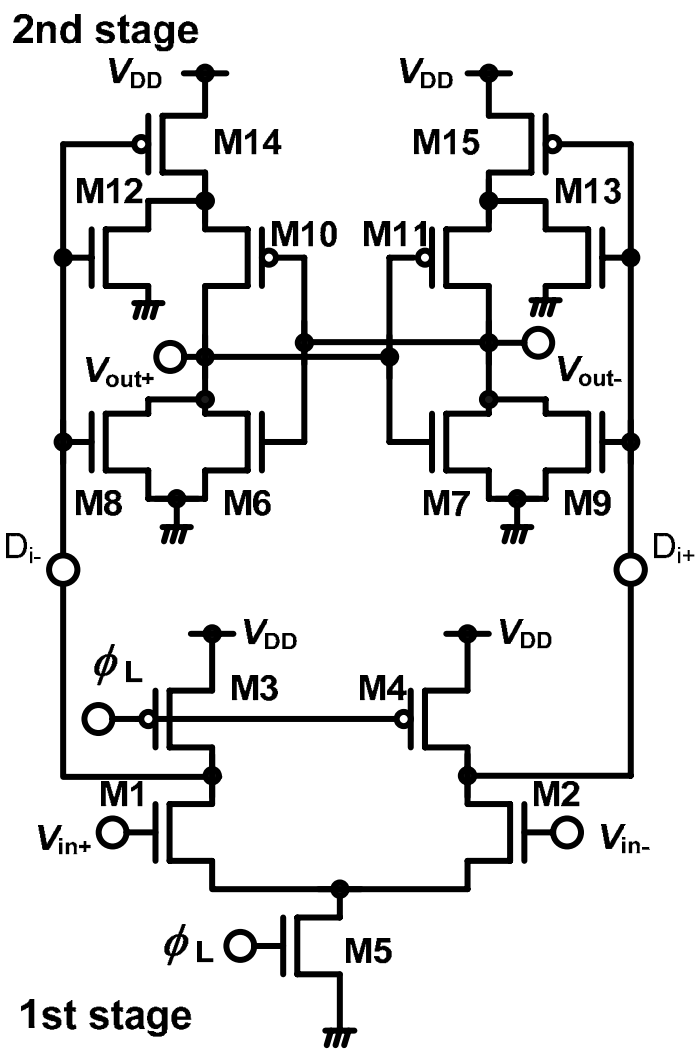
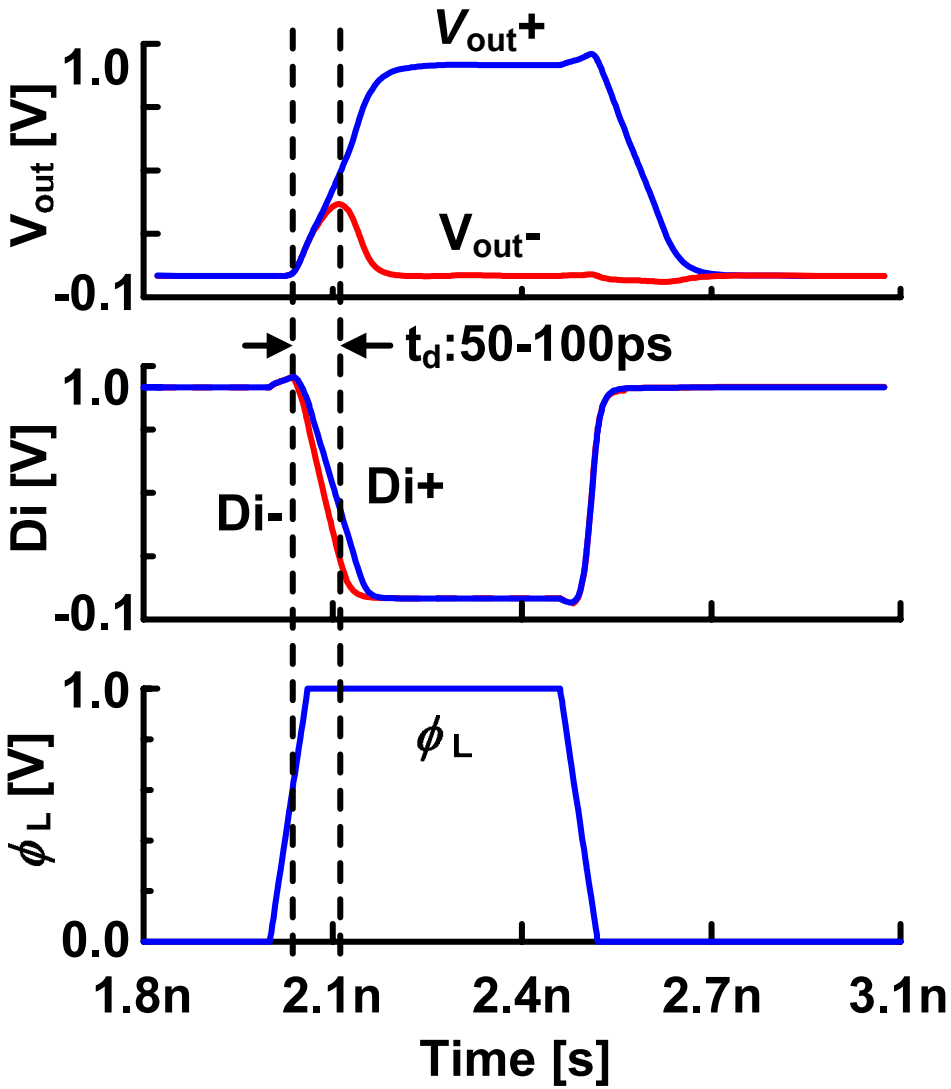
Double-tail Latched Comparator

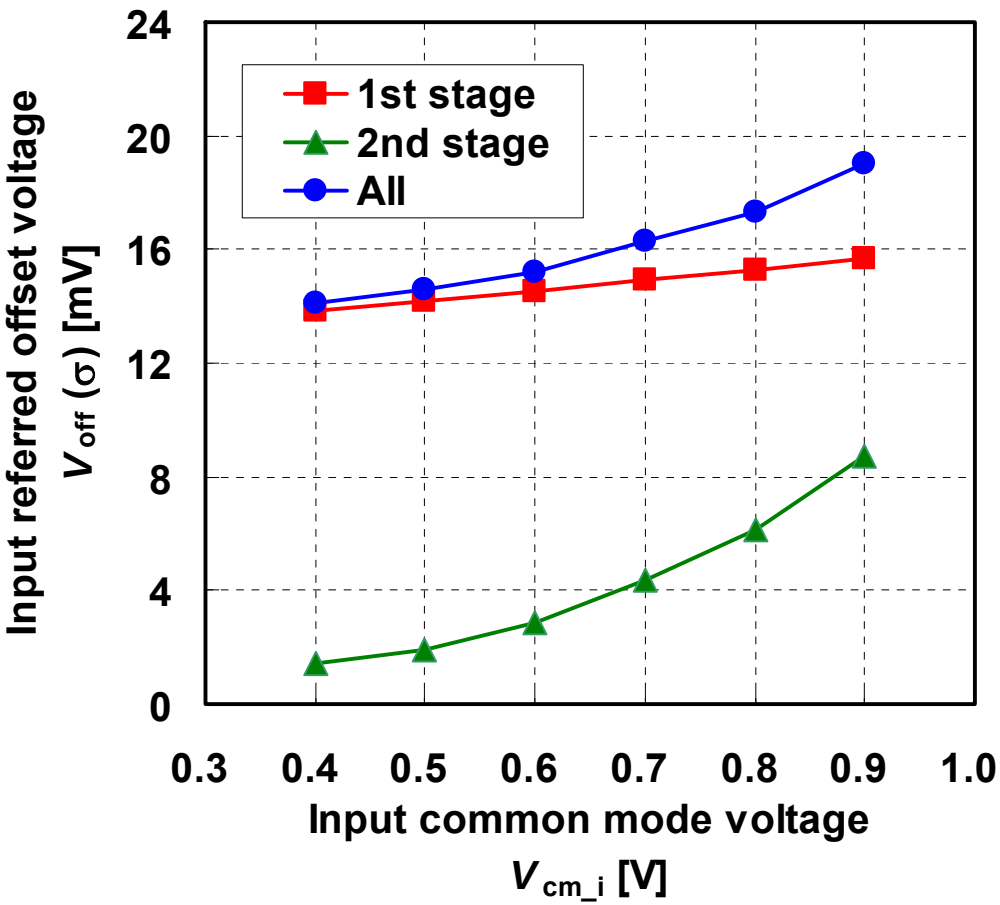




M.Miyahara, A-SSCC 2008.

Offset voltage contribution

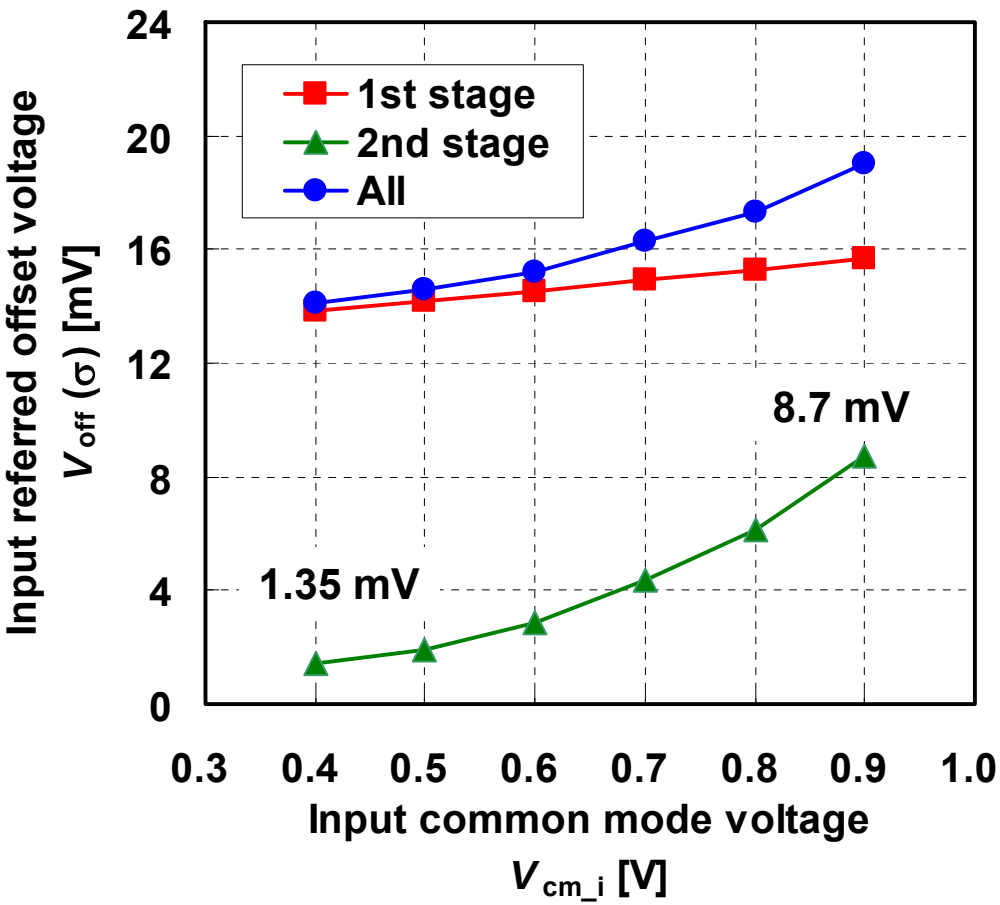
Each stage's contribution to the offset voltage obtained from Monte-Carlo simulation.



- 90nm CMOS process
- W/L = 1 μm / 0.1 μm
- V_{DD} = 1.0 V
- f_c= 500 MHz

Offset voltage contribution

Each stage's contribution to the offset voltage obtained from Monte-Carlo simulation.



- Mismatch of the 1st stage transistors becomes dominant

- The most of the offset voltage of the 1st stage is input transistor's threshold voltages (V_T)

- Input common mode voltage (overdrive voltage of the input transistors) should be kept low

Design Concept

- The V_T mismatch of the input transistors must be canceled.
- The overdrive voltage of the input transistors should be decided without being affected by the input common mode voltage.
- An offset cancellation circuit must be realized without static current for low power operation.

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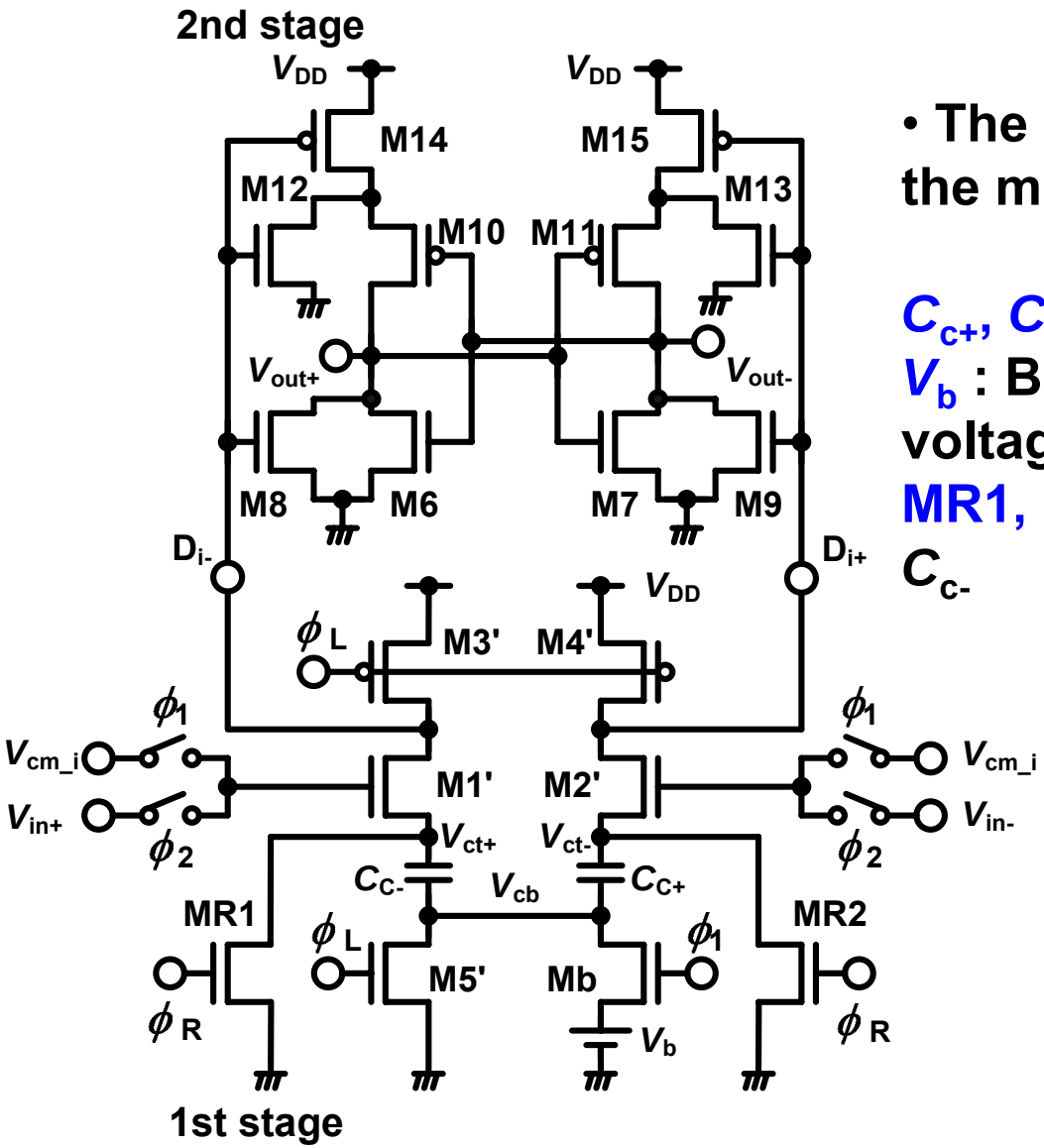
Proposed Comparator



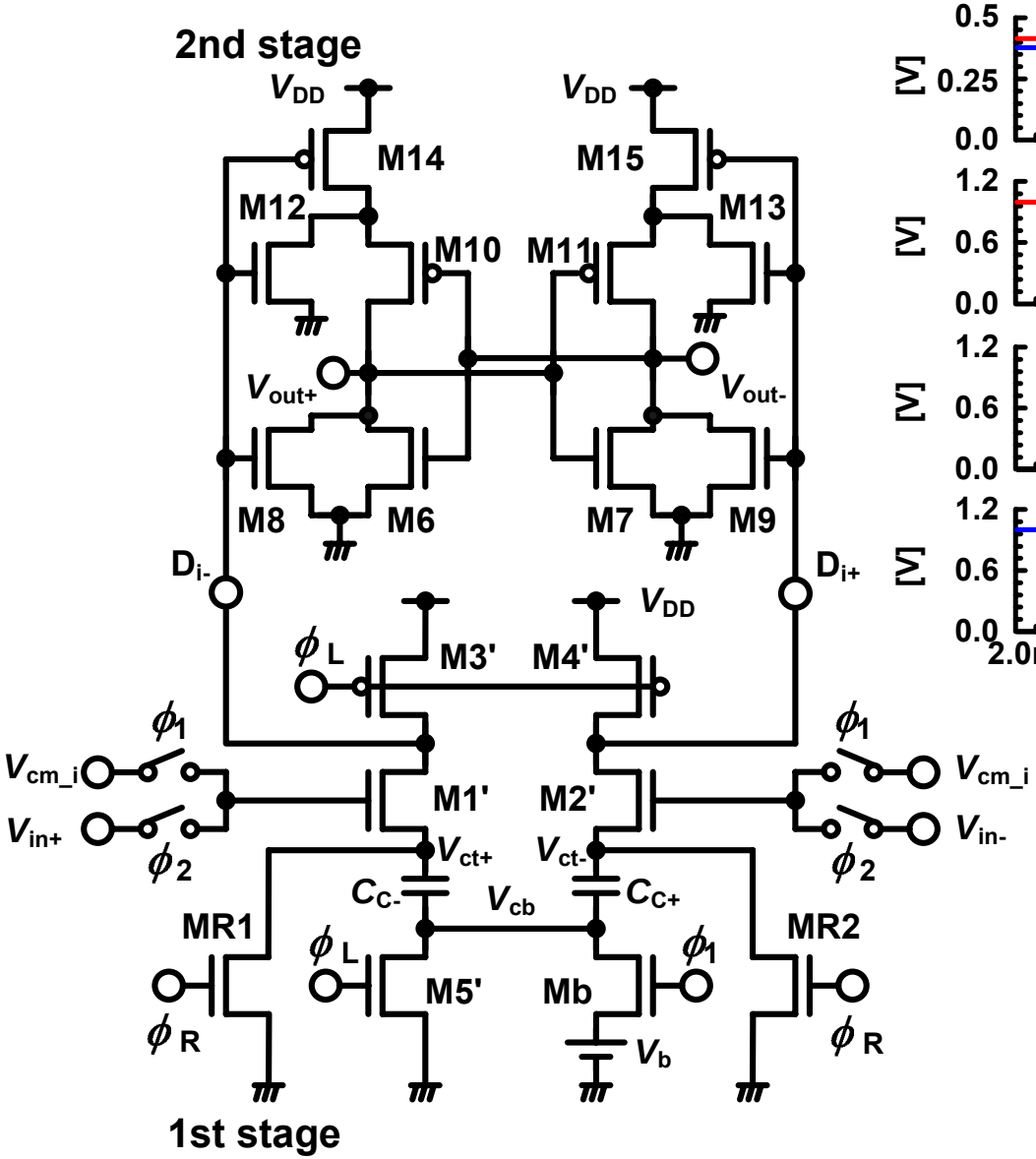
- The 1st stage is modified to cancel the mismatch voltage.

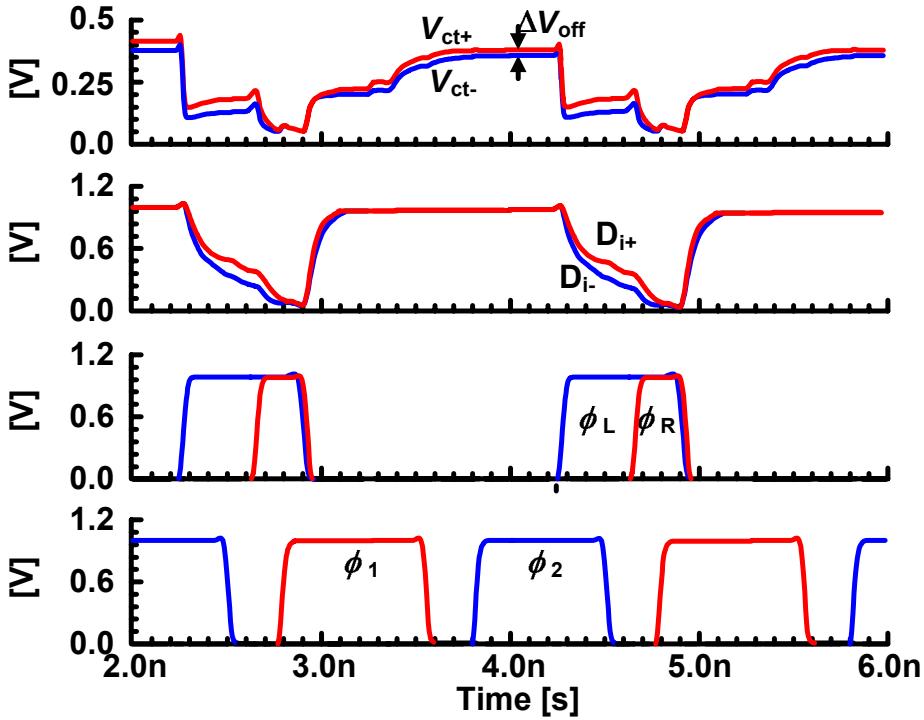
C_{c+}, C_{c-} : Offset canceling capacitor

V_b : Bias voltage to set the overdrive voltage of M1' and M2'

MR1, MR2 : Switches to reset C_{c+} and C_{c-}

Proposed Comparator Behavior





$$V_{c+} - V_{cb} \approx V_{cm\_i} - V_{th1} - V_b$$

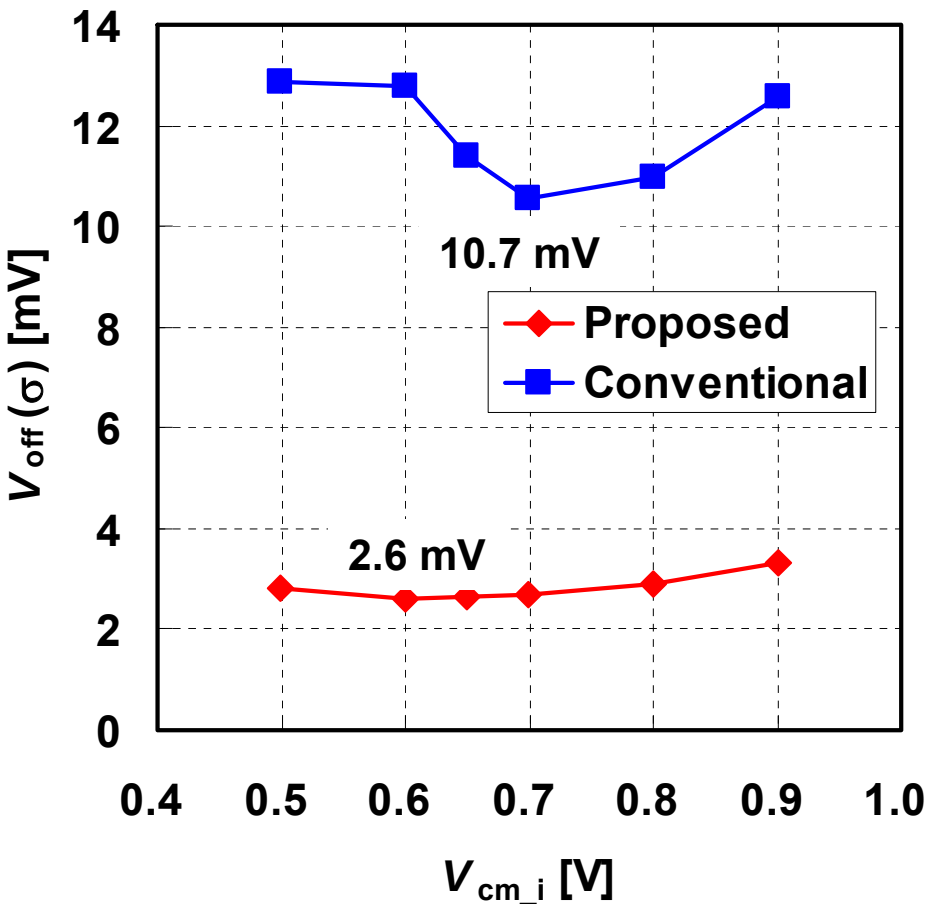
$$V_{c-} - V_{cb} \approx V_{cm\_i} - V_{th2} - V_b$$

$$V_{od1} = \Delta V_{in} + V_b$$

$$V_{od2} = -\Delta V_{in} + V_b$$

Simulation Results : V_{cm_i} Variation

Proposed comparator can suppress increase of offset voltage caused by V_{cm_i} variation.

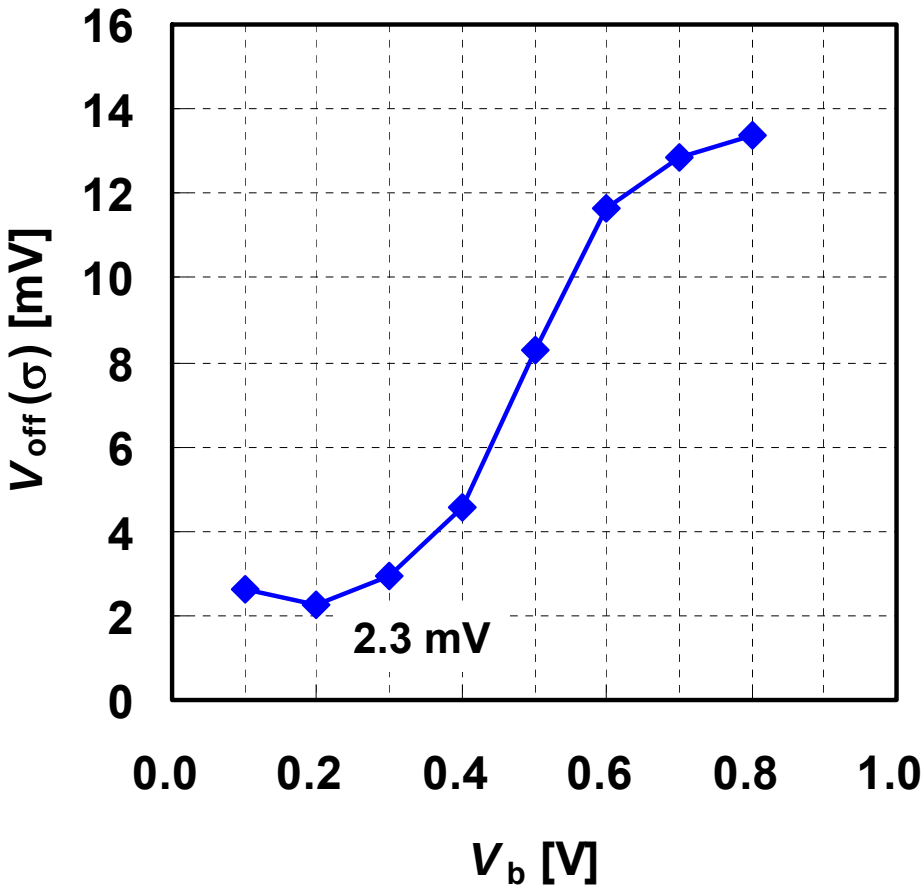


- 90nm CMOS process
- V_{DD} = 1.0 V
- V_b = 0.1 V
- f_c= 500 MHz

- All transistor channel length is minimized.
- Each transistor channel width is optimized for fast latching.

Simulation Results : V_b Variation

The bias voltage V_b had better to be set low. However, too much small overdrive voltage causes a deterioration of the latch speed.



- 90nm CMOS process
- V_{DD} = 1.0 V
- V_{cm_i} = 0.6 V
- f_c= 500 MHz

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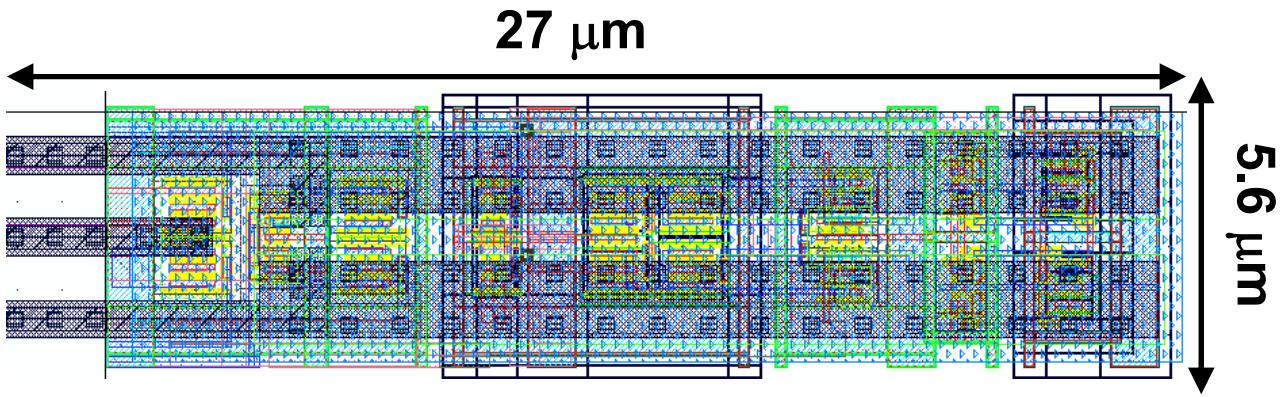
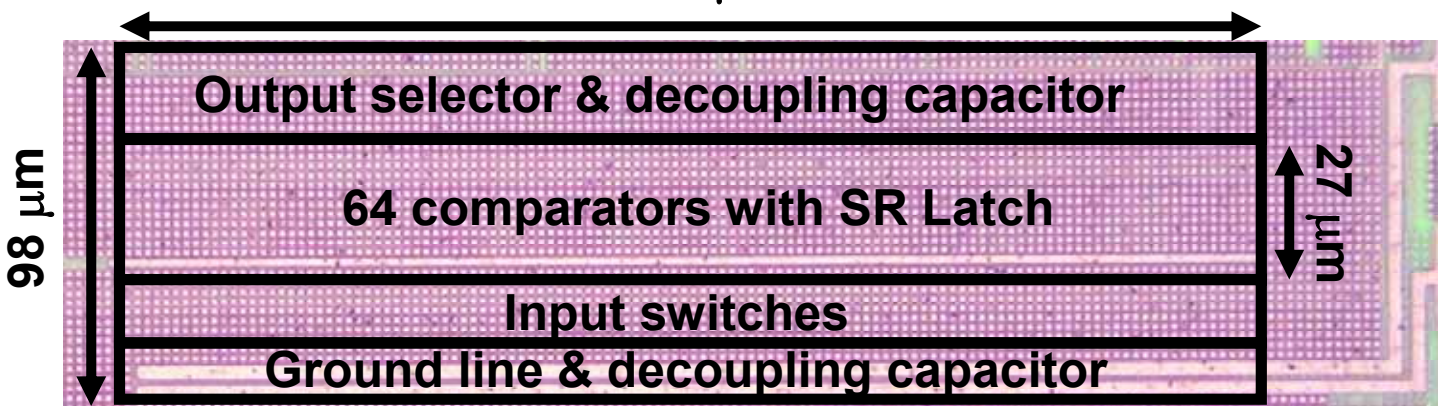
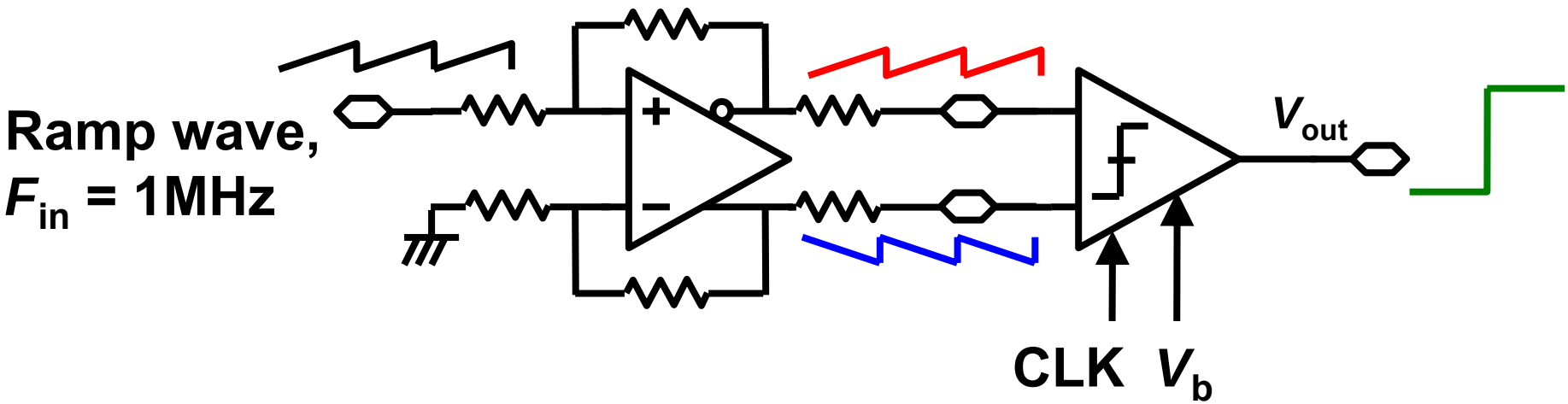
Layout

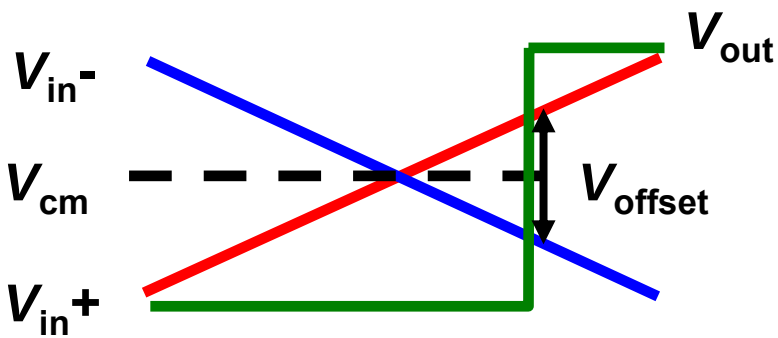
A prototype comparator has been realized in a 90 nm 9M1P CMOS technology with a chip area of 0.0354mm^2. The core comparator size is only 152 μm^2.





Measurement System

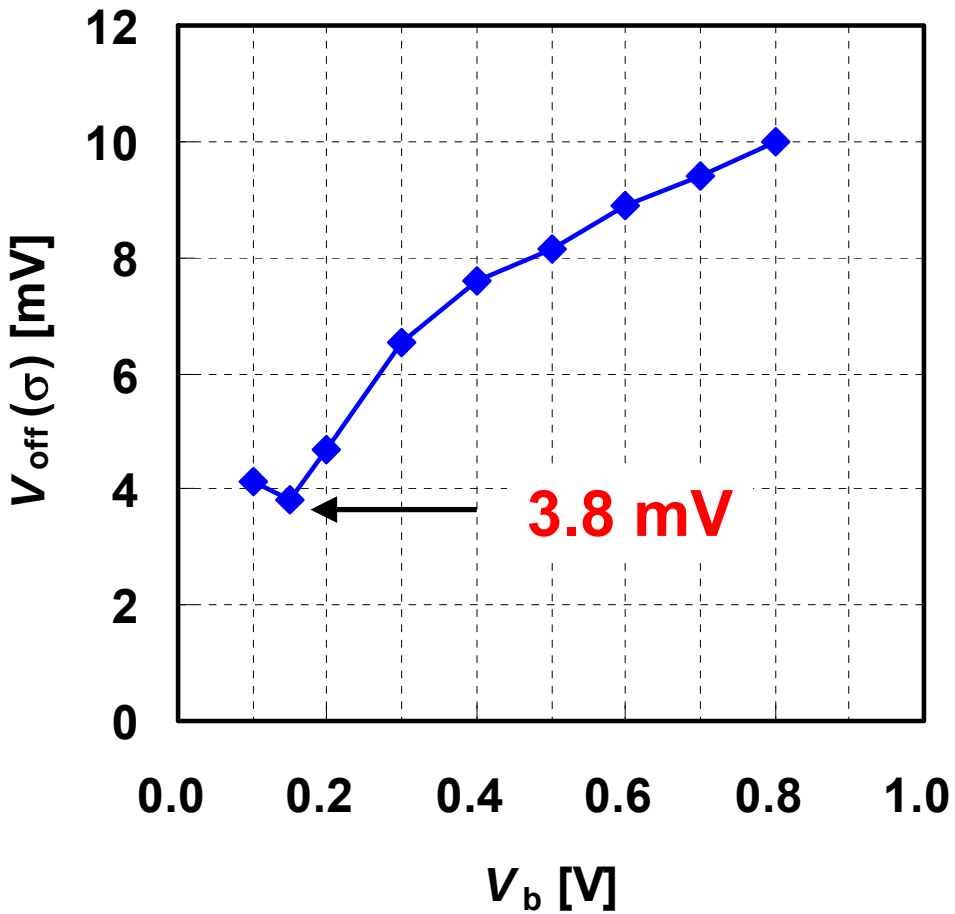




The offset voltage is the input voltage at the point that output changes from low to high.

Measurement Results: V_b Variation

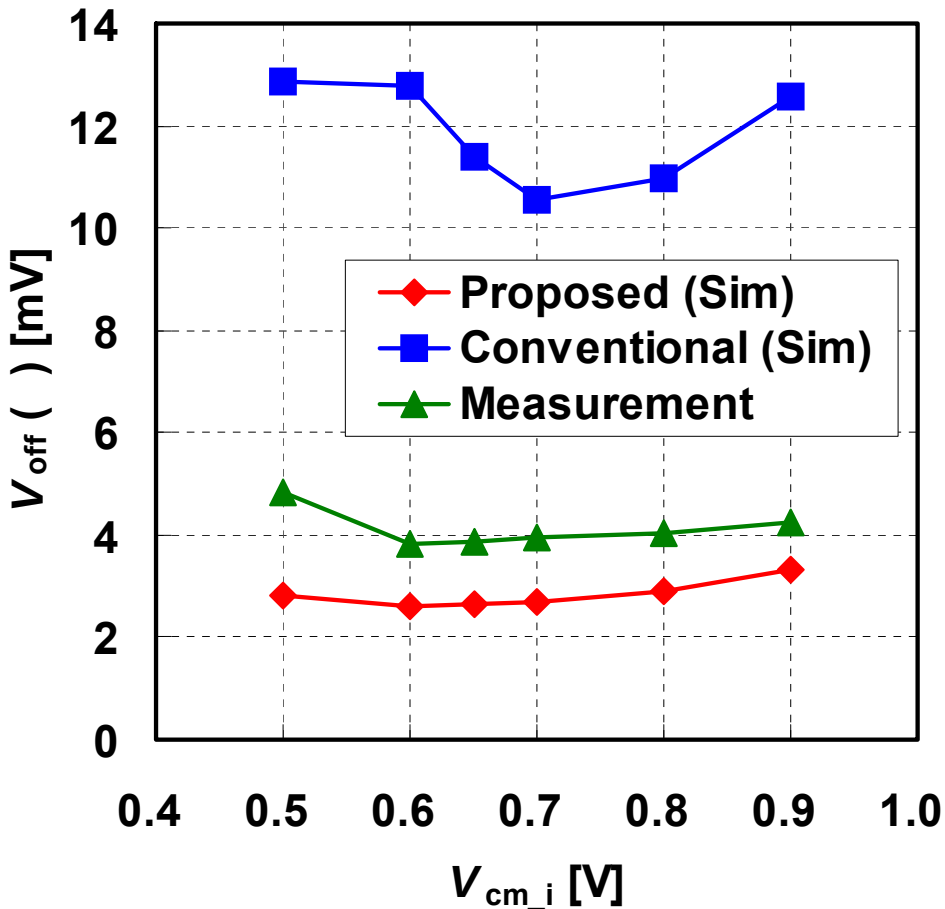
The offset voltage can be minimized in case of V_b= 0.15 V.



- V_{DD} = 1.2 V
- V_{cm_i} = 0.6 V
- f_c= 500 MHz

Measurement Results: V_{cm_i} Variation

The offset voltage increases by only 0.4 mV when V_{cm_i} changes from 0.6 V to 0.9 V.



- The measured offset voltage is slightly higher than simulation result.
  => Dummy metals affect to mismatch

Performance Summary

Technology	90nm, 1poly, 9metals CMOS
Active Area	5.6µm x 27µm (core comparator)
$V_{offset}(\sigma)$	3.8 mV (ENOB = 5.6 bit @ 1Vp-p)
Supply Voltage	1.2 V
Power consumption	4.8mW @ 500 MHz *

* Power consumption includes 64 comparators, I/O buffers and clock drivers.
Simulated power consumption of the comparator is 68 µW/GHz.

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Conclusion

A low offset voltage dynamic latched comparator using a zero-static power dynamic offset cancellation technique is proposed.

☺ **Features**

- **The proposed comparator consumes no static power.**
- **Measured results show the input offset voltage is improved from 12.8 mV to 3.8 mV by using proposed technique.**
- **The offset voltage of the comparator does not change by increasing the input common mode voltage.**

Thank you for your interest!

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