A 0.9-3.0 GHz Fully Integrated CMOS Power Amplifier for Multi-Band Transmitters

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Outline

- Introduction
- PA design
- Measurement results
- Conclusion

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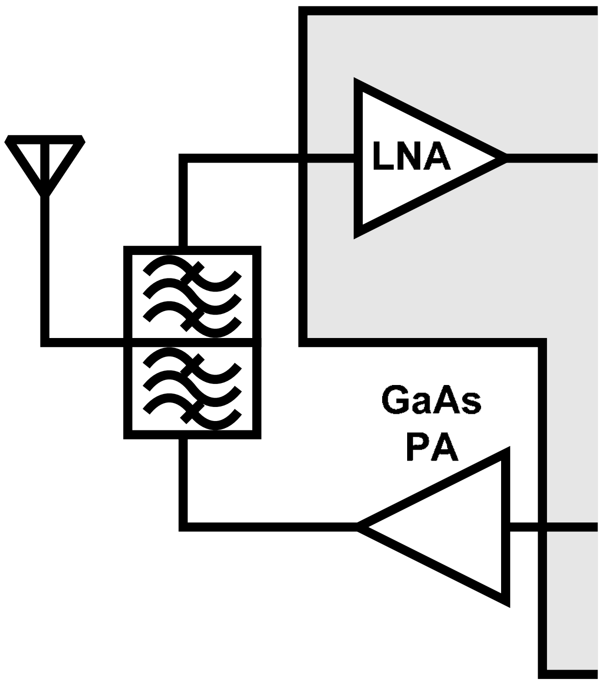
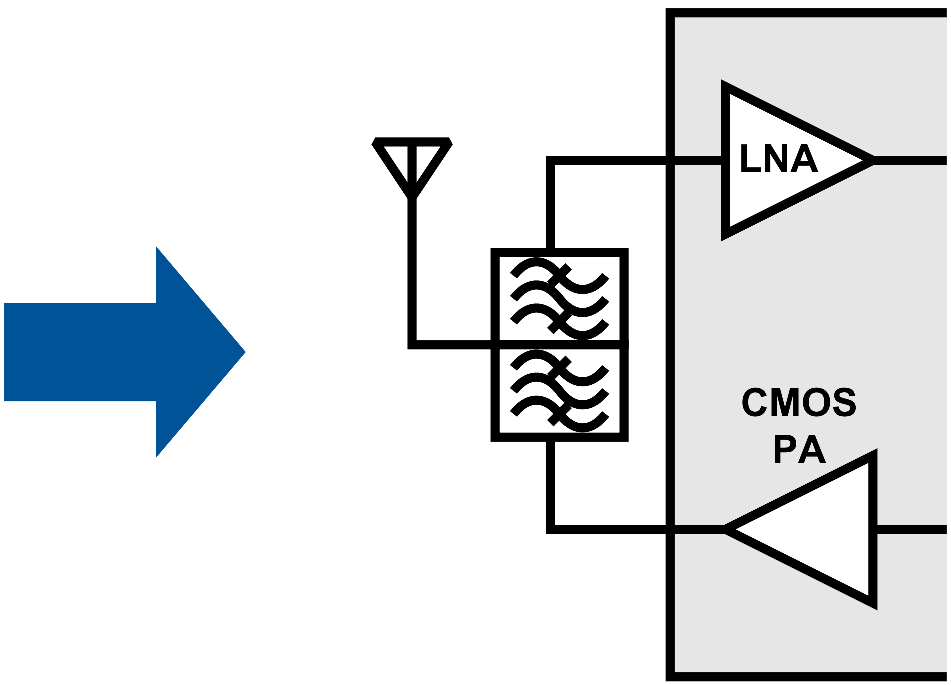
Single chip transceiver

- **Now**

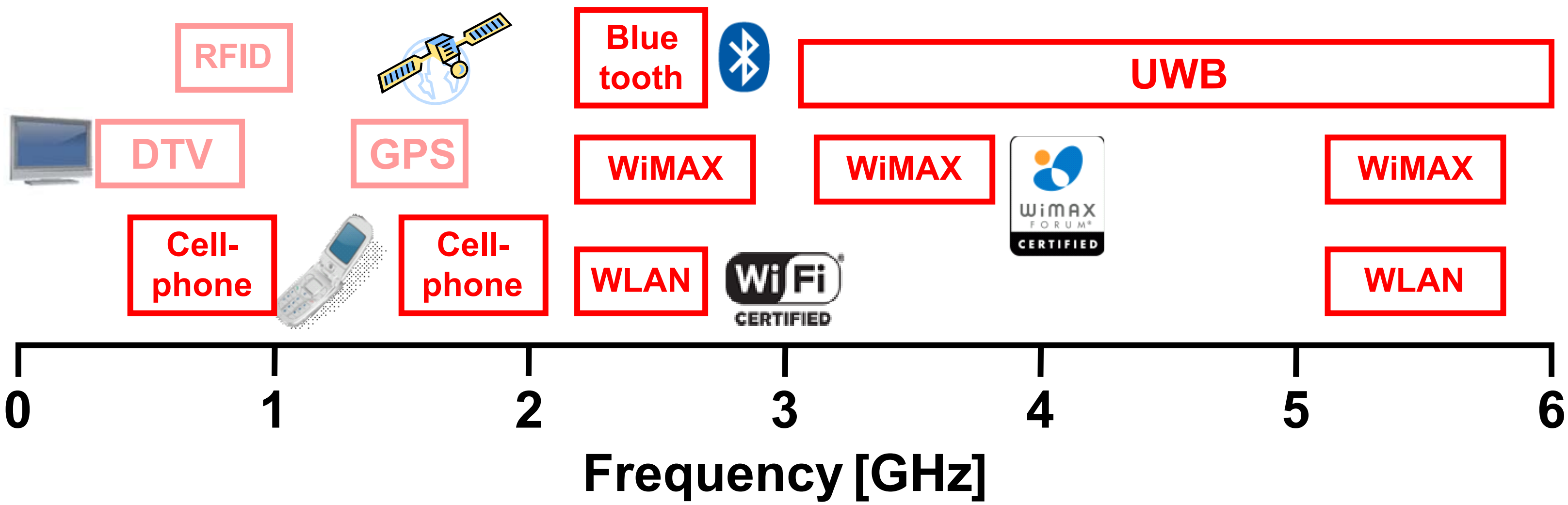


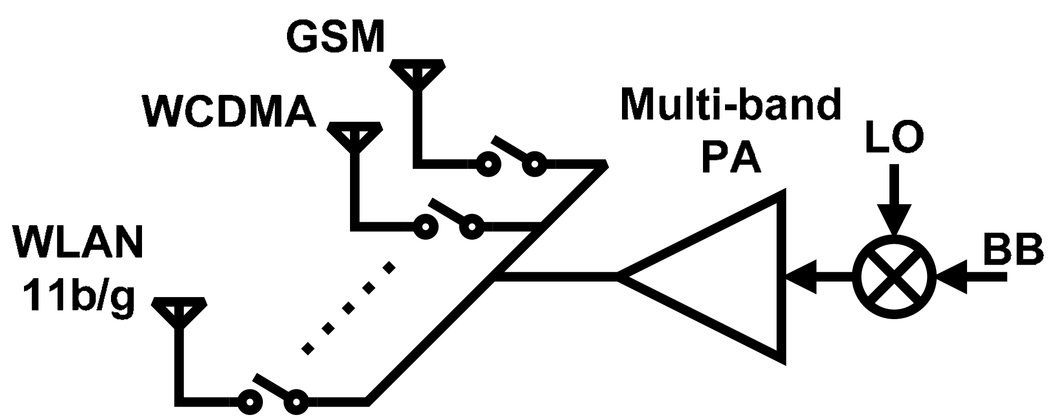
- **Future**



- **Conventionally, PA is fabricated in compound semiconductor such as GaAs**
- **Recently, CMOS PA is under hot debate to realize single chip transceiver**

Multi-band transmitter





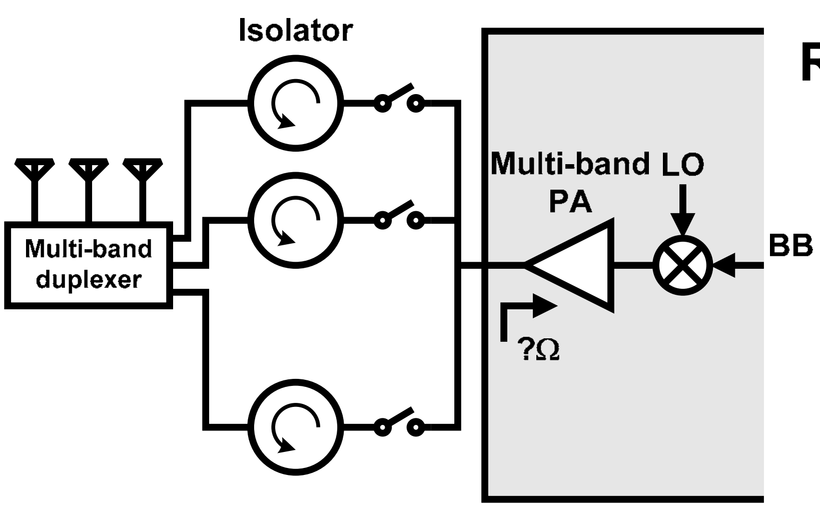
The target of this work is to cover multiple wireless standards with only one CMOS PA

Isolator-less transmitter

- **Function of isolators**
  - Maintain PA's output impedance 50Ω
  - Protect PAs from reflected wave

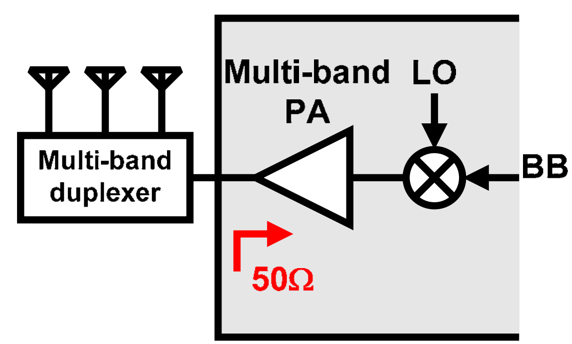
Isolators can be removed if PAs have 50Ω output impedance

- **Conventional**



Reducing off-chip component

- **Proposed**



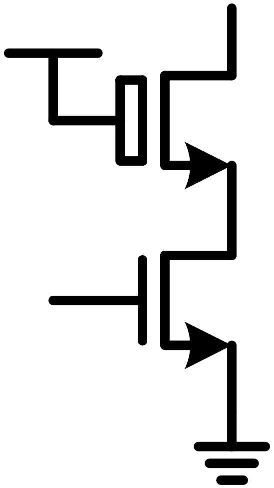
Challenges of CMOS PA

- Low breakdown voltage of transistor
  - In submicron CMOS process, V_{DD}=1~2V
  - Output power $\propto$ $(\text{Voltage})^2$

➡ 10V amplitude for 1W output power

Solution

- Use thick-oxide transistor
- Apply cascode topology and share output voltage



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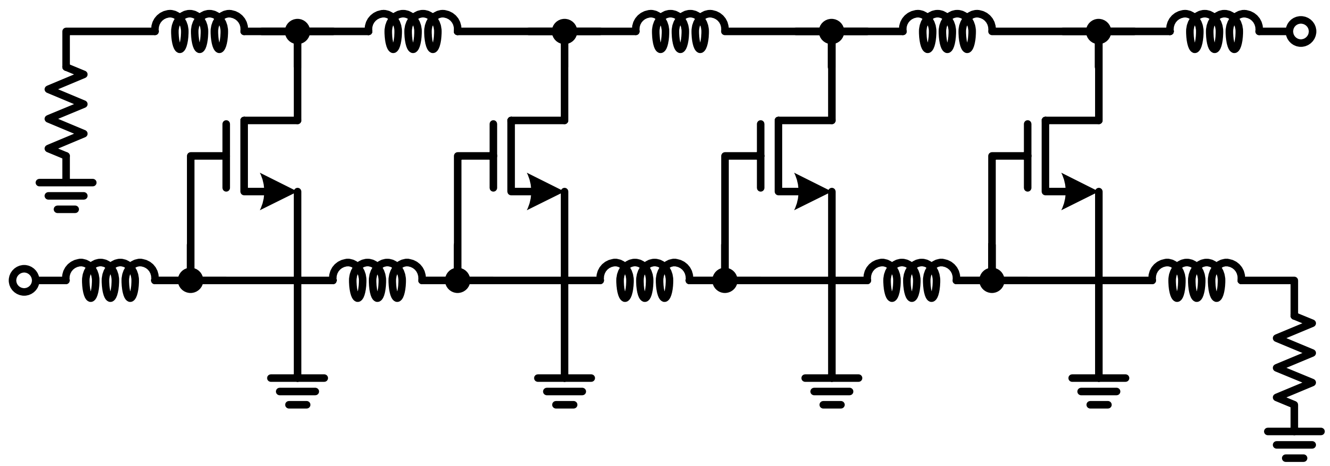
Conventional approach

Distributed amplifier



- ✓ **Wideband input and output matching**
- ✗ **Large chip area**
- ✗ **Small output power due to the absence of impedance transformation**

Output impedance tuning 1

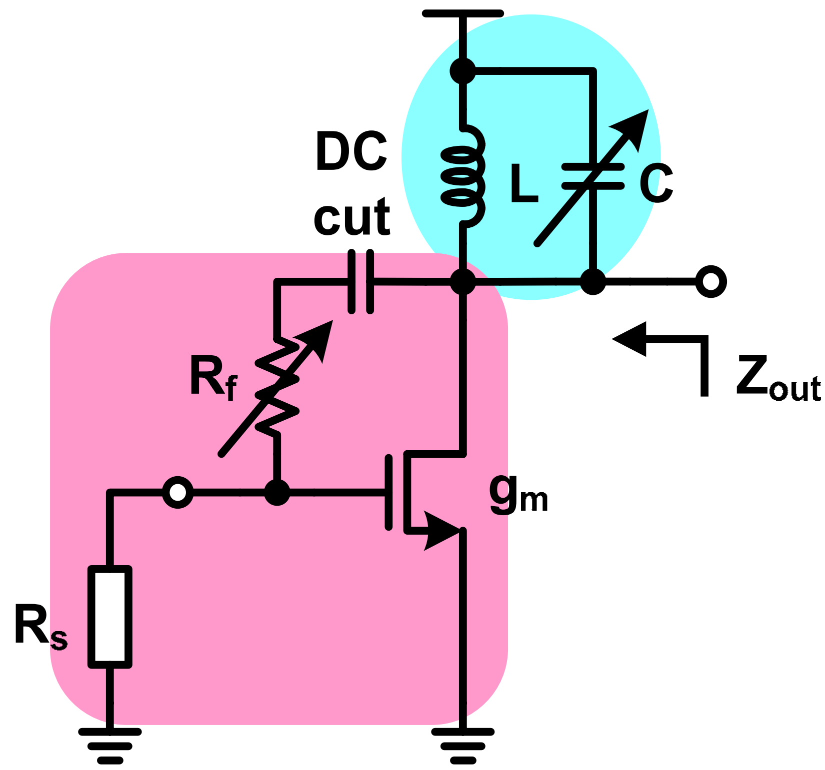
If $r_{ds}=\infty$,

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{1}{j\omega C} // (R_L + j\omega L)$$

When $f = \frac{1}{2\pi\sqrt{LC}}$

(Resonance frequency)

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{L}{CR_L}$$



R_s : source impedance (50Ω)

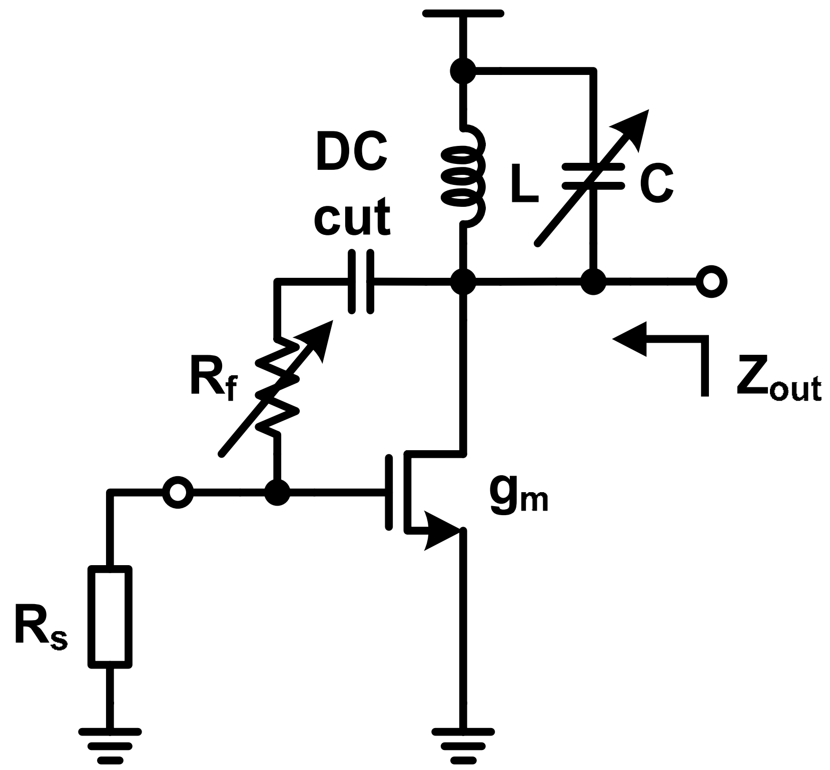
R_L : inductor parasitic resistance

Tune C to cancel imaginary part of Z_{out} at arbitrary frequency

Output impedance tuning 2

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{L}{CR_L}$$

- Tune R_f to match Z_{out} to 50Ω
- Since Z_{out} depends on the value of C, R_f needs to be changed according to the matching frequency

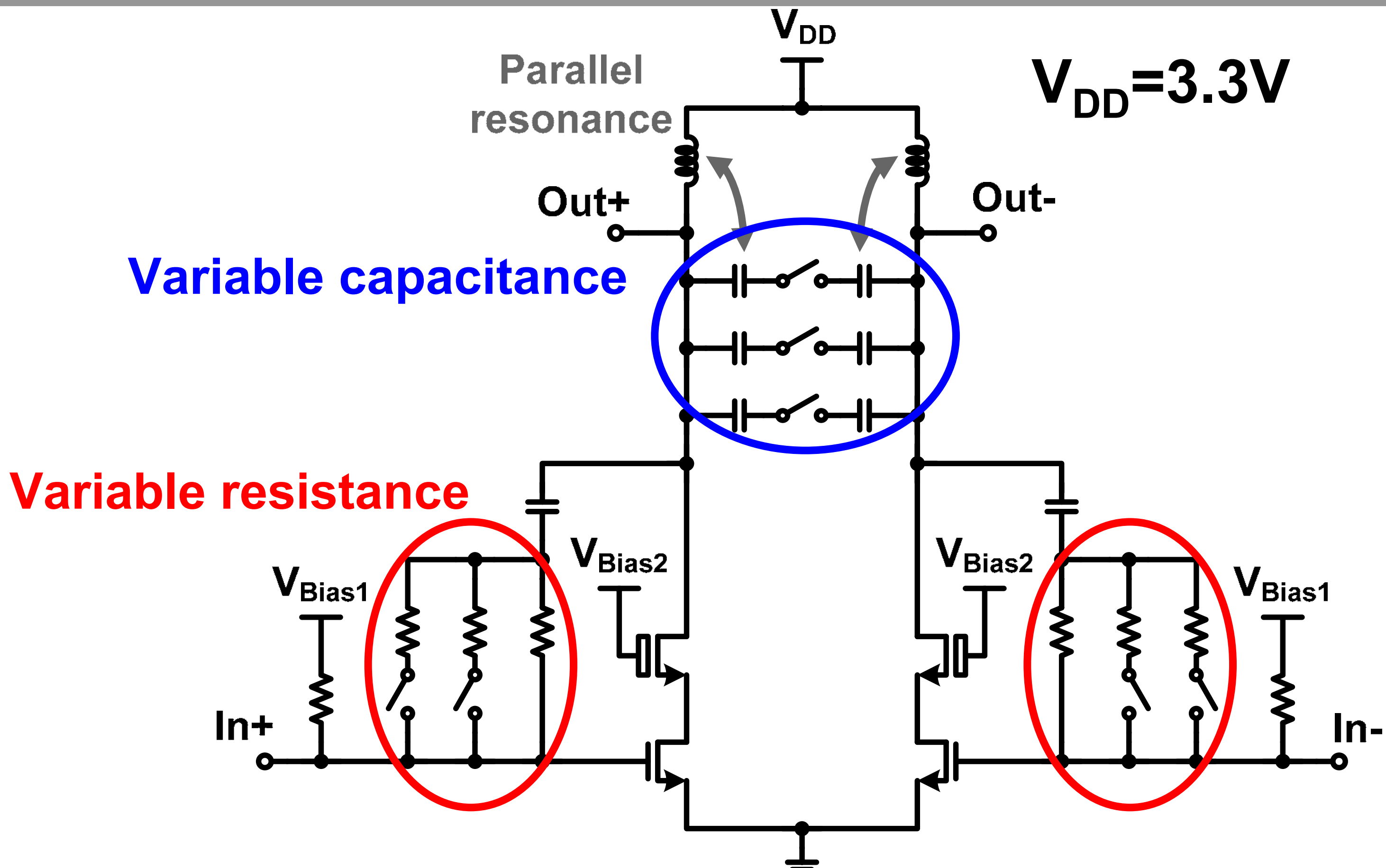


R_s : source impedance (50Ω)

R_L : inductor parasitic resistance

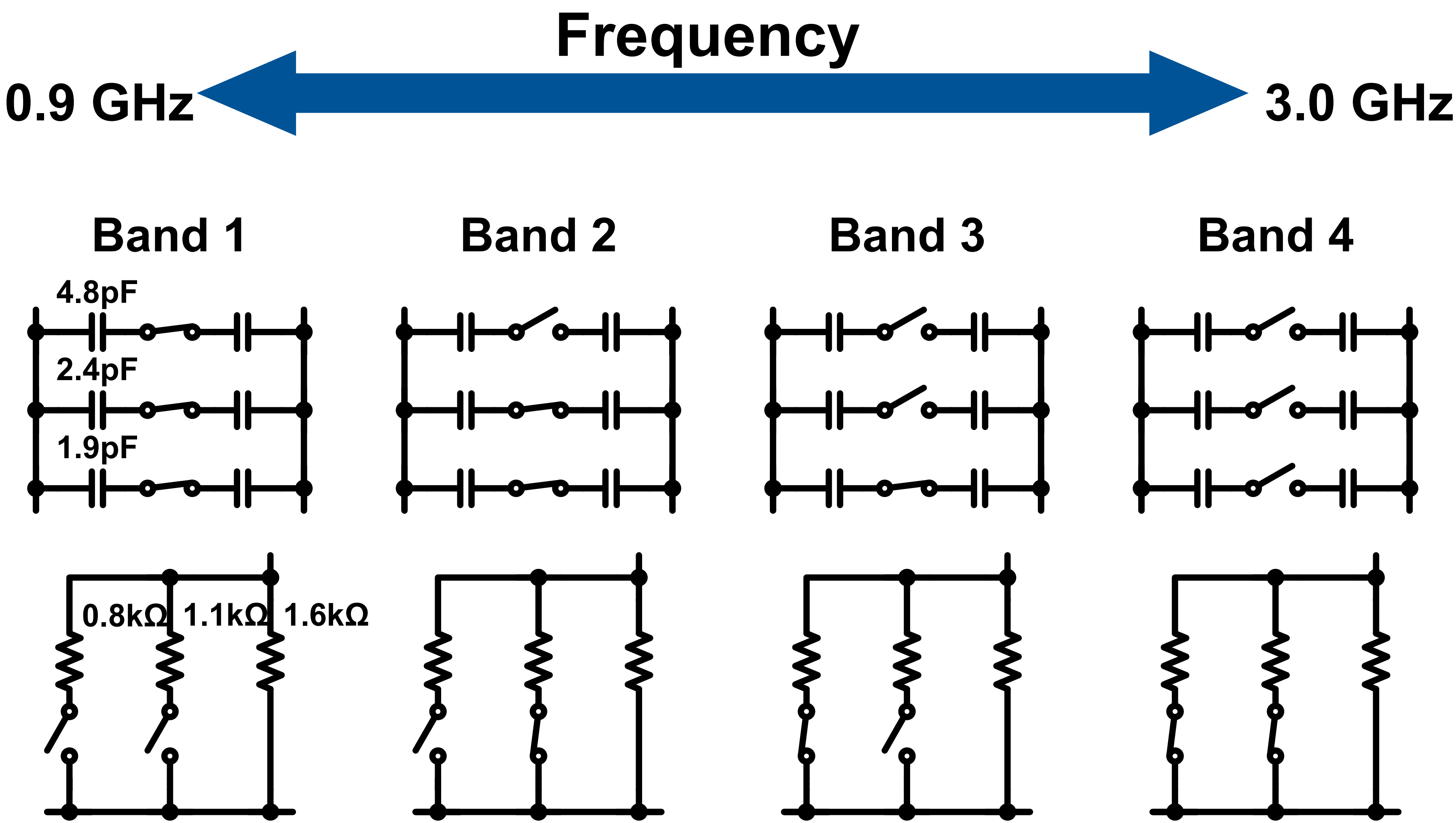
In fact, r_{ds} is small… ➡ Cascode topology is used

Schematic of the proposed PA



- Change output matching band by switching C and R
- Differential topology for 3dB larger P_{sat}
- Class-A bias

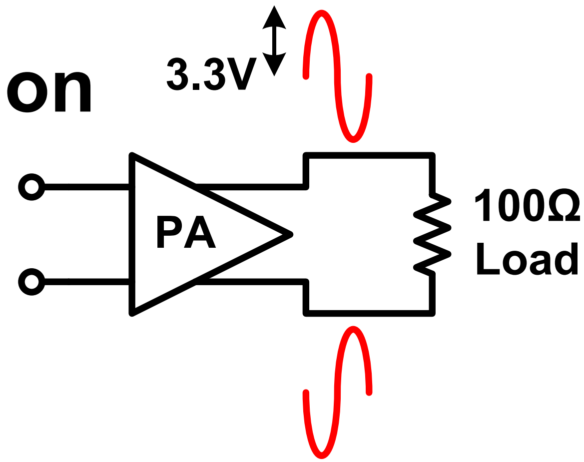
State of switches



Theoretical maximum output power

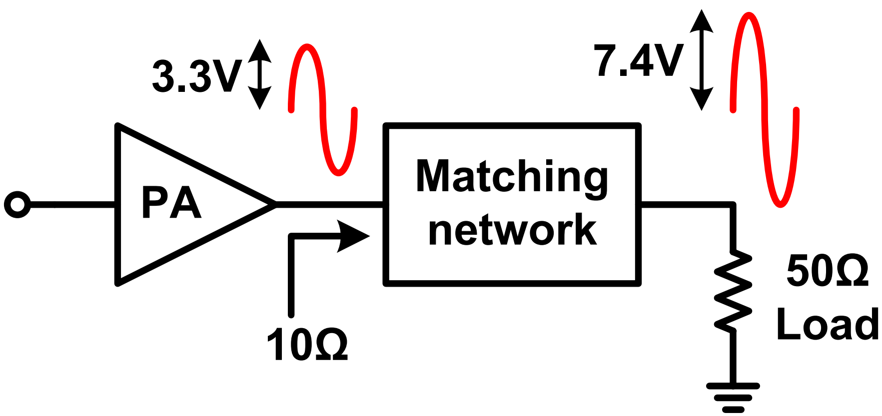
- **Without impedance transformation**

$$P_{sat} = \frac{(6.6V)^2}{2 \cdot 100\Omega} = 0.22W\ (23dBm)$$



- **With impedance transformation**

$$P_{sat} = \frac{(3.3V)^2}{2 \cdot 10\Omega} = 0.54W\ (27dBm)$$

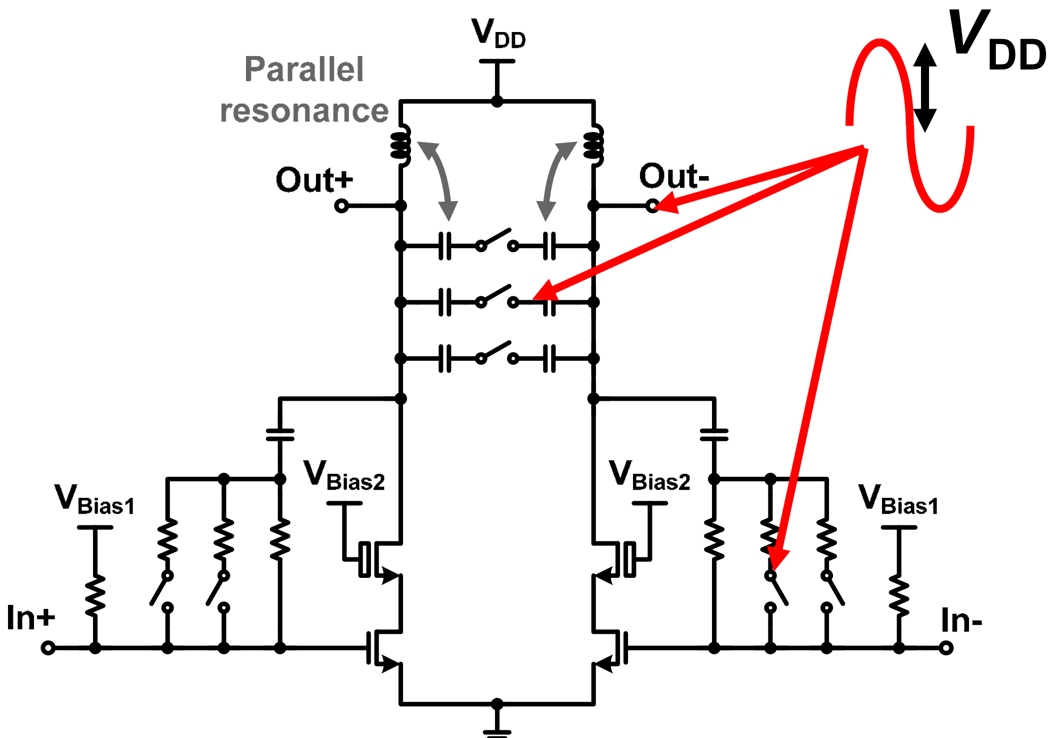


- **Impedance transformation network can enhance the output power, but it is usually narrow-band**
- **23dBm P_{sat} can be achieved due to differential topology and high V_{DD}**

Voltage stress of switches

- Maximum voltage swing at output node is about V_{DD}=3.3V
- The same voltage is applied to switches when they are off

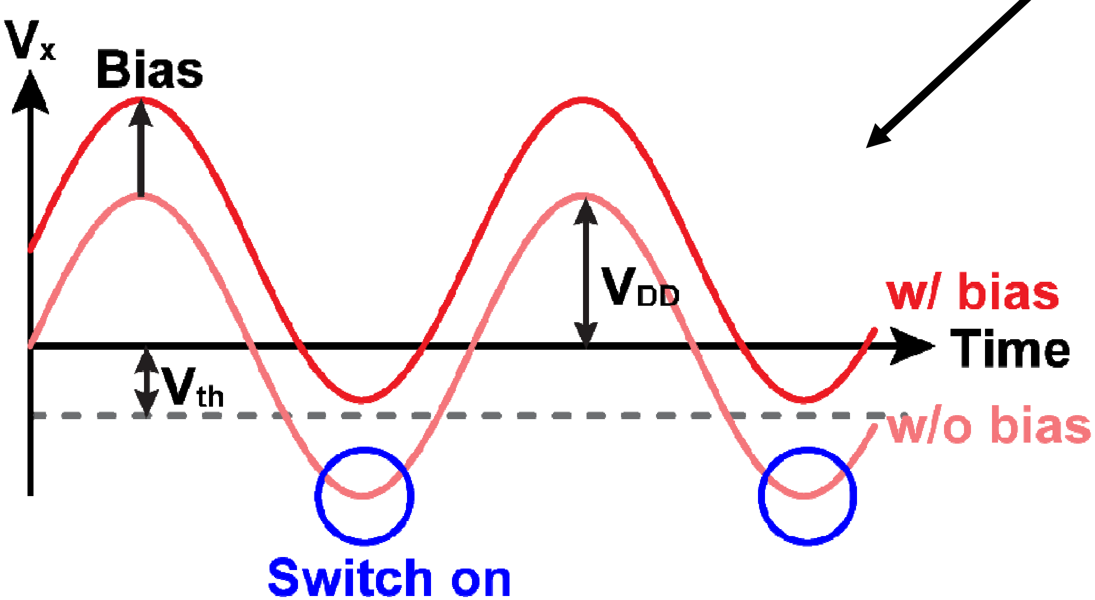
➡ **Thick oxide nMOS is applied as switch**

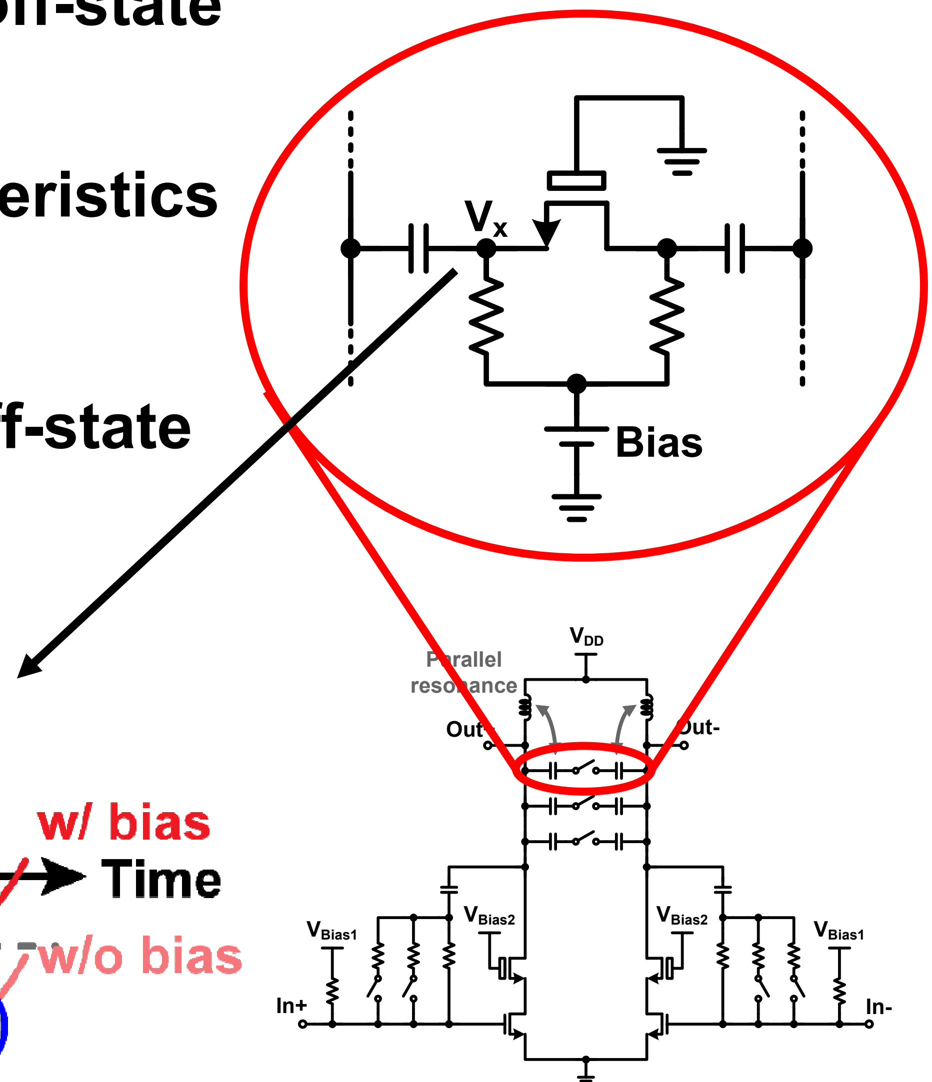


Switch biasing

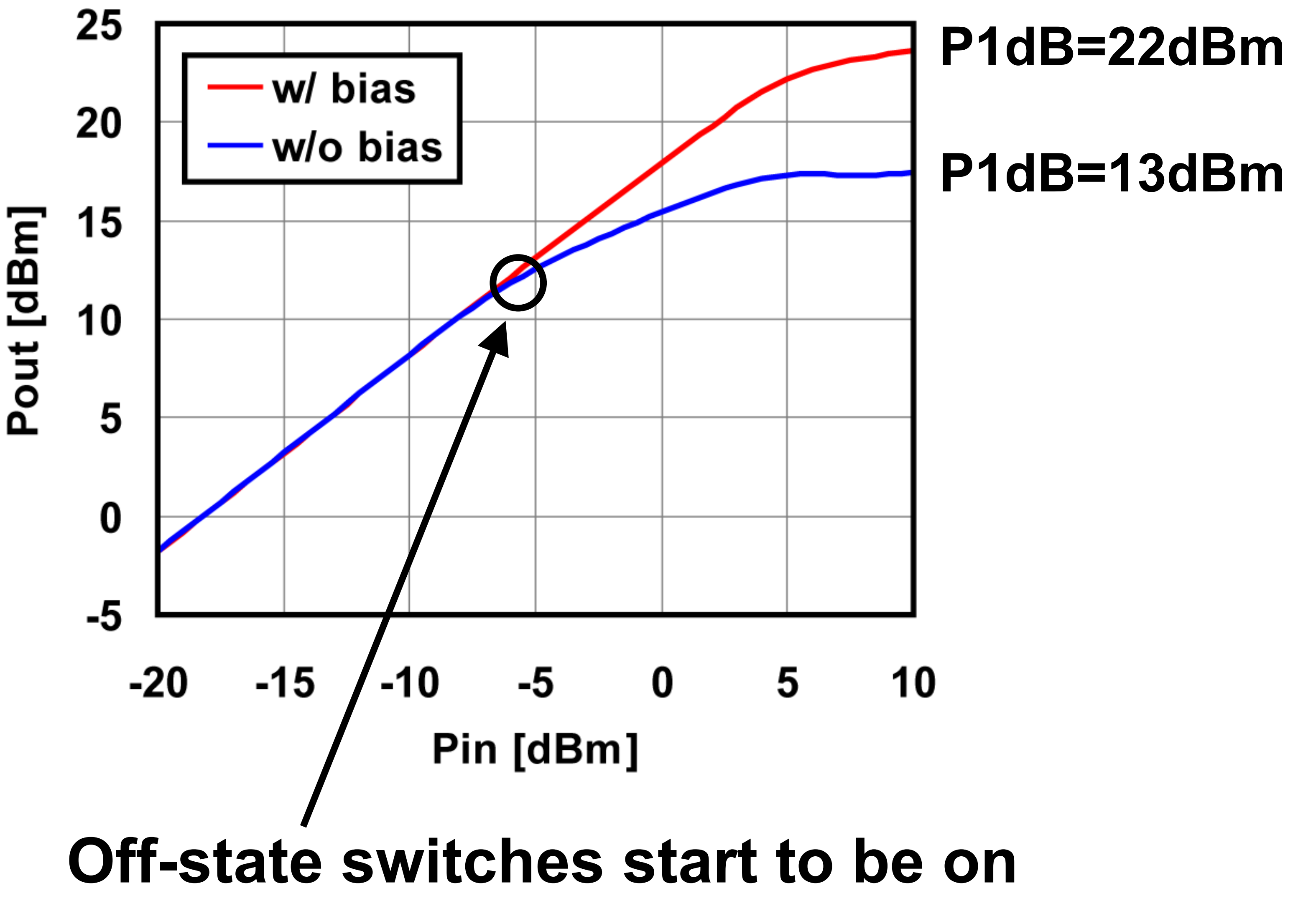
- **Large voltage swing makes off-state switch on for a moment**
- **Degrade large signal characteristics such as P_{1dB}**

Bias to source and drain of off-state switches



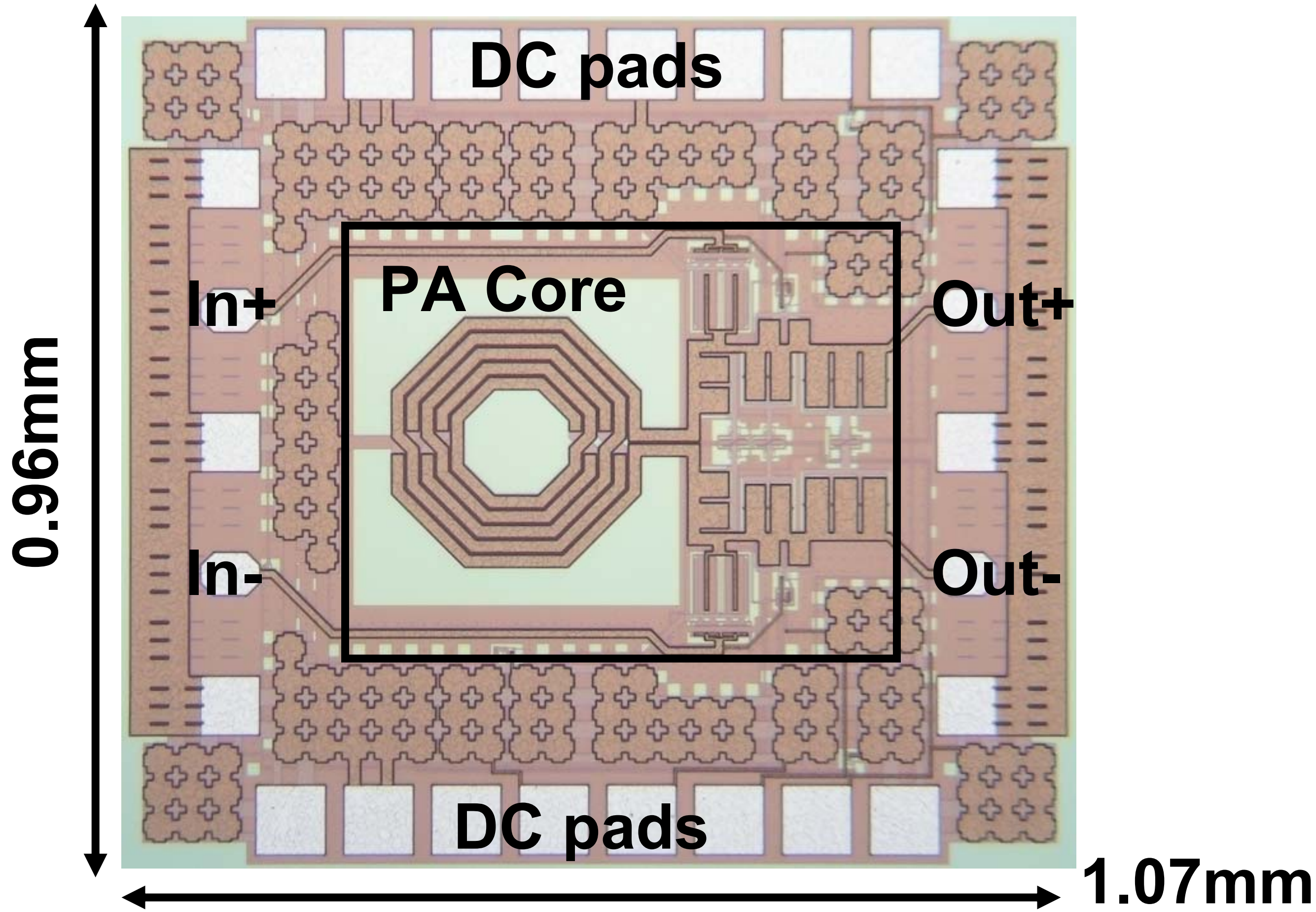


Simulation of switch biasing effect



Chip micrograph

- 0.18μm CMOS
- Chip was measured using probes and external DC block capacitors



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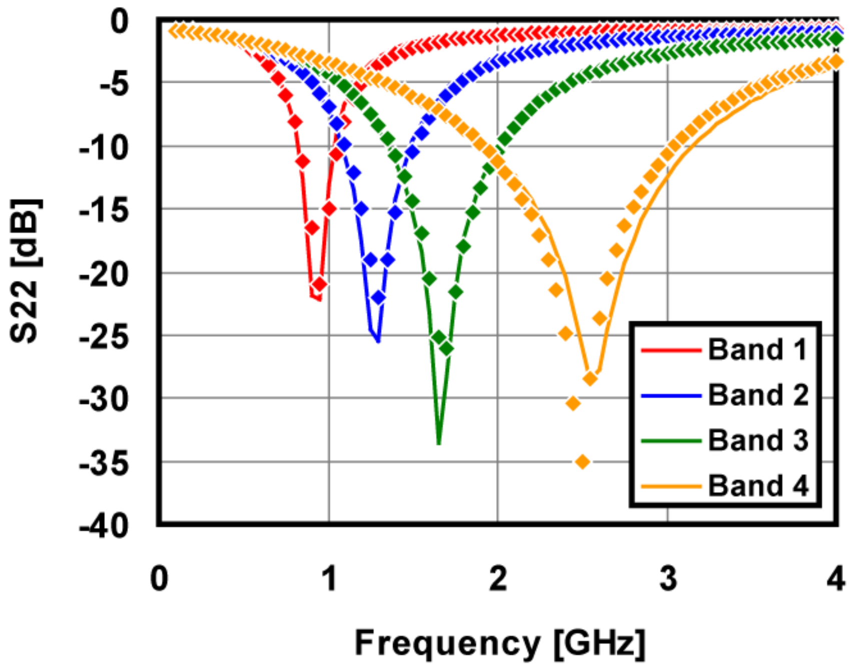
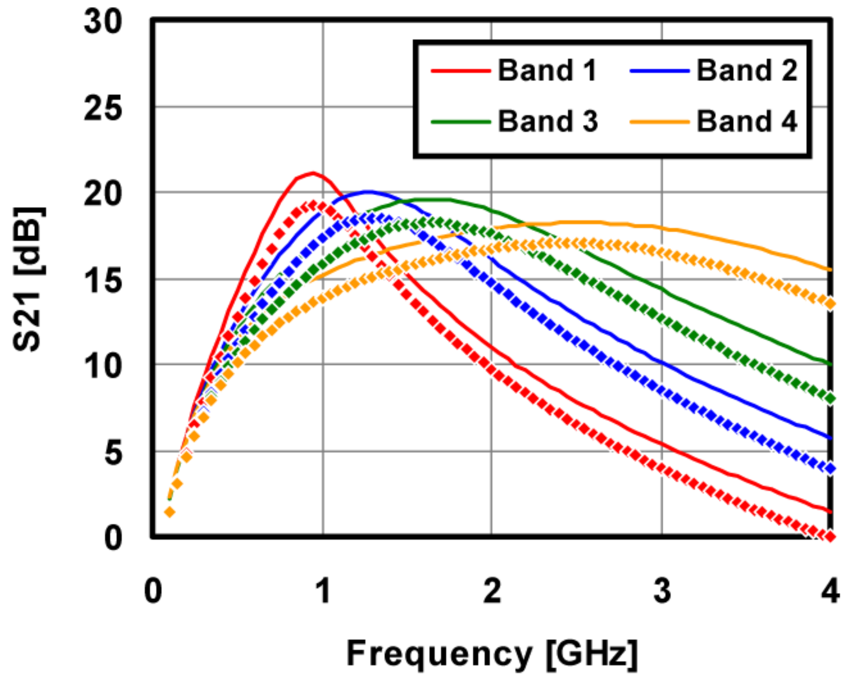
Small signal S-parameters

- Differential-mode S-parameter calculated from 4-port S-parameter

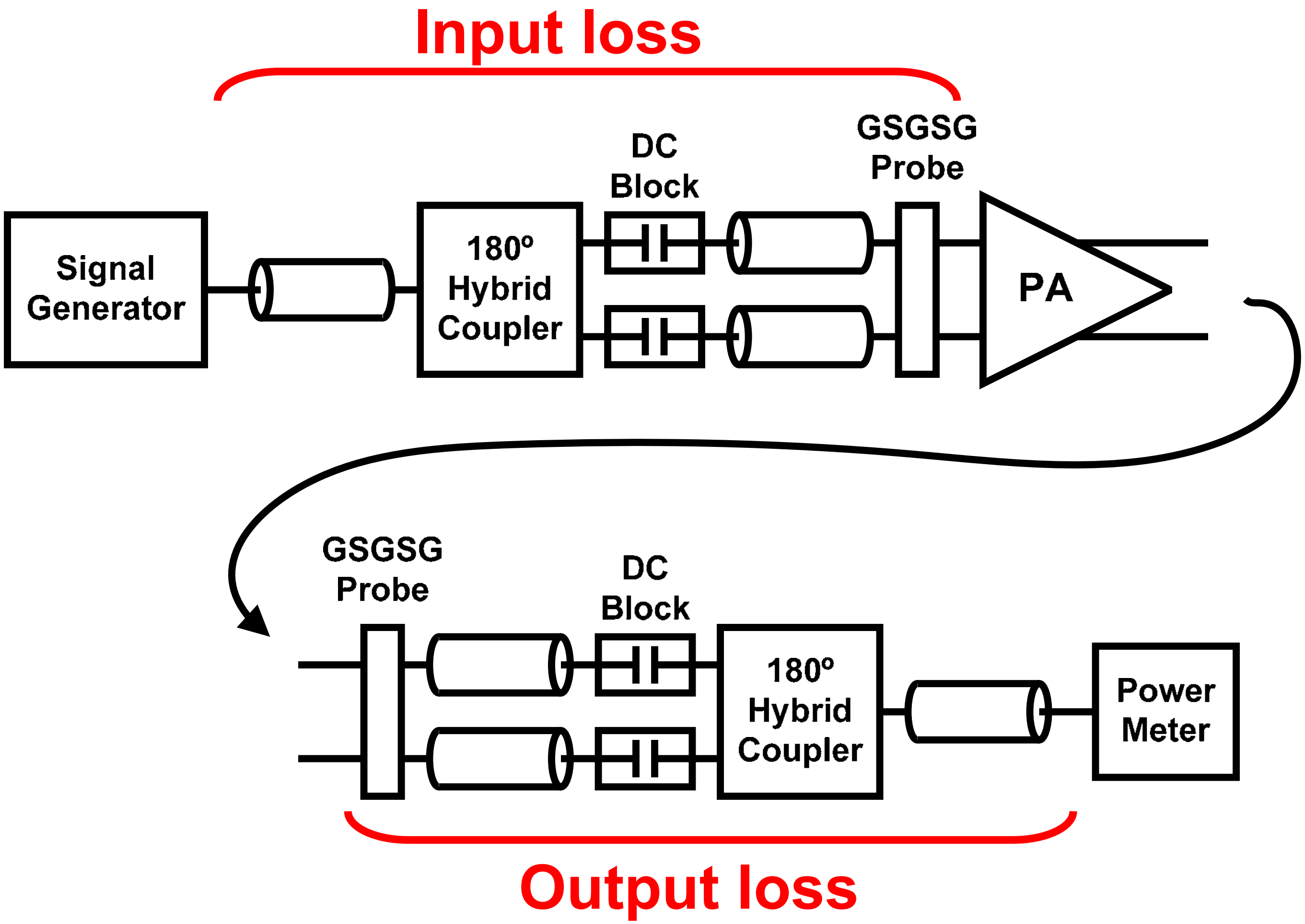
Solid line : Simulation
Marker : Measurement





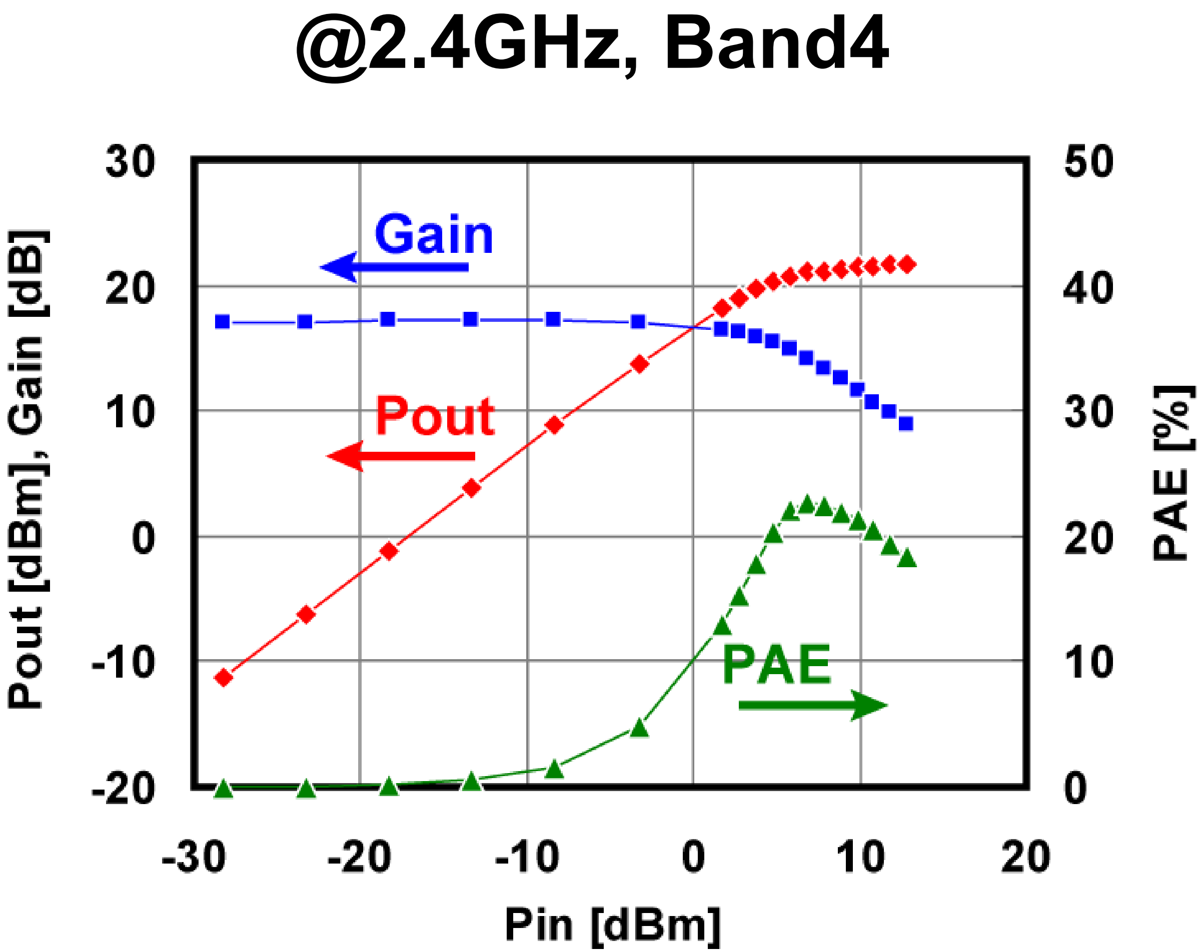
0.9~3.0GHz, S22 < -10dB, S21 > 16dB

Large signal measurement setup



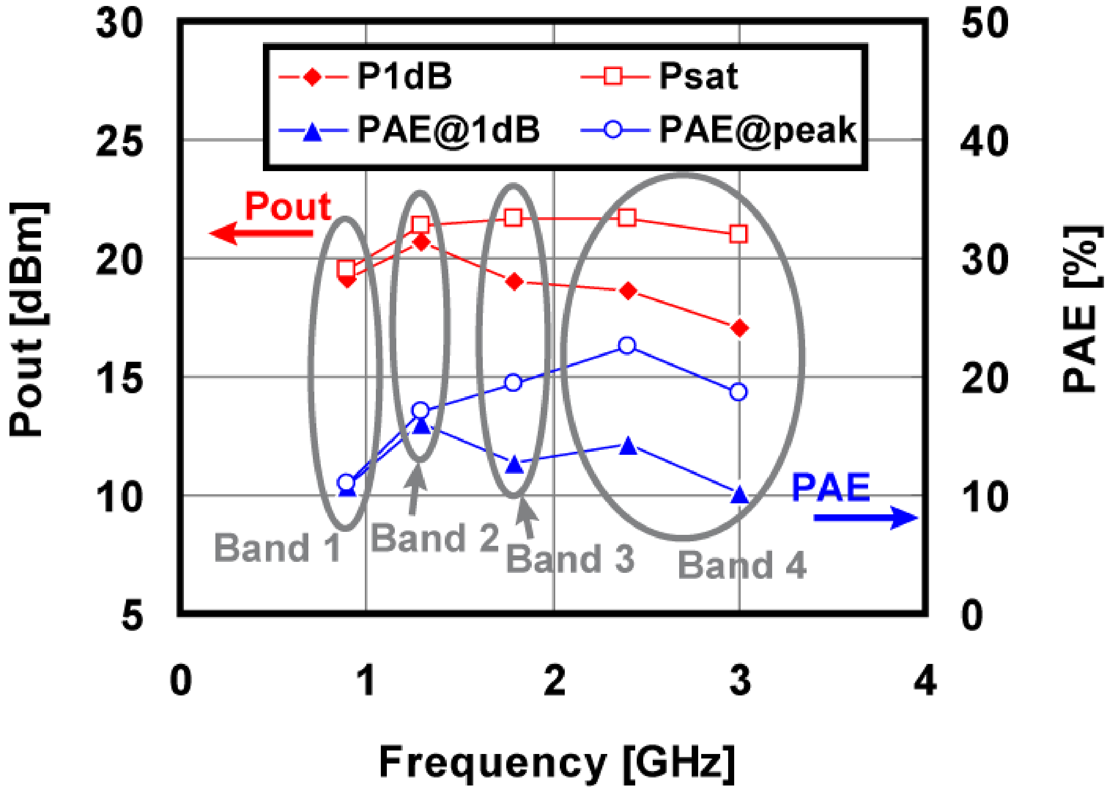
- **Input and output losses are calibrated from results**

Large signal measurement result



P_{1dB}	18.6dBm
P_{sat}	21.7dBm
PAE_{max}	22.6%

P_{out}, PAE v.s. Frequency



- Measured large signal performance in each band and each signal frequency
- P_{sat} is larger than 19dBm, and PAE@peak is larger than 11% at the entire frequency range

Comparison of CMOS PAs

	Technology	V_{DD} [V]	Frequency [GHz]	P_{sat} [dBm]	PAE@peak [%]	Area [mm^2]	Output matching
RFIC '04 [4]	0.13μm CMOS	2.0	2.0 ~ 8.0	7 ~ 10	2 (@1dB)	—	Wideband
ISSCC '09 [5]	0.13μm CMOS	1.5	0.5 ~ 5.0	14 ~ 21	3 ~ 16 (drain eff.)	3.6	Wideband
T-MTT '07 [6]	0.18μm CMOS	2.8	3.7 ~ 8.8	16 ~ 19	8 ~ 25	2.8	Wideband
ISSCC '09 [7]	0.13μm CMOS	3.0	1.0 ~ 2.5	28 ~ 31	18 ~ 43	2.56*	Wideband
This work	0.18μm CMOS	3.3	0.9 ~ 3.0	20 ~ 22	11~ 23	1.03	Tunable

*With distributor

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Conclusion

- Output impedance tuning method utilizing LC-resonance and resistive feedback is proposed
- 0.18μm fully integrated CMOS PA
- 0.9-3.0 GHz output matching
- At the entire frequency range, over 19dBm output power and over 11% PAE is achieved

Thank you for your attention!