A 9.3MHz to 5.7 GHz Tunable LC-based VCO Using a Divide-by-N Injection-Locked Frequency Divider

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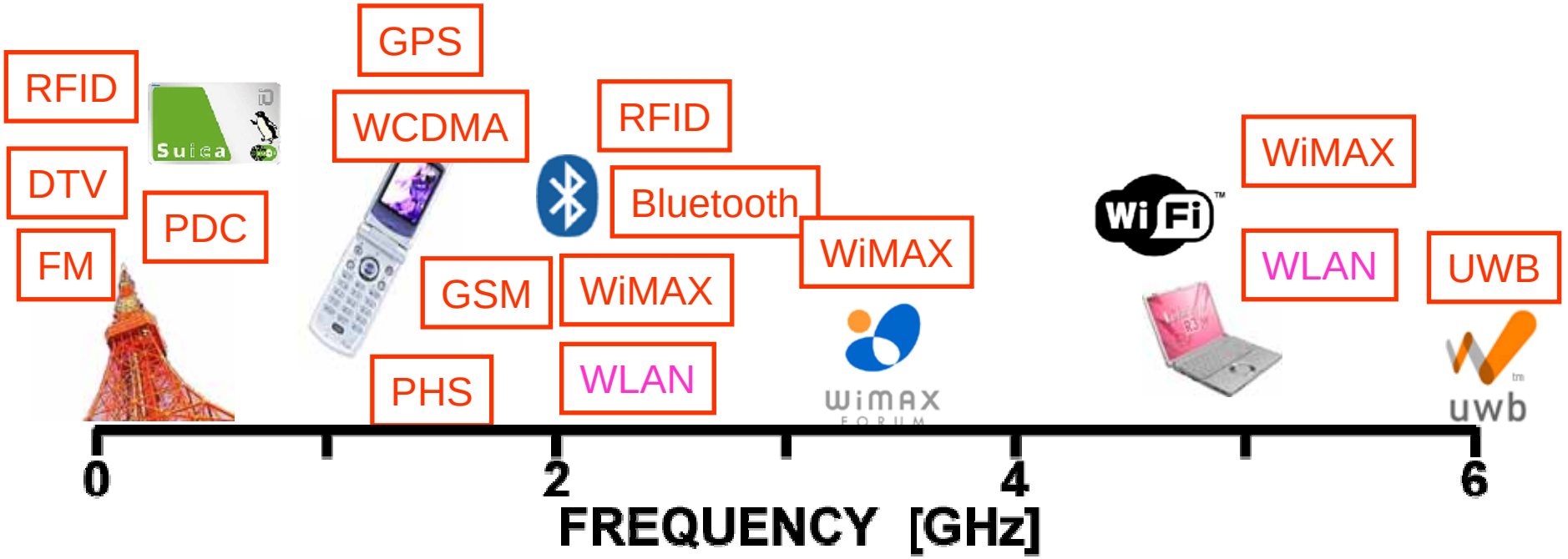
Outline

- **Background**
- **Wideband VCO using divide by *N* ILFD**
- **Schematic and Measurement results**
- **Summary**

Background

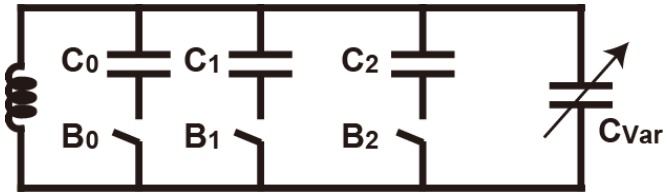


Wideband VCO

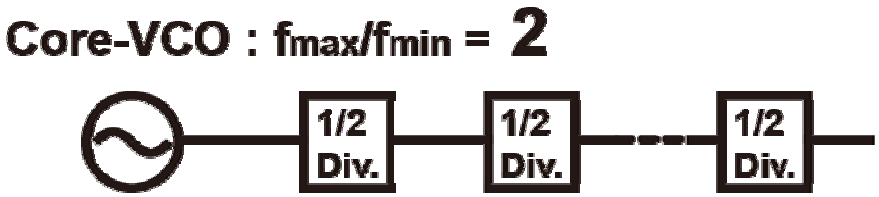
- **10 MHz to 6 GHz of frequency range**
- **Lower phase noise**
- **Lower power operation**
- **Smaller size**
- **Quadrature output**
- **Spurious tones, *etc.***

Previous work

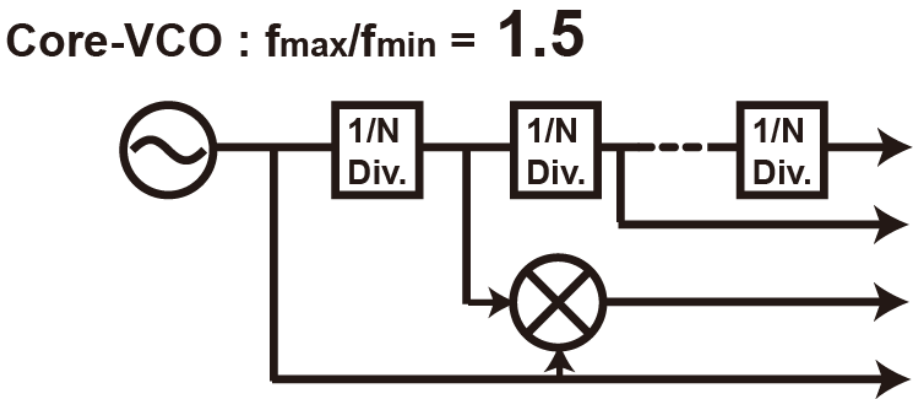
- **Switched-Capacitor Resonator**
  - + Reduced K_{VCO}
  - - Q_L is degraded at edge of tuning range
  - - Limited C_{max}/C_{min} (parasitic capacitance limited)



- **1/2 Divider**
  - + Continuous wide tuning range
  - - Wide tuning range requirement for VCO
  - - Poor phase noise

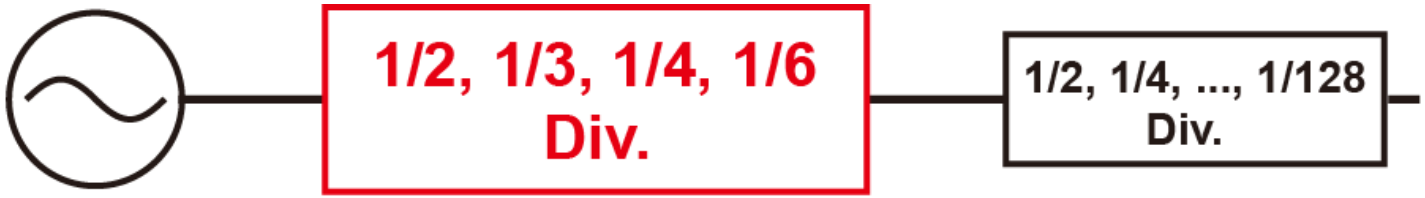


- **Dividers, Mixers**
  - + Narrow tuning range
  - - Large power consumption
  - - Spurious tones



[1] Z. Safarian, *et al., CICC*, Sep. 2008.

Proposed wideband VCO

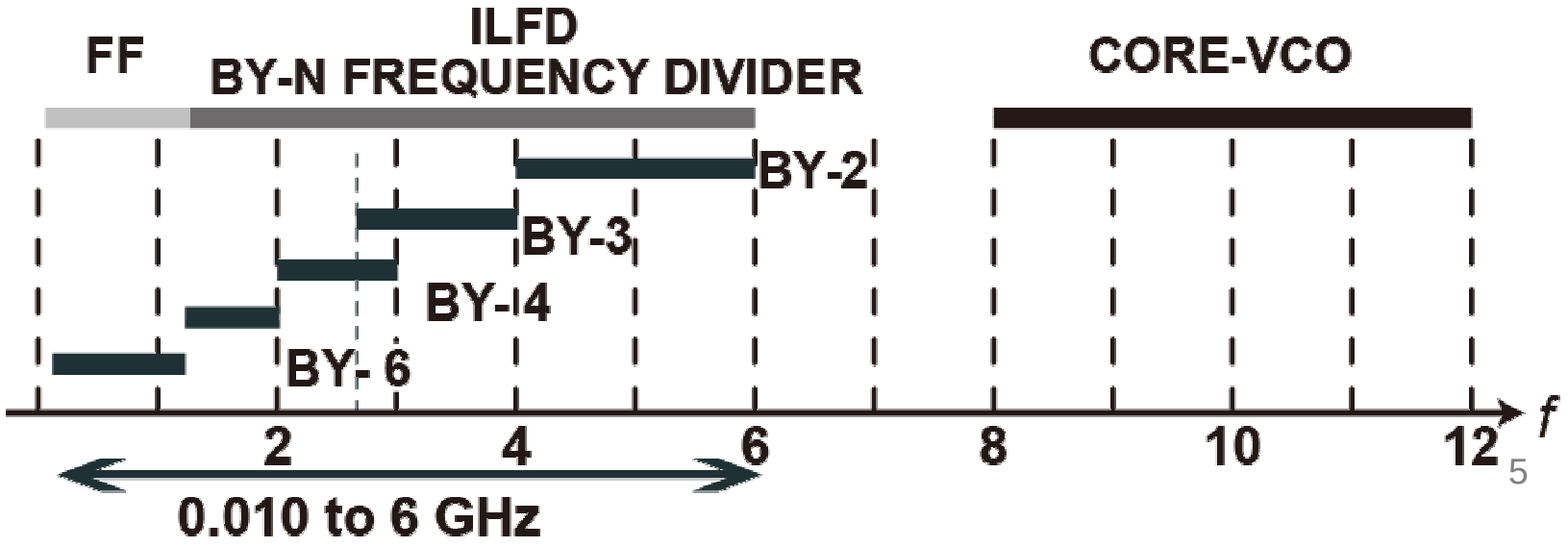


Core-VCO
8 to 12 GHz
f_{max}/f_{min} = 1.5
Differential

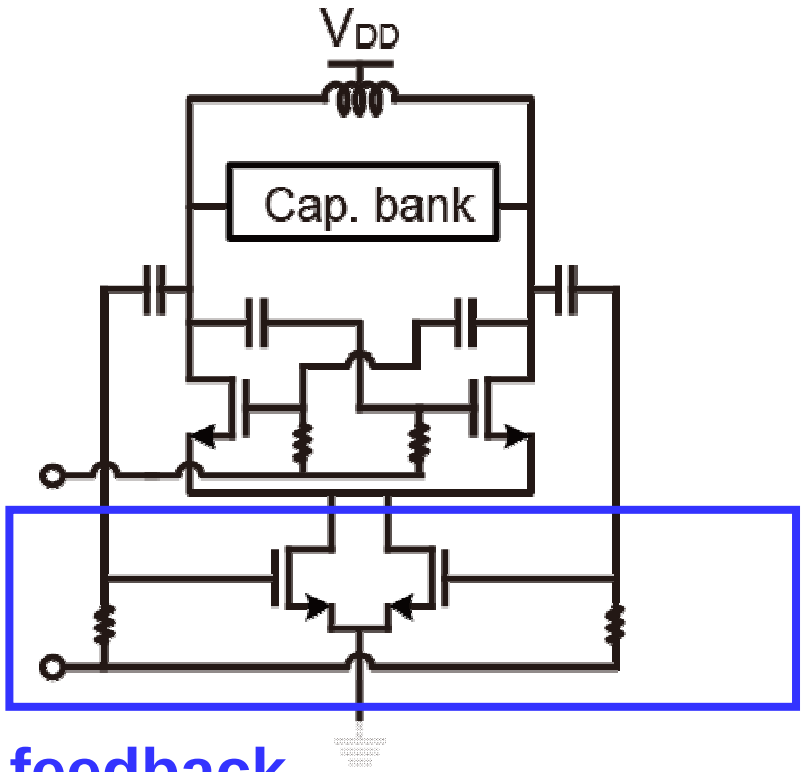
Injection-Locked
Frequency Divivder (ILFD)
1.33 to 6 GHz
fmax/fmin = 4.5
Quadrature

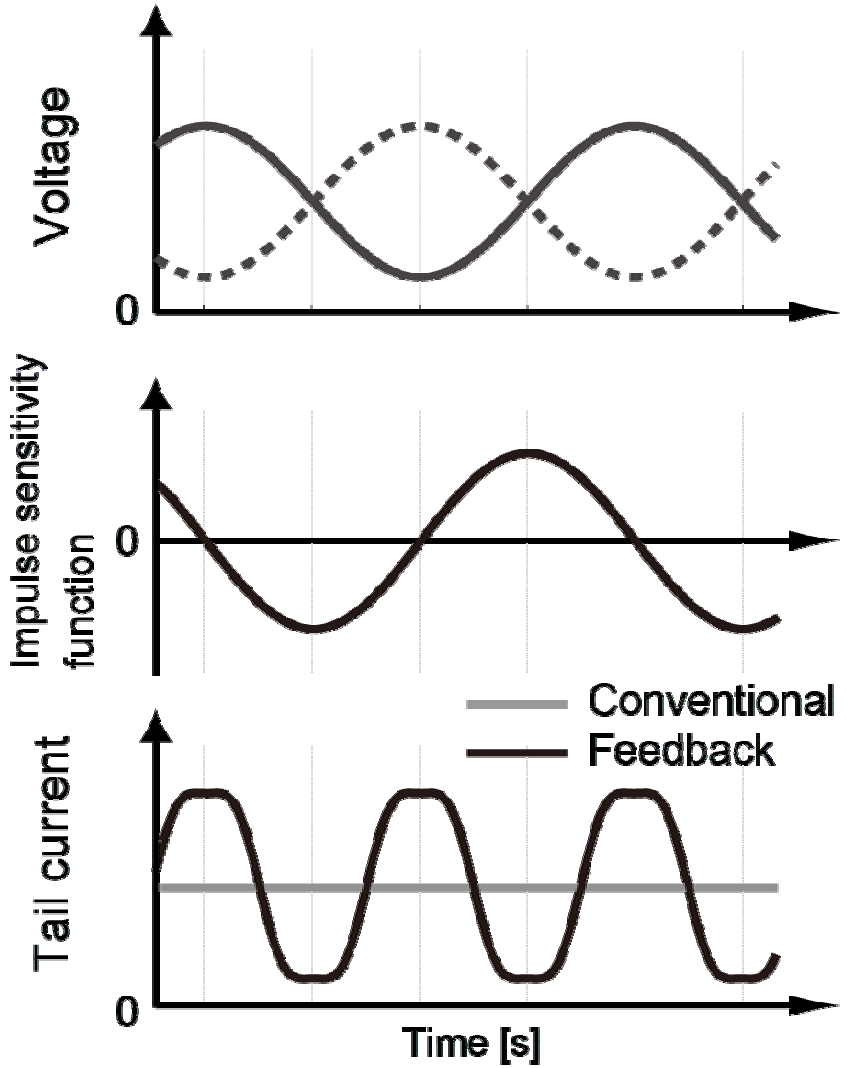
Flip flop divider * 7

Narrow required tuning range, No spur, Quadrature output



Core VCO



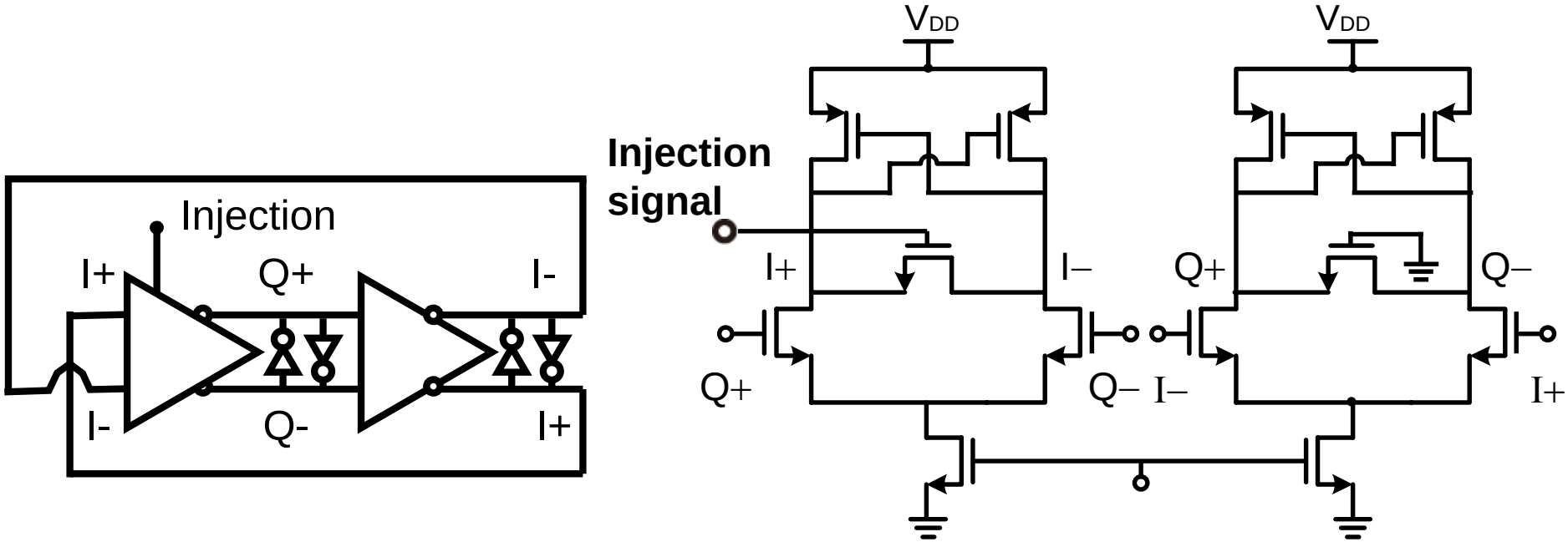


Tail feedback

3.5dB phase noise improvement

- **Tuning range : 8.0 to 12.0 GHz**

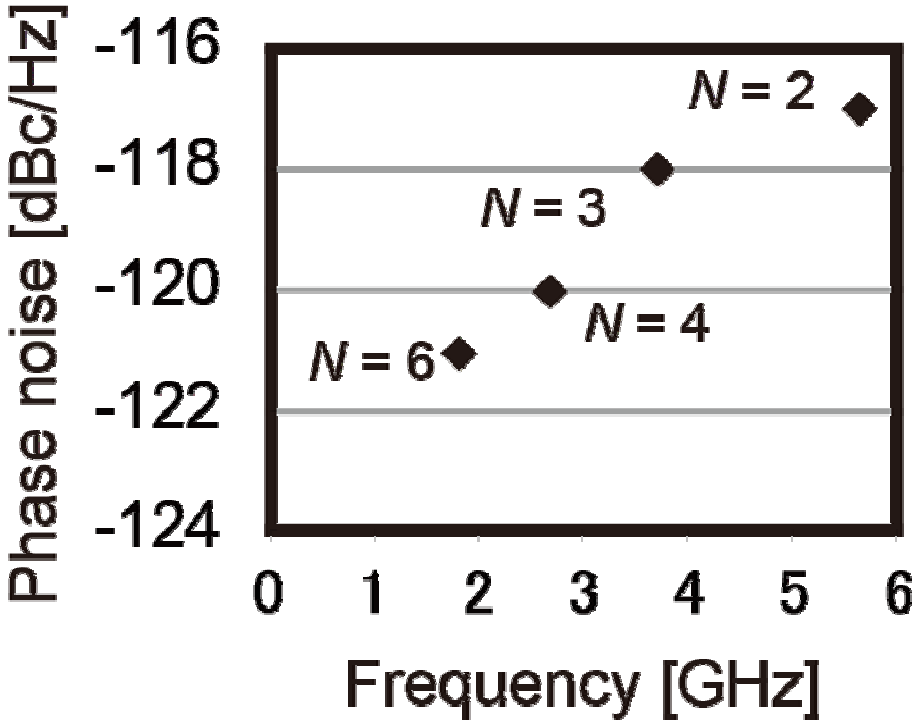
Injection Locked Frequency Divider

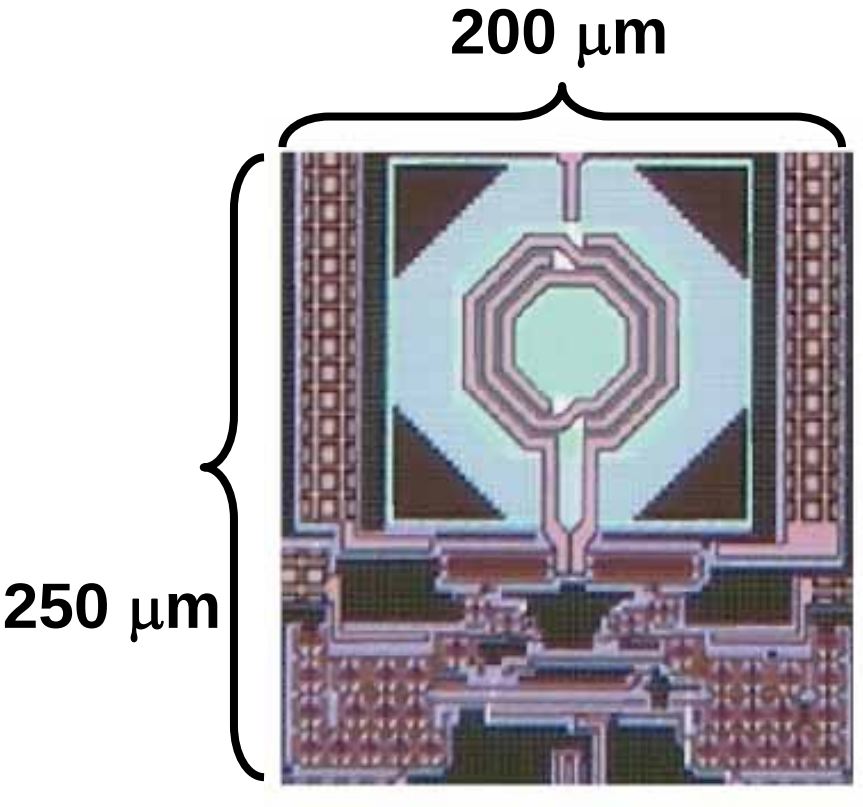


- **Tuning range : 1.3 to 6.0 GHz**
- **2-stage differential ILFD is utilized.**

Merit: Quadrature output, No Spur, Wide frequency range

Measurement result





Fabricated by 90 nm CMOS Process

VCO measurement summary

	This work	VLSI 2009[2]	RFIC 2009[3]
Architecture	VCO with ILFD	QVCO with mixer and dividers	2VCOs and dividers
Divide ratio	2,3,4,6…	2,3,4,5, 6,8,10	2,4,8,16,32…
Tuning range of core LC-VCO	±20 %	±20 %	±33.3 % (total)
Output freq.	0.009 - 5.7 GHz	1 - 10 GHz	0.1 - 5.0 GHz
Power cons.	5.9 - 11.2 mW	31 mW	19.8 mW
FoM$_T$	-210 dBc/Hz	-194 dBc/Hz	-209 dBc/Hz
Area	0.05 mm^2	0.29 mm^2	0.22 mm^2

$$FoM_T = L(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{FTR}{10}\right) + 10\log\left(\frac{P_{VCO}}{1\text{mW}}\right)$$

[2] B. Razavi, *VLSI Circuits*, June 2009.
[3] P. Nuzzo, *et al*., RFIC, June 2009.

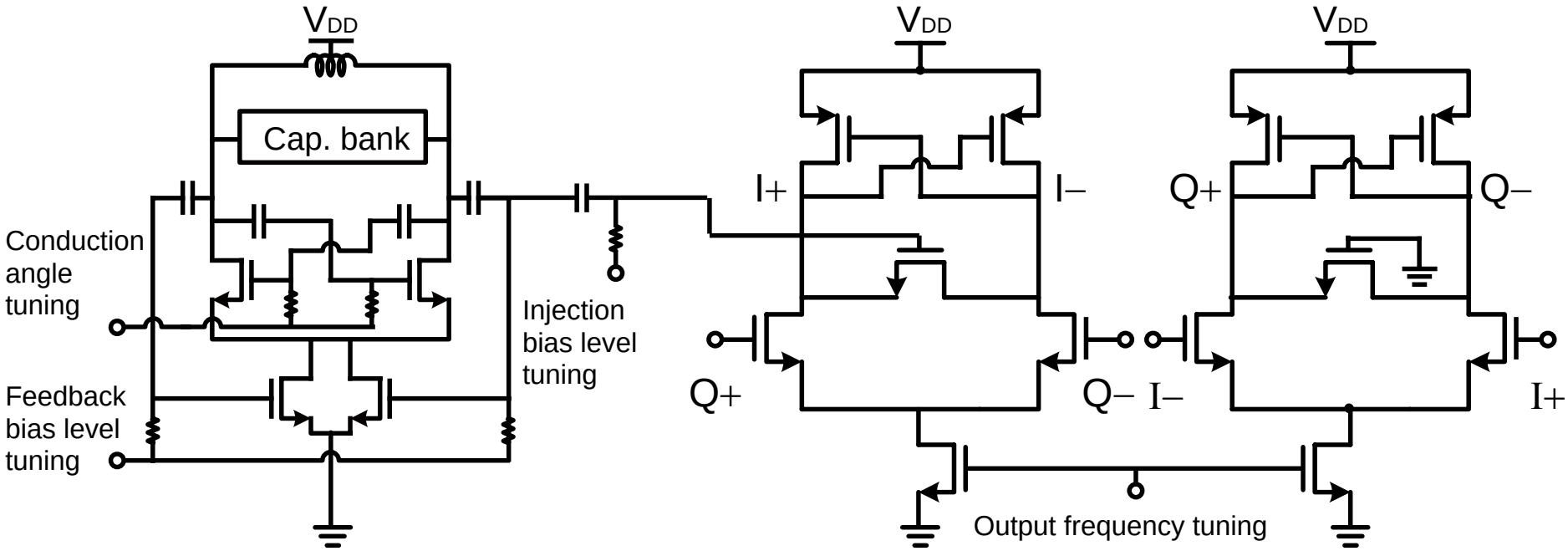
Summary and conclusion

- **A differential LC-VCO and injection locked frequency divider are utilized instead of a QVCO and a SSBM for the spurious and narrow band and small area.**
- **The proposed wideband VCO can achieve wide tuning range with sufficient phase noise.**

FTR=199% FOM$_T$=-210dBc/Hz

Thank you for your attention!

Circuit schematics

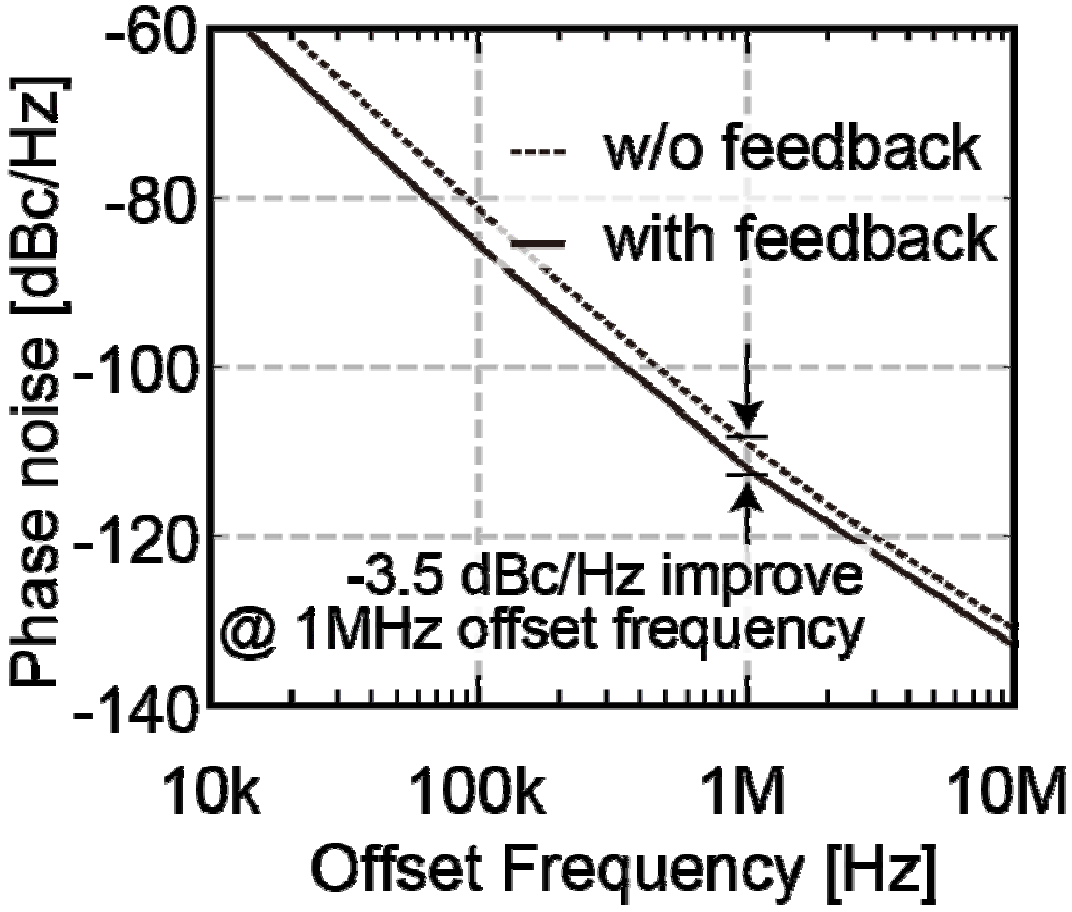


Core VCO

Injection locked frequency divider

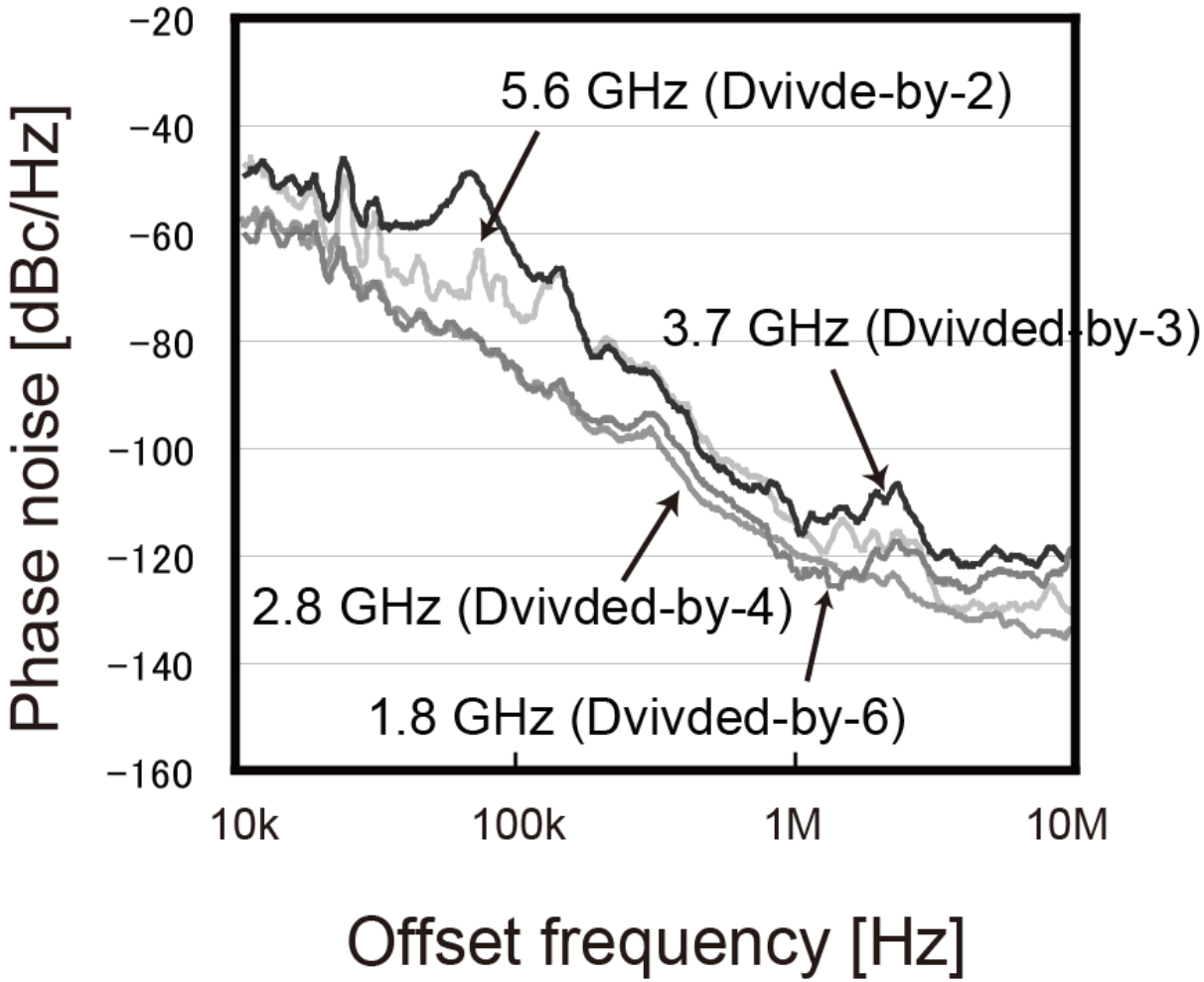
- **ILFD generates 1.33 to 6.0 GHz output.**
- **Lower frequency (under 1.33GHz) can be obtained by using FF dividers.**

Simulation result of feedback VCO



Feedback VCO can improve phase noise with smaller power consumption

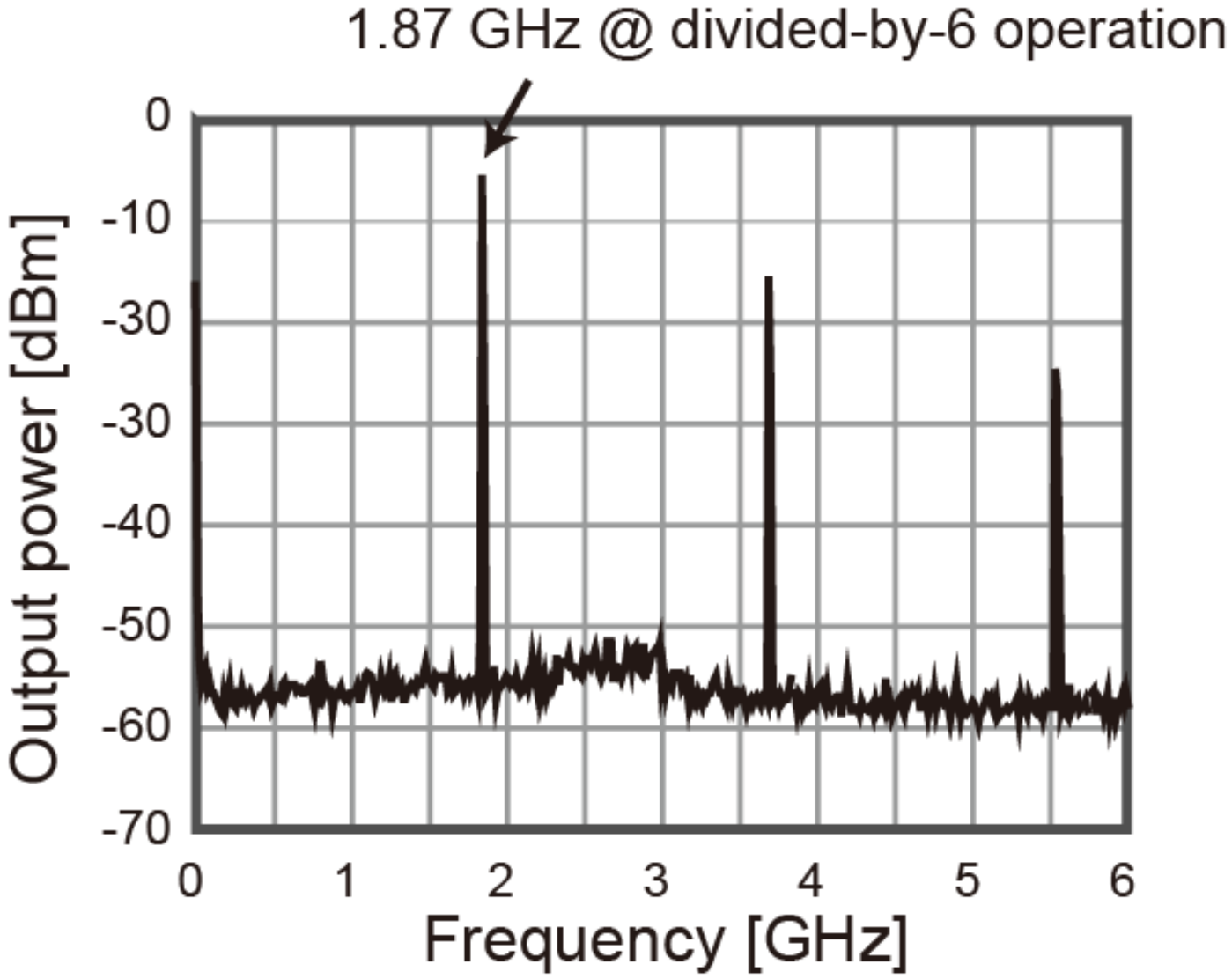
Phase noise


−20
−40
−60
−80
−100
−120
−140
−160
Phase noise [dBc/Hz]
5.6 GHz (Dvivde-by-2)
3.7 GHz (Dvivded-by-3)
2.8 GHz (Dvivded-by-4)
1.8 GHz (Dvivded-by-6)
10k
100k
1M
10M
Offset frequency [Hz]

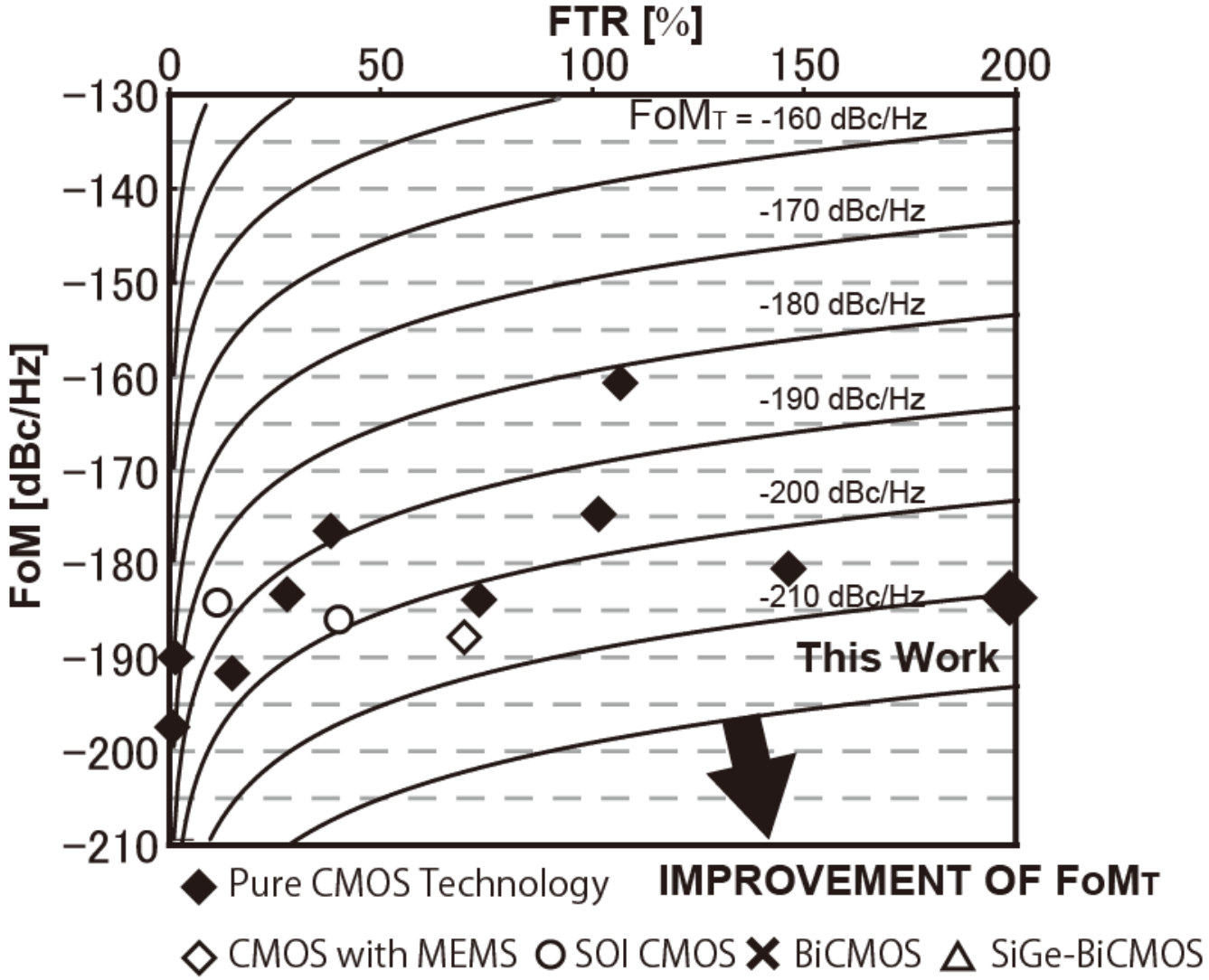
Phase noise 2

Oscillation frequency	Phase noise @1MHz offset	FoM	FoMT
5.6 GHz (1/2 *f*o)	-117 dBc/Hz	-184 dBc/Hz	-184 dBc/Hz
3.7 GHz (1/3 *f*o)	-118 dBc/Hz	-184 dBc/Hz	-184 dBc/Hz
2.8 GHz (1/4 *f*o)	-120 dBc/Hz	-184 dBc/Hz	-184 dBc/Hz
1.9 GHz (1/6 *f*o)	-121 dBc/Hz	-184 dBc/Hz	-184 dBc/Hz

Output spectrum



Performance comparison



VCO performance

Technology	FUJITSU 90nm CMOS
Supply voltage	1.2 V
Power consumption of VCO core	4.8 - 10.2 mW
Power consumption of ILFD	1.0 - 1.3 mW
Power consumption of FF dividers	- 0.1 mW
Total power consumption	5.9 - 11.2 mW
Tuning range	9.3 MHz - 5.7 GHz
Chip area	250 μm x 200 μm

質疑

- ロックレンジは？
  - I could not measure lock sensitivity because the input power of ILFD is fixed. Actually, the larger divide operation has narrower lock range, so we need lock-range calibration. The divide ratio is selected by the control voltage of ILFD. 次のページに続く。
- VCOの位相雑音特性の分布は？
  - Unfortunately, I don’t have detailed data now, but it is not so bad. The worst case may be 2 or 3dB higher than the best case.
- LC-VCOの出力電力は？
  - I have no data now. I have a full voltage swing at almost entire frequency range. It is sufficient for locking operation.

質疑

- 分周比が大きいところで位相雑音劣化してない？
- 分周器通すとなんで位相雑音よくなるの？
  - Basically, the phase noise of the ILFD is determined by the phase noise of incident VCO signal. At the high offset frequency, the phase noise is a little degraded, and the band width is determined by the ILFD.
- どうやって分周比変えるの？
  - The divide ratio is selected by the control voltage of ILFD, and tuning is required. This circuit will be finally implemented as a PLL, and it also has a feedback loop. So, we can know the relationship between the control voltage and free running frequency of ILFD by using the PLL mechanism. The information can be used for the lock-range selection. Actually, there is some papers for the locking range calibration.