A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC

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Outline

1. Motivation
2. Conventional issues
3. Proposed circuit
4. Experimental results
5. Conclusions

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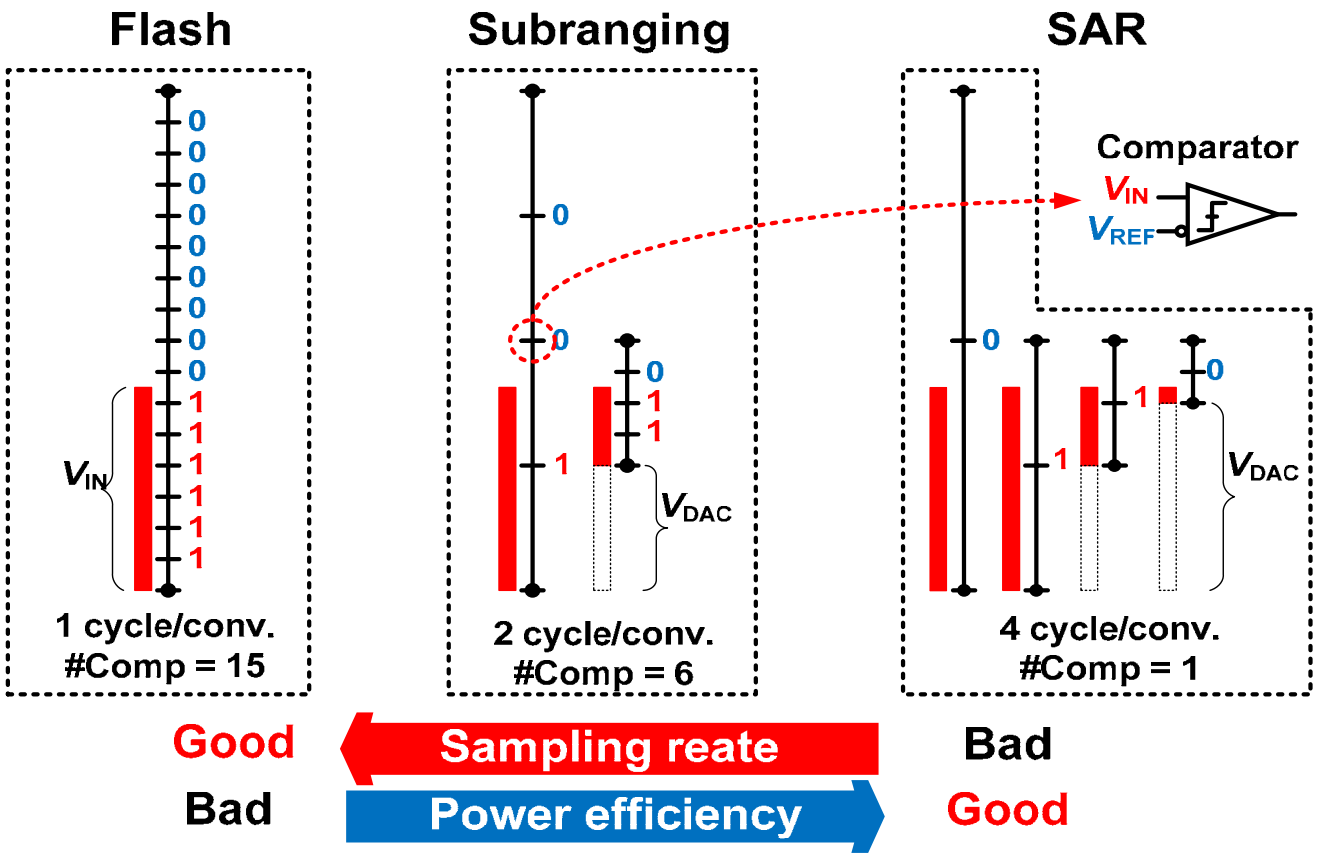
Motivation

- **6~7 bit, around 1GS/s ADCs have many applications.**
  - **Disk drive front-ends**
  - **Ultra wideband receivers**
- **Ultra low power ADC IP cores are needed for portable applications and Green IT regulation.**
- **Conventional ADC has difficulty adjusting to deep submicron technology.**
  - **Increasing VT mismatch**
  - **Lowering supply voltage**
  - **Degradation of intrinsic gain of MOS FET**

ADC architectures



6~7bit, around 1GS/s operation
Flash ➔ Poor power efficiency
SAR ➔ Extremely high speed CLK (6GHz~)
Subranging ➔ Good balance

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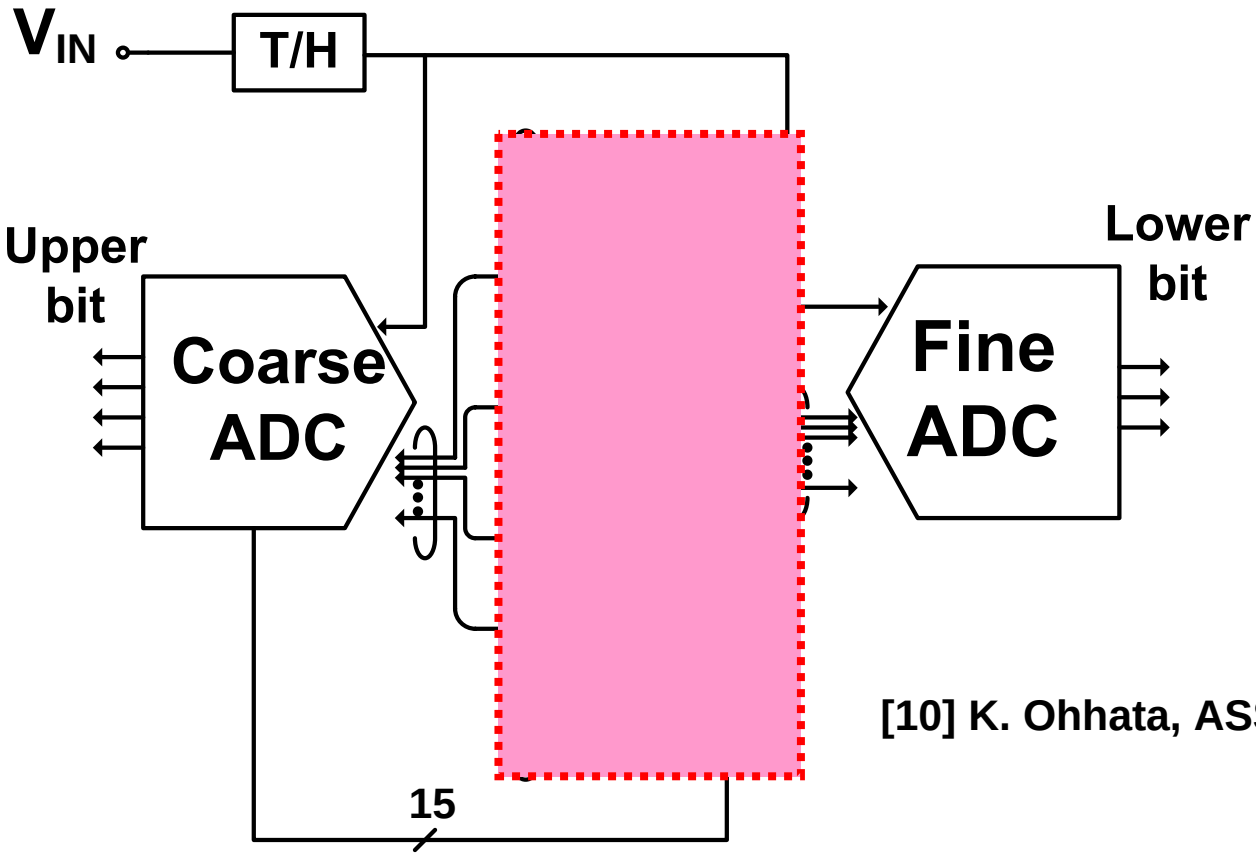
Issue of reference voltage generation



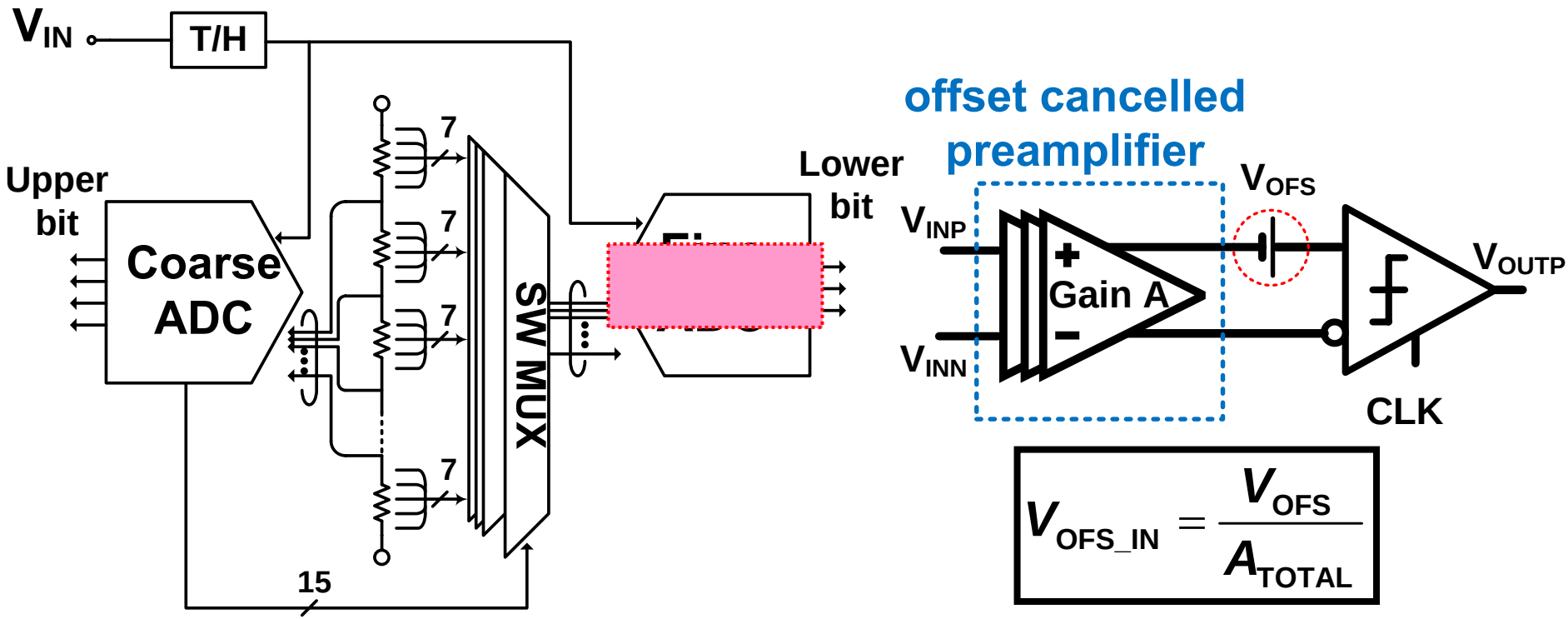
[10] K. Ohhata, ASSCC 2008

Resistor ladder + SW MUX:

- **Static power consumption in resistor ladder**
- **Resistance should be low for fast settling.**

➔Trade-off between power consumption and settling time.

Power consumption for offset cancellation



Preamplifier + Comparator :

- **The preamplifier consumes a static power**
- **Gain is degraded in deep submicron device**
- **Offset cancelation of the preamplifier is needed.**

➔ **Cascade amplifier have disadvantage in power and area.**

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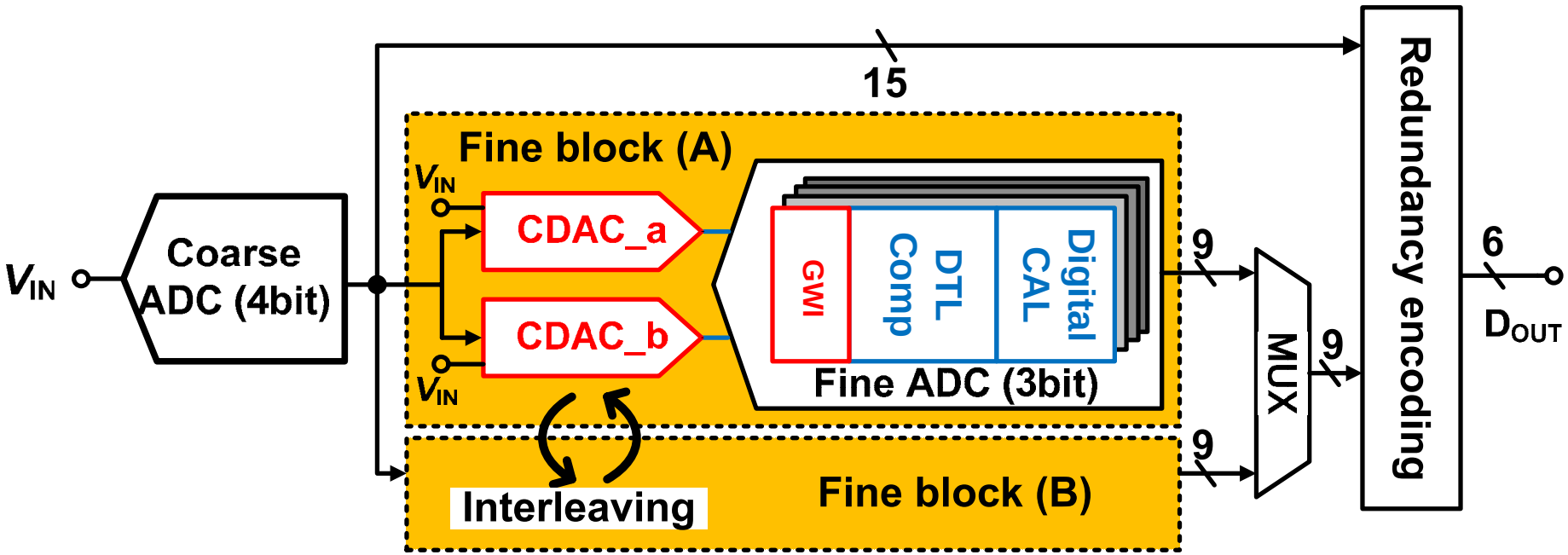
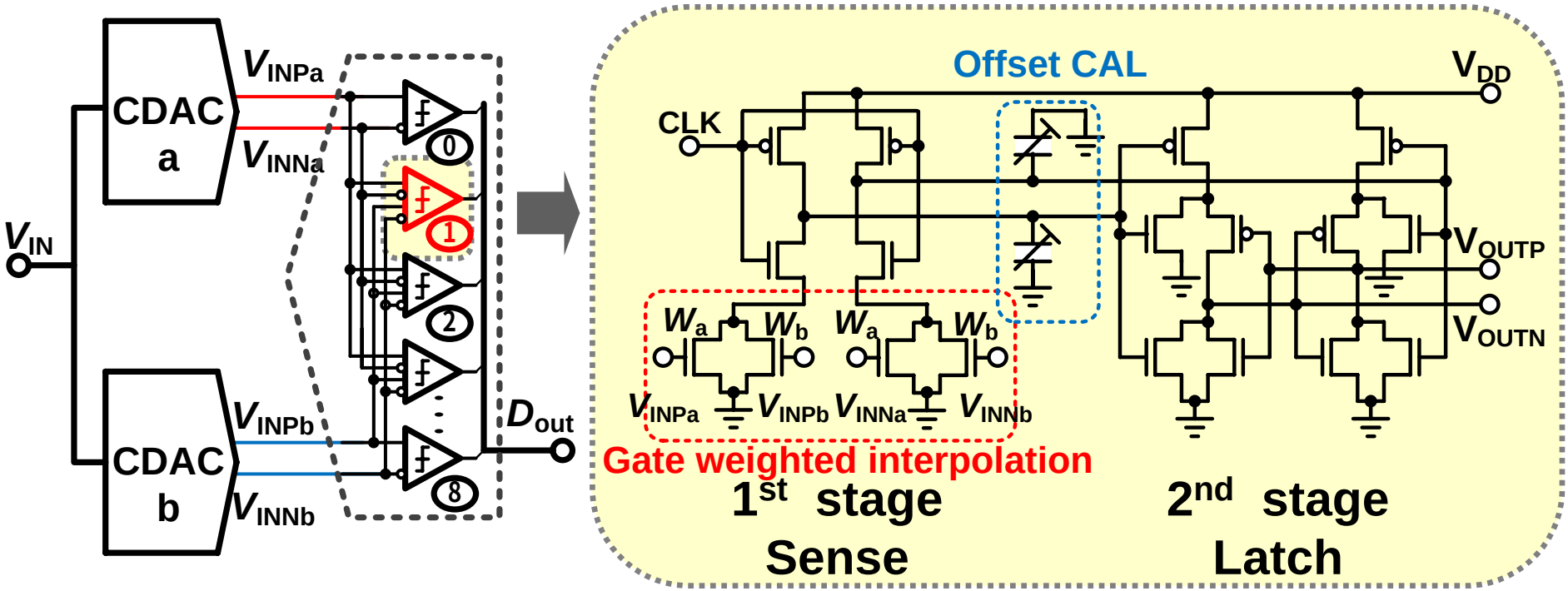
Proposed system



System Configuration

- **Redundancy encoding**
  - ➔ Correct conversion error of coarse ADC
- **Fine block Interleaving**
  - ➔ Reduce conversion cycle from 2 to 1.
- **Proposed fine block (CDAC + Fine ADC)**
  - ➔ Reduce power in Fine ADC & Reference Voltage Gen.

Detail of proposed circuit



Proposed Circuit

1. Capacitive DAC (C-DAC)
2. Gate-weighted interpolation (GWI)
3. Digital offset calibration

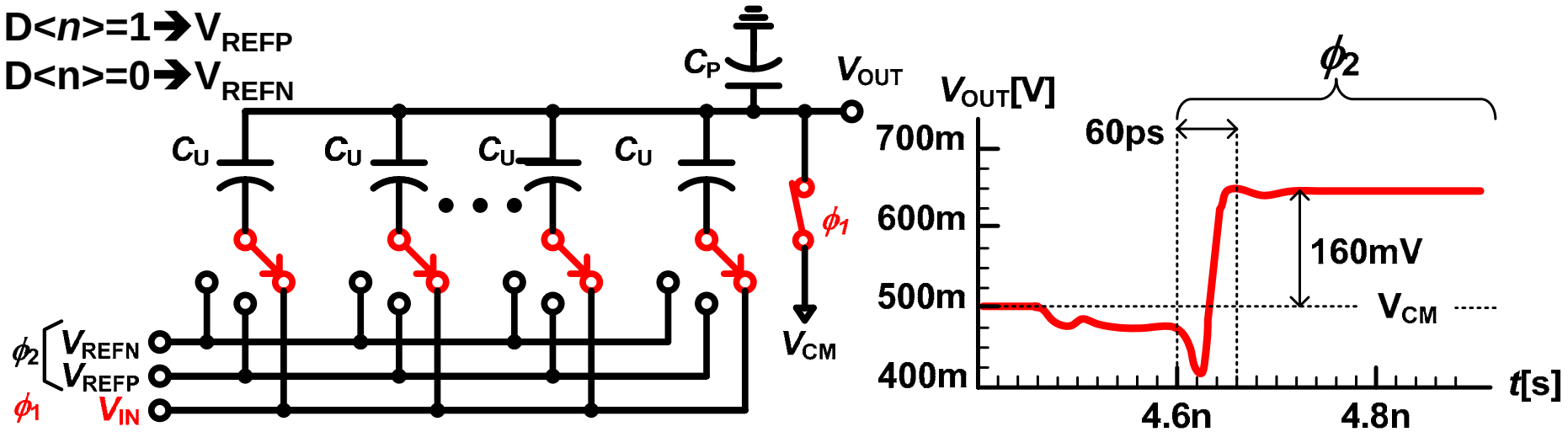
Conventional Circuit

~~R ladder + SW MUX~~

~~Preamplifer~~

➔Fine block consumes no static power.

1. C-DAC



$$V_{OUT} = \frac{16C_U}{16C_U + C_P}\left(V_{IN} - V_{DAC}\right)$$

Advantage :

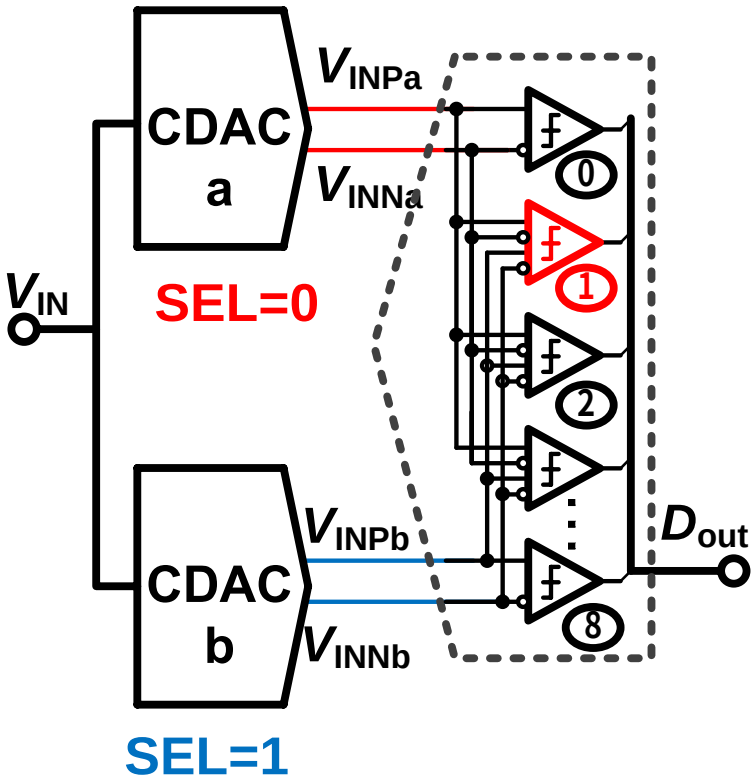
- **Operating as S/H circuit**
- **No static power consumption (360μW@1GHz)**
- **Smaller C_u realize faster settling time**

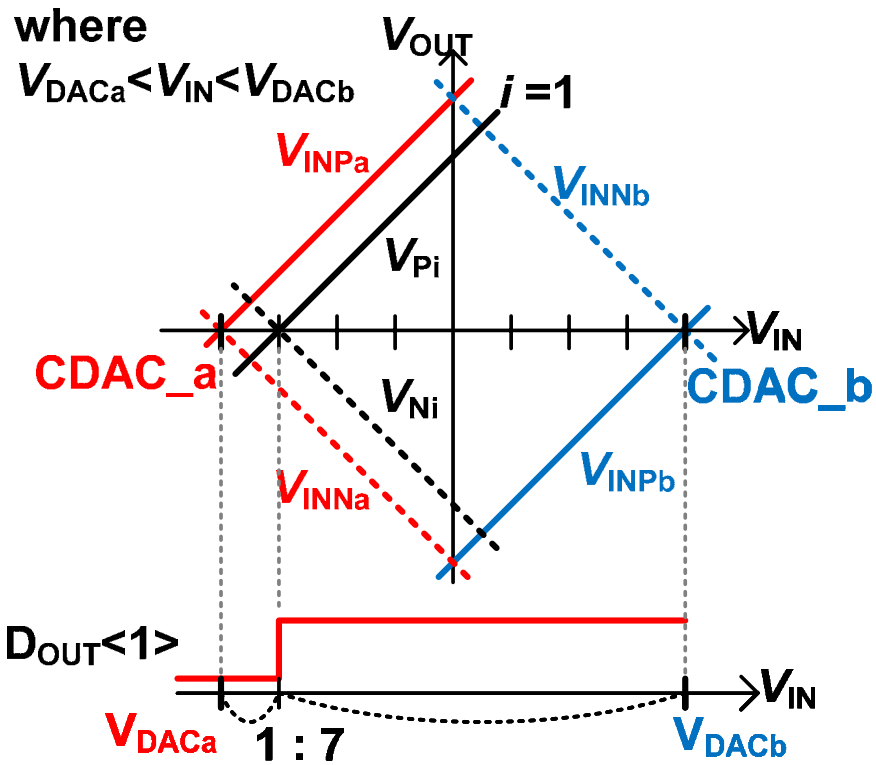
  (t_{DAC}= 3.4 $r_{on}C_U$ < 80ps @ r_{ON} = 1kΩ, C_U= 15fF)

Disadvantage :C_P causes gain error.

➔ Interpolation comparator overcomes the disadvantage.

Conversion mechanism of interpolation

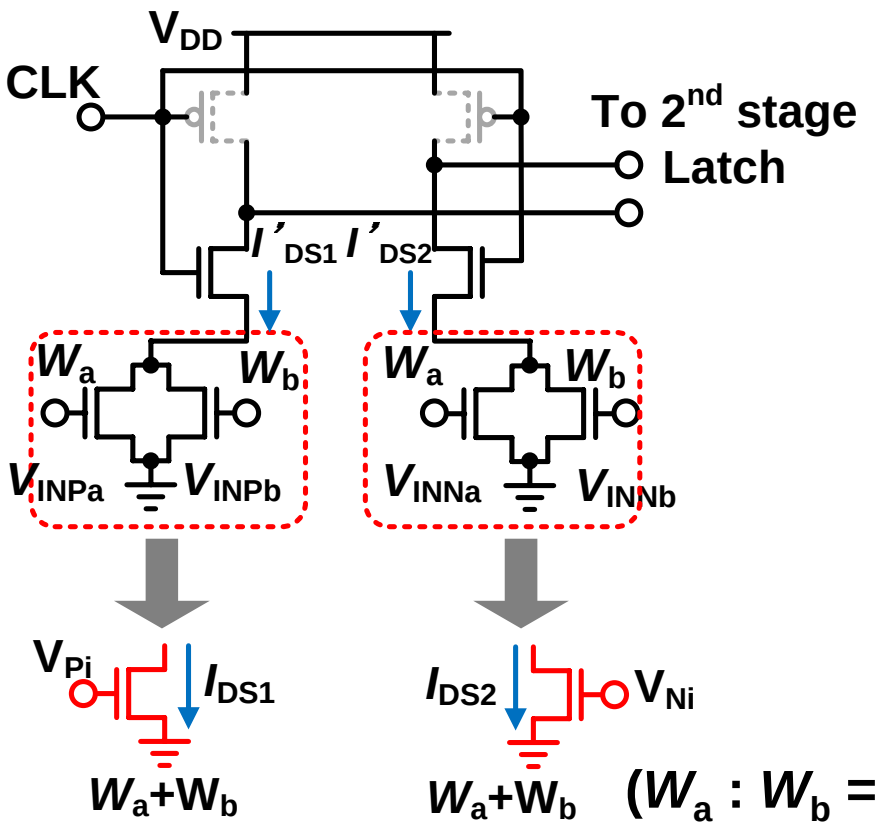




$$V_{Pi} = \frac{(8-i)V_{INPa} + iV_{INPb}}{8}, V_{Ni} = \frac{(8-i)V_{INNa} + iV_{INNb}}{8}$$

- No reference voltage is required for each comparator.
- comparator threshold is NOT sensitive to CDAC gain error

2. Gate-weighted interpolation



Long channel device

$$I_{DS1} = \beta \frac{W_a + W_b}{L}\left(V_{Pi} - V_T\right)^2$$

$$\Rightarrow \quad I'_{DS1} \neq I_{DS1}$$

Deep submicron device

$$I_{DS1} \approx \alpha \left(W_a + W_b\right)\left(V_{Pi} - V_T\right)$$

$$\Rightarrow \quad I'_{DS1} \approx I_{DS1}$$

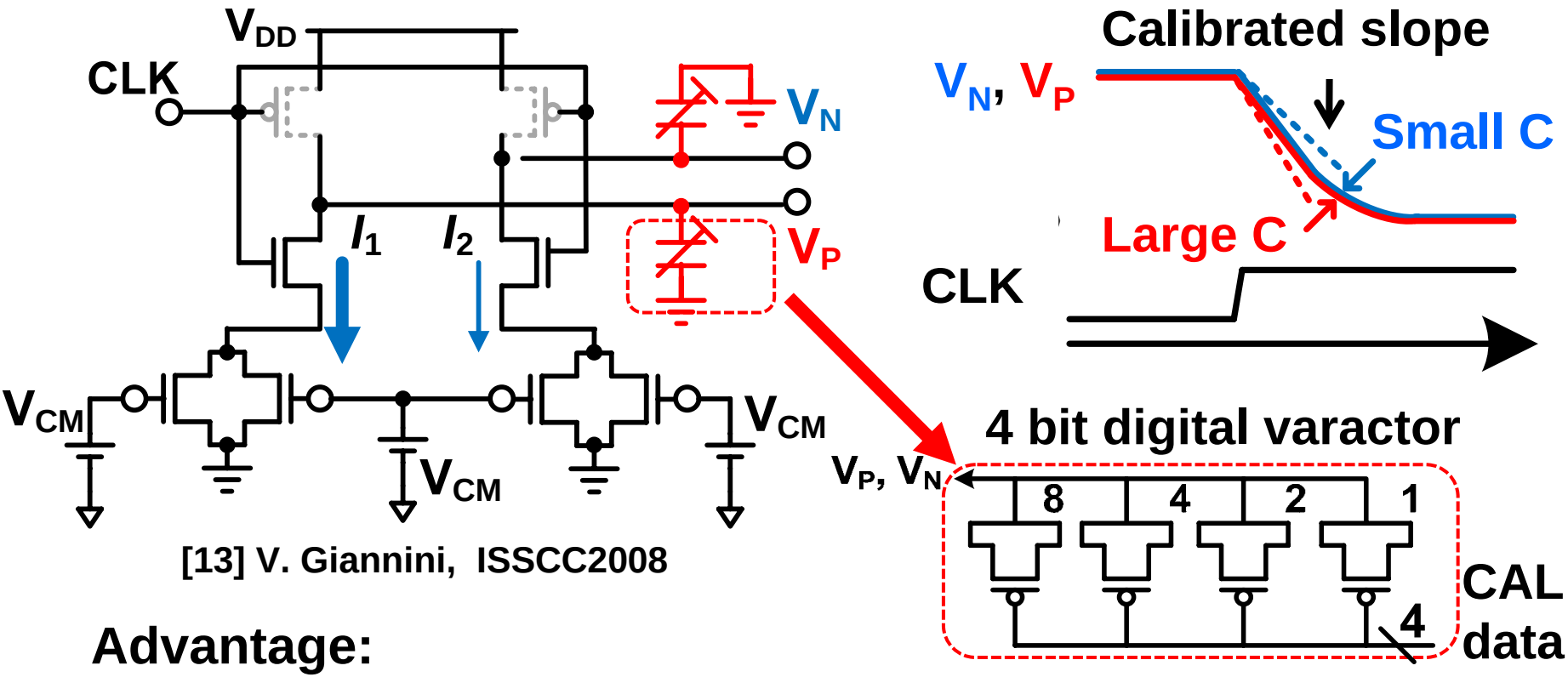
$(W_a : W_b = i : 8 - i)$

Advantage : **Power consumption increases very little.**

Disadvantage : **Interpolation error** **because of non-linear characteristic of MOS FET.**

➔ **Interpolation error is only less than 0.3%.**

3. Digital calibration



[13] V. Giannini, ISSCC2008

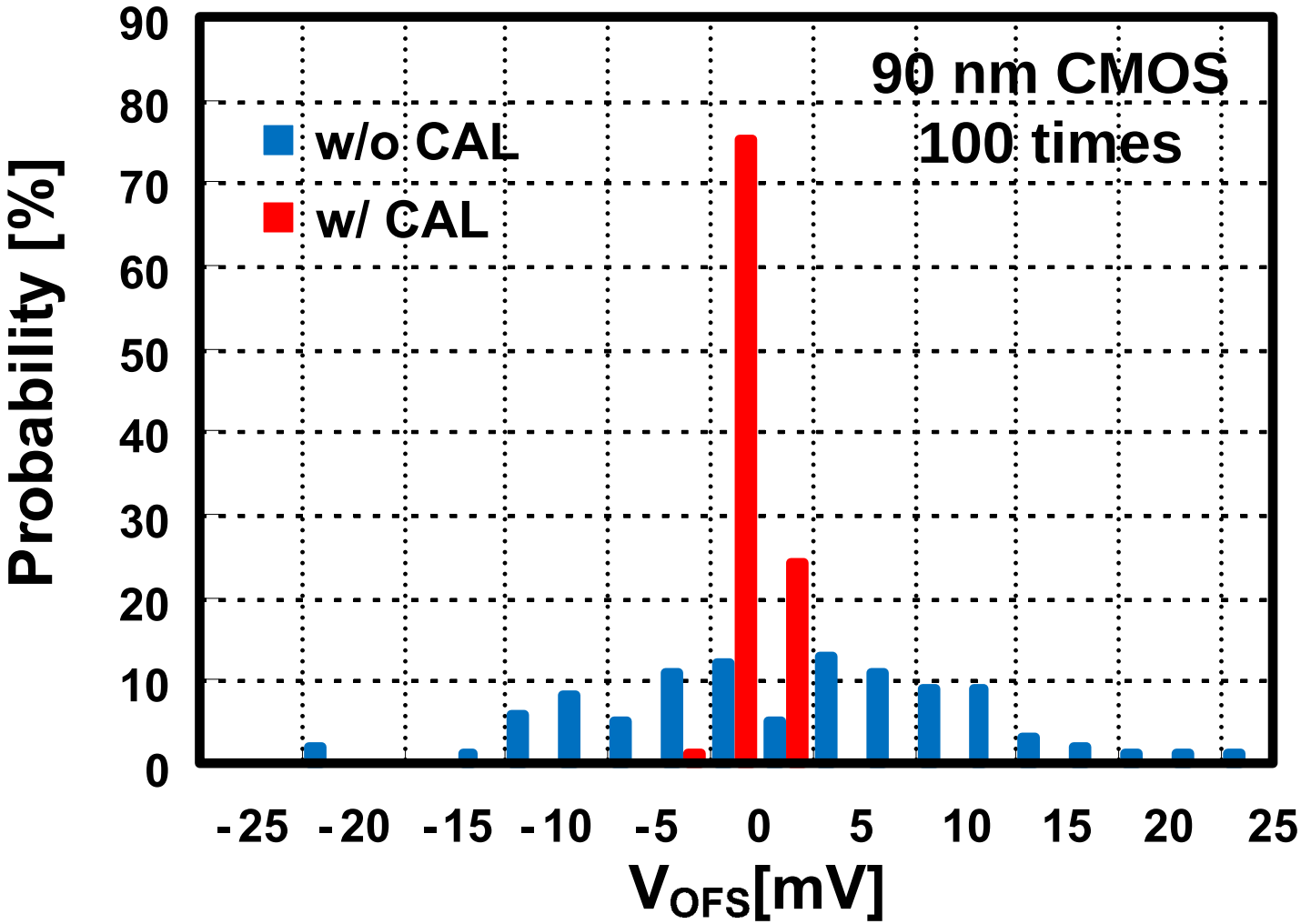
Advantage:

- **Low power operation (63 fJ/conv.)**
- **Input noise is improved (σ=0.7mV$_{RMS}$)**

Disadvantage: Latch speed is slightly slowed down.

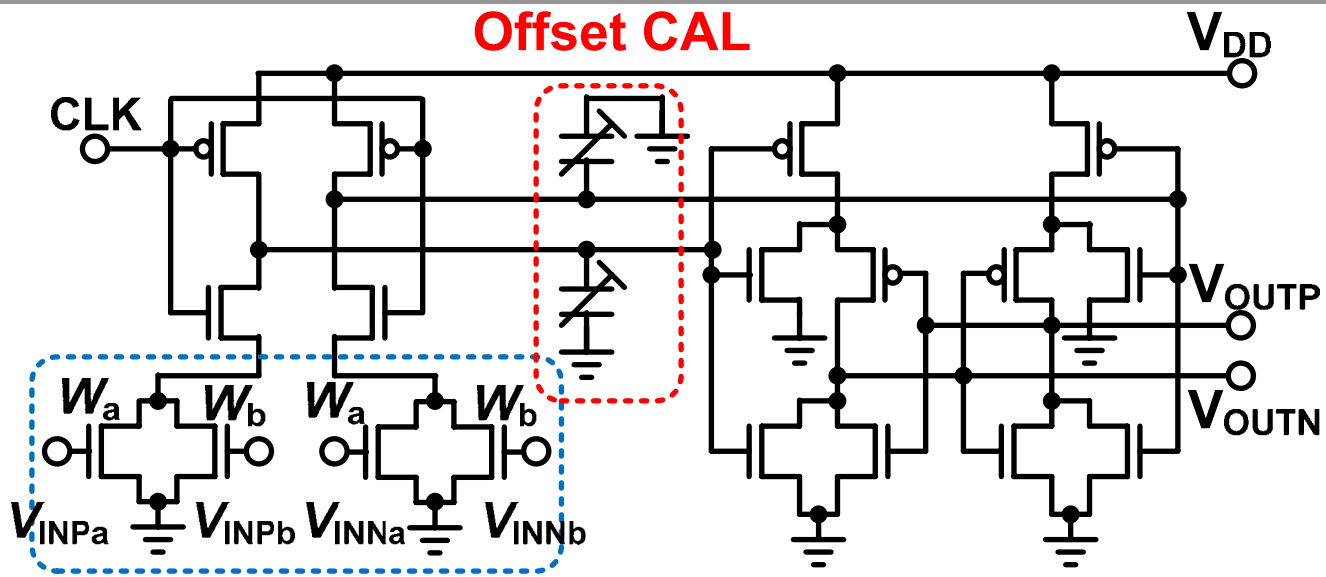
➔ However, comparator can operate precisely over 2GHz.

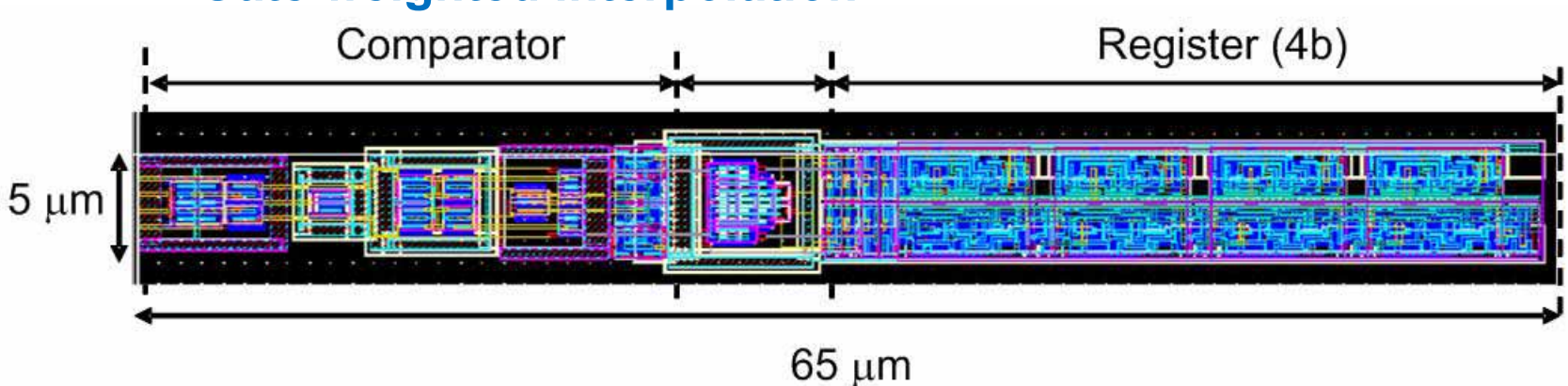
Monte Carlo simulation



Offset variation is reduced from $9mV_{RMS}$ to $0.9mV_{RMS}$.

Comparator layout





Proposed comparator achieves low power, high accuracy and small area at the same time.

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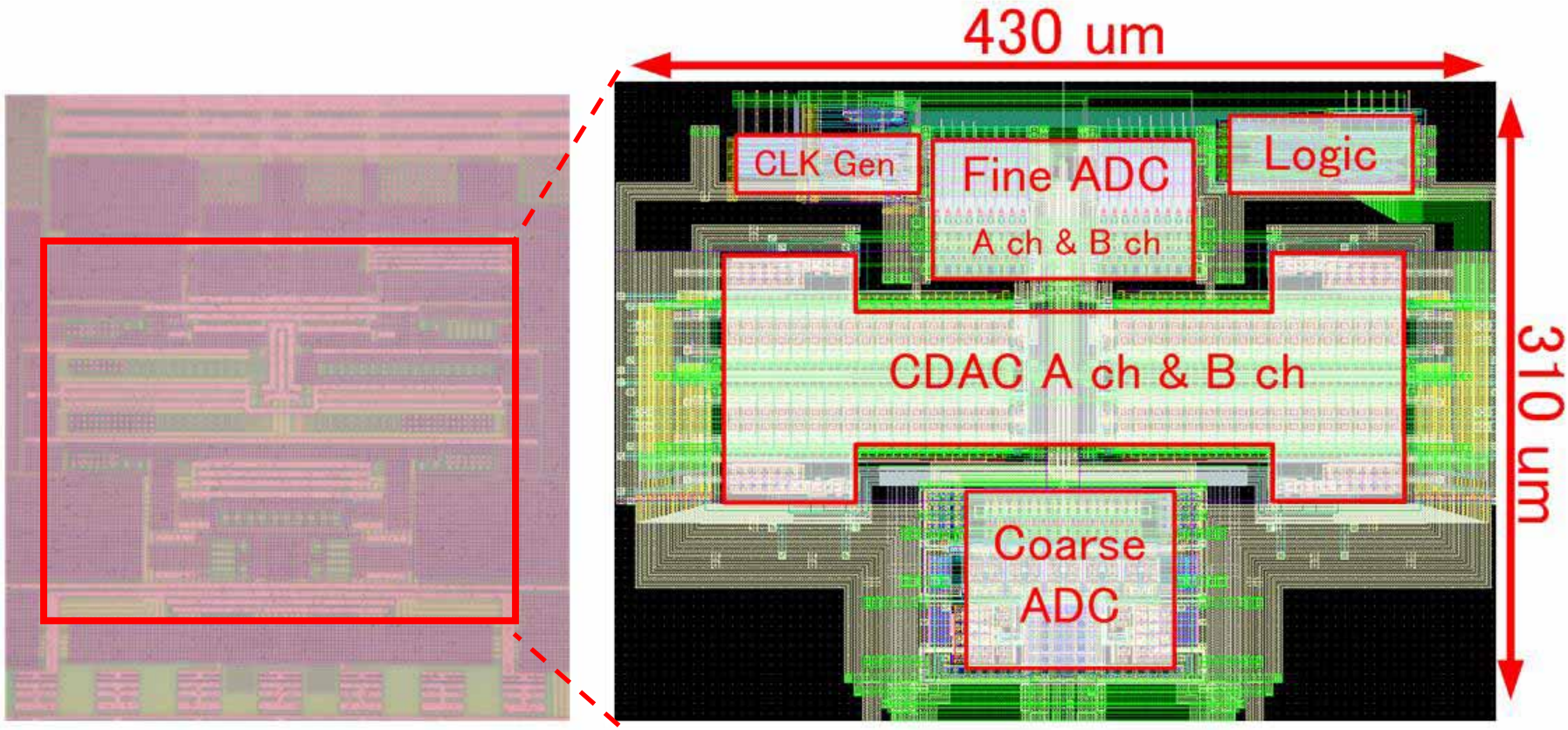
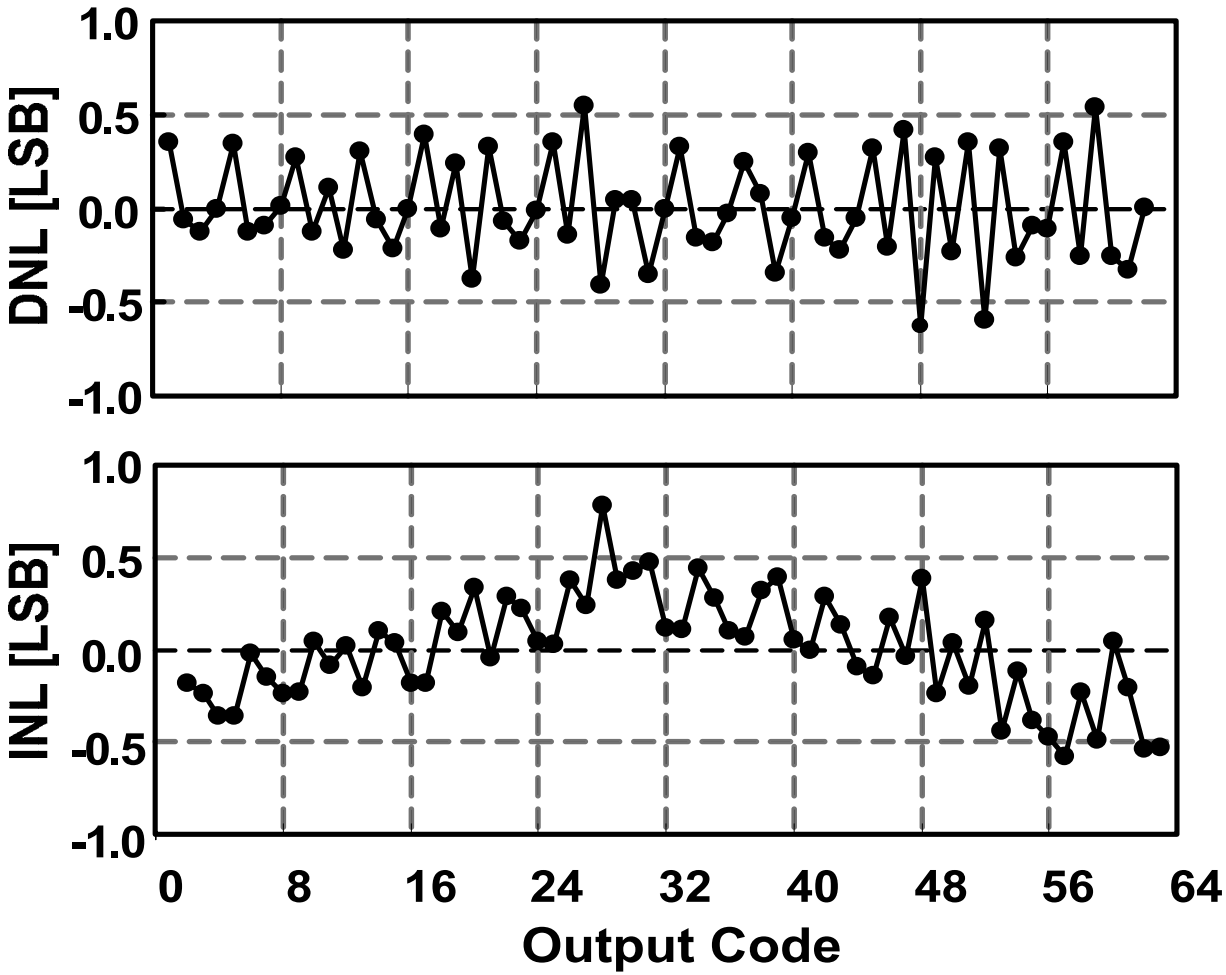
Chip photo & Layout

- **6 bit ADC has been realized in a 90 nm 10M1P CMOS technology with a chip area of 0.13mm^2**



DNL, INL

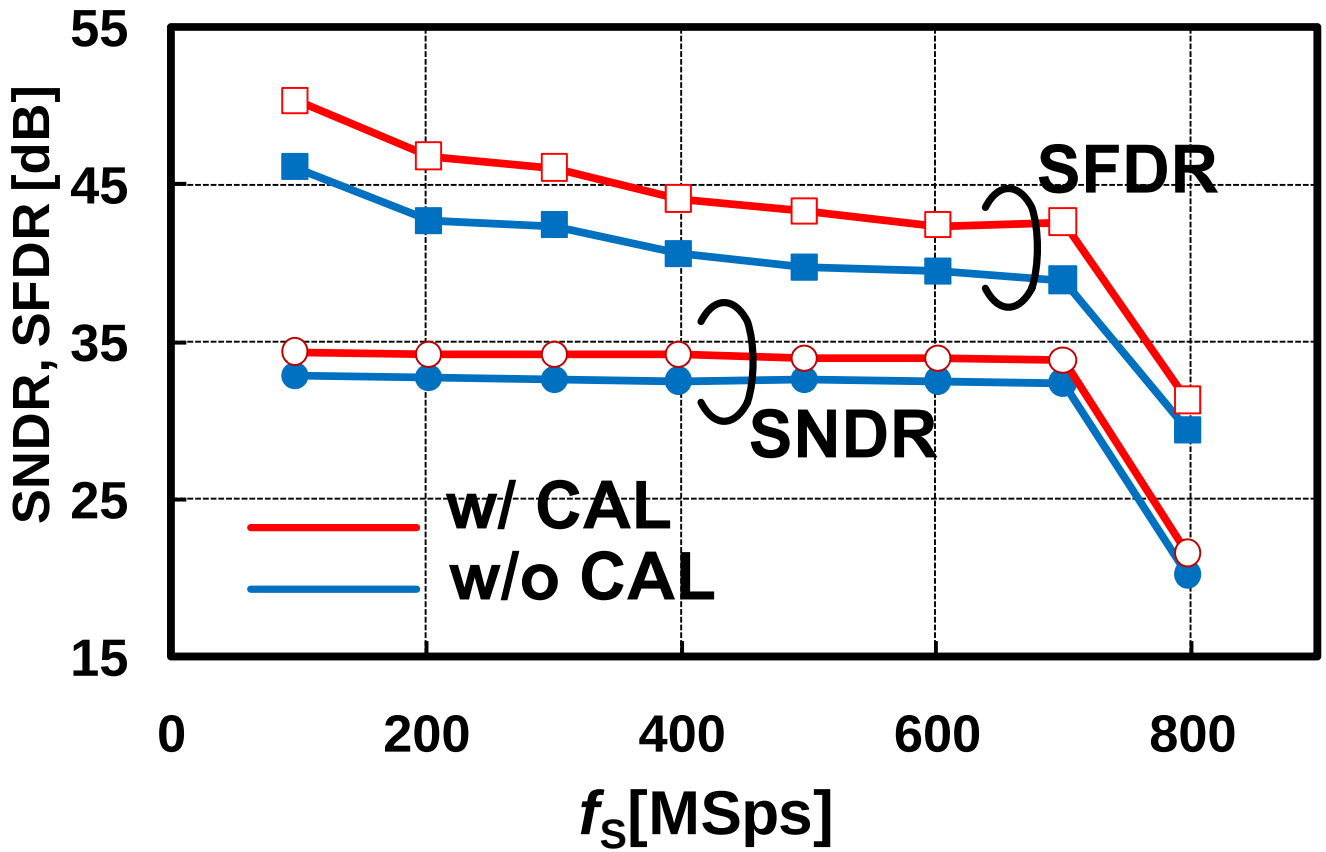
VDD=1.2V, after Calibration



- **DNL : +/- 0.6LSB INL : +/- 0.8LSB**

SNDR, SFDR vs. f_S

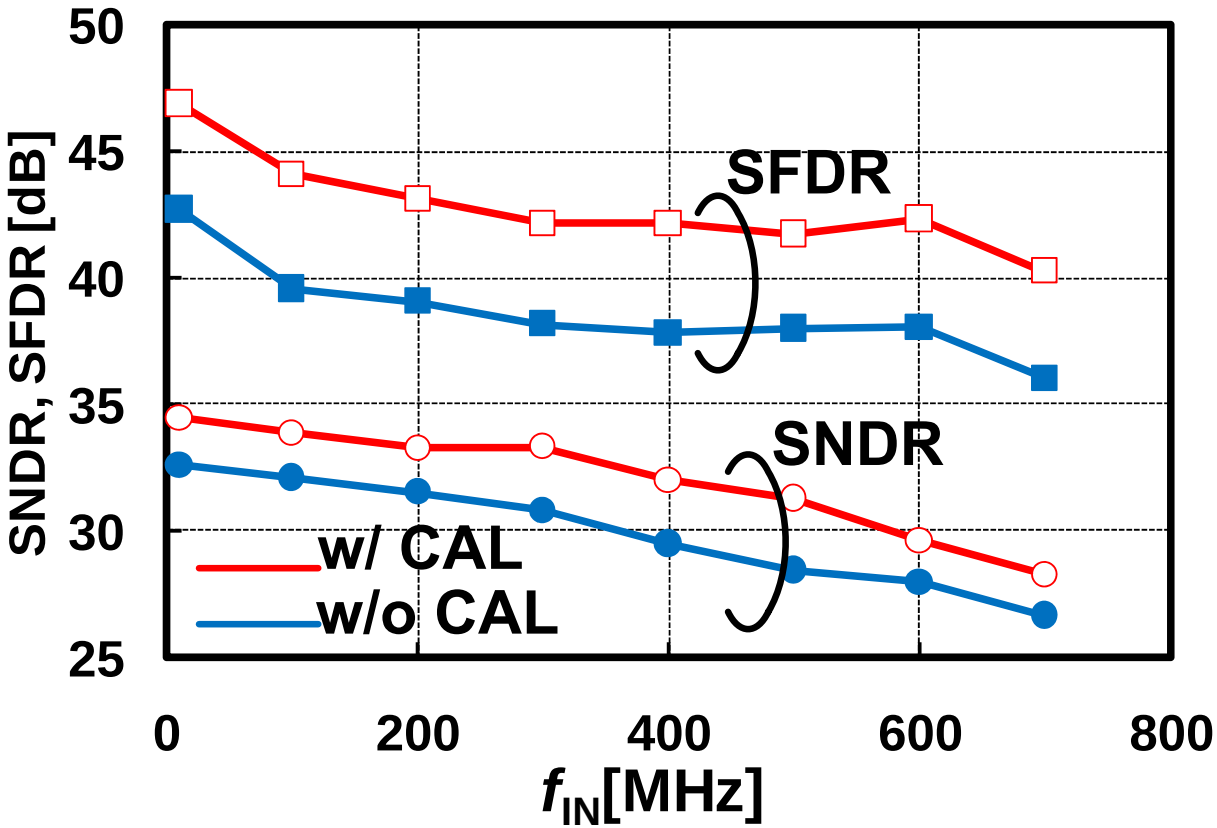
V_{DD}=1.2V, f_{IN}=50MHz



- Offset calibration improves SFDR by **5dB**.

SNDR,SFDR vs. f_{IN}

V_{DD}=1.2V, f_S=700MS/s



- SNDR is 34dB (ENOB = 5.3) at Nyquist frequency
- P_{TOTAL}=7mW @ f_S=700MS/s

➔ FoM = 250fJ/conv.

$$FoM = \frac{P_{TOTAL}}{2^{ENOB} \bullet f_S}$$

Performance summary

Proposed circuits has realized the best power efficiency.

	[1]	[2]	[3]	[4]	[6]	This Work
Resolution(bit)	6	6	6	6	6	6
fs(GS/s)	0.8	1.2	0.7	1.25	1	0.7
SNDR(DC/Nyq.)	35/32	34/33	31/30	34/28	35/33	35/34
Pd (mW)	12	75	24	32	30	7
Active area(mm^2)	0.13	0.43	0.052	0.09	0.18	0.13
FoM(pJ)	0.44	2.17	1.31	1.22	0.8	0.25
CMOS Tech.(nm)	65	130	130	130	90	90
Architecture	Flash	Flash	Pipeline	2b-SAR	Subrange	Subrange

[1] C-Y. Chen, VLSI Circuits 2008.
[2] B-W. Chen, A-SSCC 2008.
[3] F. C. Hsieh, A-SSCC 2008.
[4] Z. Cao, ISSCC 2008.
[6] Y. C. Lien, A-SSCC 2008.

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Conclusions

- **We have proposed ultra low power subranging ADC, which is suitable for deep sub-micron technology.**
  - **DTL comparator with digital calibration**
    - **Good power efficiency(63fJ/conv.)**
    - **Low offset variation (0.9mV$_{RMS}$)**
  - **CDACs and gate-weighted interpolation**
    - **Good power efficiency(CDAC:360μW@1GHz)**
    - **Fast settling time (< 80ps)**
    - **Without any reference voltage for sub-scale**

- **Proposed circuit has good power efficiency for high speed operation. (FoM 250fJ/conv.)**

Thank you for your interest!