A Low-Offset Latched Comparator Using Zero-Static Power Dynamic Offset Cancellation Technique

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Abstract—**A low-offset latched comparator using new dynamic offset cancellation technique is proposed. The new technique achieves low offset voltage without pre-amplifier and quiescent current. Furthermore the overdrive voltage of the input transistor can be optimized to reduce the offset voltage of the comparator independent of the input common mode voltage. A prototype comparator has been fabricated in 90 nm 9M1P CMOS technology with 152 μm^2. Experimental results show that the comparator achieves 3.8 mV offset at 1 sigma at 500 MHz operating, while dissipating 39 μW from a 1.2 V supply.**

I. INTRODUCTION

A low-offset, low-power consumption, small area comparator is a very important circuit block for many applications, such as memory sensing circuits, analog to digital converters (ADC), and so on. The technology scaling of CMOS transistor decreases power consumption and occupying area. However, offset voltage of the comparator exceeds tens mV at 1 sigma due to the transistor mismatch. Therefore, offset voltage cancellation or calibration techniques are vital for realizing a low offset voltage comparator. In conventional designs, preamplifiers were used for offset voltage cancellation [1]. However, it increases power consumption because wide bandwidth amplifiers are required to reduce the offset voltage in the high frequency operation. Furthermore, it is very difficult to realize a high voltage gain amplifier because of low drain resistance caused by technology scaling. Therefore, a technique to reduce the offset voltage of the comparator without amplifier is strongly required. In recent years, some offset calibration techniques were proposed for dynamic latched comparator. In report [2], load capacitances of the comparator are controlled digitally to reduce the offset voltage. The resolution of the calibration is determined by the size of the load capacitance and digital word. This results in lower speed and wider area in a high resolution ADC. In report [3], the back gate bias voltage of the input transistor in the comparator is controlled by the digital-to-analog converter (DAC) to reduce the offset voltage. This method suppresses the deterioration of the latch speed compared with [2] because load capacitance of the comparator is not increased. However, necessity to divide the well of the input transistors causes an increasing in the area when using in a flash ADC. Moreover, the PVT variation may change the offset voltage in long time operation, because these

calibration techniques are usually executed before circuit operation.

On the other hand, dynamic offset cancellation techniques that require no static current were proposed for latched comparators [4, 5]. These techniques have tolerance to PVT variations because these are executed at every conversion. The charge-transfer preamplifier which does not need static power was proposed in [4]. The charge-transfer preamplifier looks difficult to increase conversion frequency since three phases, i.e. reset, pre-charge, and amplifying, are required for each conversion. In report [5], large size capacitance for offset canceling is needed for suppressing the deterioration of the input signal. Offset canceling capacitors have to drive the gate of the input transistor in the comparator.

In this paper, a low-offset latched comparator using new dynamic offset cancellation is proposed. The proposed comparator requires two phases; a reset mode and a regenerative mode. Furthermore, increasing offset voltage due to the input common mode variation can be suppressed by using the proposed method.

II. CIRCUIT DESIGN

A. Offset Voltage Contribution

The offset voltage of the comparator is caused by the mismatch of the transistor's threshold voltages. Figure 1 shows the conventional double-tail latched comparator circuit [6] and signal behavior. Moreover, each stage's contribution to the offset voltage of the conventional comparator obtained from Monte-Carlo simulation is shown in Fig. 2. The comparator circuit was designed using general 90 nm CMOS process. We set aspect ratio of all transistor to W/L = 1 μm / 0.1 μm. Supply voltage V_{DD} is 1.0 V and conversion frequency f_c is 500 MHz in this simulation.

The offset voltage of the 2nd stage is relaxed by conversion gain G_1 between the 1st stage and 2nd stage. On this account, mismatch of the 1st stage transistors becomes dominant in the comparator offset voltage. Furthermore, the most of the offset voltage of the 1st stage is caused by the mismatch of the input transistor's (M1, M2) threshold voltages. Therefore, the

offset voltage of the comparator can be suppressed by cancelling the threshold voltage mismatch of the input transistors.

In case the mismatch threshold voltage M1 and M2 can be cancelled, the offset voltage of the 2nd stage becomes dominant in the comparator offset voltage. G_1 must be kept high to reduce the 2nd stage offset voltage. However, G_1 is affected by the input common mode voltage V_{cm_i} variation. For instance, the offset voltage increases from 1.35 mV to 8.7 mV at 1 sigma when V_{cm_i} changes from 0.4 V to 0.9 V. This means that G_1 is decreased to 1/6 by changing the input common mode voltage. When the input common mode voltage is determined by the output common mode voltage of the pre-amplifier, the offset voltage will increase. Therefore, the circuitry that can decide G_1 without being affected by the input common mode voltage of the comparator should be developed.

B. Circuit Implementation

Figure 3 shows the proposed comparator using a new dynamic offset cancellation technique, and figure 4 shows its operation wave forms obtained from *Spectre* simulation. The proposed comparator consists of conventional double-tail latched comparator, offset canceling capacitors C_{c+}, C_{c-} and switches Mb, MR1 and MR2.

In a reset phase, ϕ_1 turns on, the common mode voltage V_{cm_i} input to the gate of the transistor M1' and M2'. At the same time, the bottom node of the capacitors V_{cb} connect to the bias voltage V_b. The top nodes of the capacitors V_{c+} and V_{c-} are charged up until when M1' and M2' are turned off. Therefore, voltages of the offset capacitors are given by

$$V_{c+} - V_{cb} \approx V_{cm\_i} - V_{th1} - V_b \tag{1a}$$

$$V_{c-} - V_{cb} \approx V_{cm\_i} - V_{th2} - V_b \tag{1b}$$

where V_{th1} and V_{th2} are threshold voltages of the M1' and M2' respectively. When ϕ_1 turns off, C_{c+} and C_{c-} maintain these voltages.

After the reset phase, ϕ_2 turns on, the input nodes of the comparator connect to the input signal; $V_{in+} = V_{cm\_i} + \Delta V_{in}$ and $V_{in-} = V_{cm\_i} - \Delta V_{in}$. The comparator starts to compare the input voltages when ϕ_L turns on. Because V_{cb} changes from V_b to GND, overdrive voltages of M1' and M2' are given by

$$V_{od1} = \Delta V_{in} + V_b \tag{2a}$$

$$V_{od2} = -\Delta V_{in} + V_b \tag{2b}$$

The threshold voltage mismatch of the input transistors can be cancelled because the overdrive voltage of the transistors does not depend on threshold voltage of the transistor. Moreover, the overdrive voltage is not affected by input common mode voltage V_{cm_i}. Therefore, even if V_{cm_i} is in high condition, comparator can operate with low offset voltage.
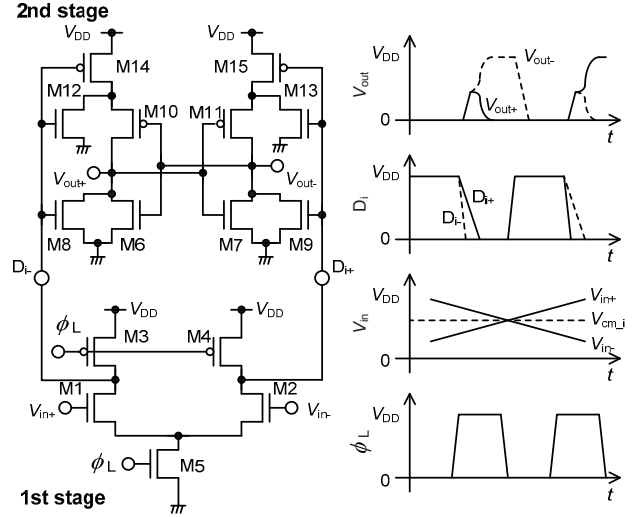

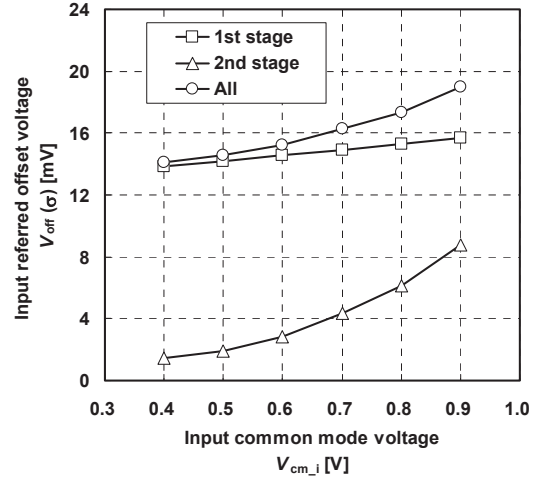Fig. 1. The conventional double-tail latched comparator.

Fig. 2. Each stage's contribution to the offset voltage.

After comparison, ϕ_R turns on to reset the offset canceling capacitor.

Figure 5 shows the relation between the input common mode voltage and offset voltage of the comparator obtained from 100 times Monte-Carlo simulation. Same size transistors are used in conventional and proposed comparators. The operating conditions are $V_{DD} = 1.0$ V, conversion frequency $f_c = 500$ MHz and the bias voltage $V_b = 100$ mV. The offset voltage of the proposed comparator is lower than conventional comparator in all condition. $V_{off}(\sigma)$ in the proposed comparator equals 2.6 mV, while conventional one equals 12.8 mV in case of $V_{cm\_i} = 0.6$ V. Moreover, $V_{off}(\sigma)$ in the proposed comparator increases by only 0.7 mV when V_{cm_i} changes from 0.6 V to 0.9 V. The simulation result shows that proposed comparator can suppress increase of offset voltage caused by V_{cm_i} variation.
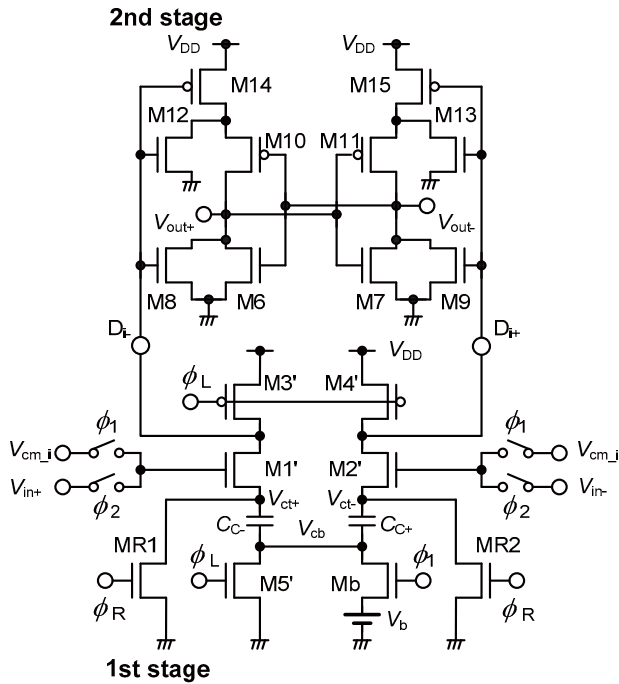
Fig. 3. The proposed comparator using dynamic offset cancellation technique.
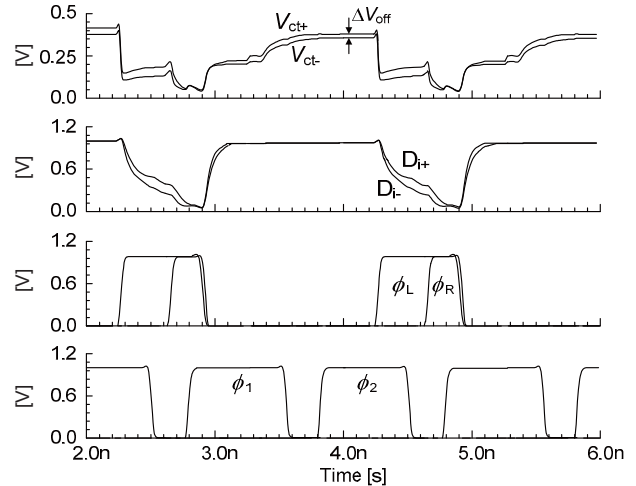

Fig. 4. Operation waveform of the proposed comparator.
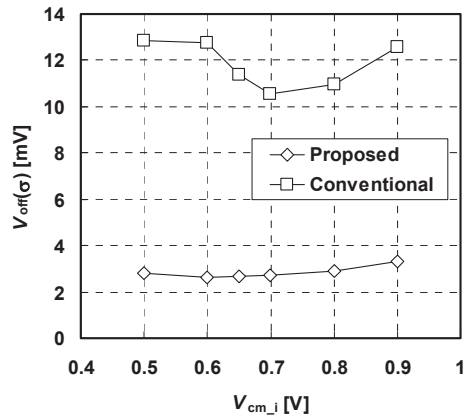

Fig. 5. Simulated offset voltage $V_{\text{off}}(\sigma)$ vs. input common mode voltage of the comparator.
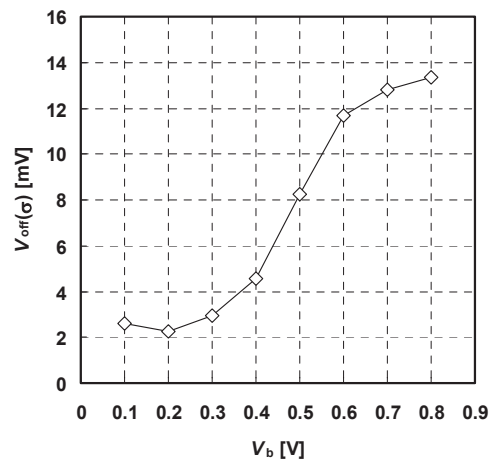

Fig. 6. Simulated offset voltage $V_{\text{off}}(\sigma)$ vs. bias voltage V_{b}.

Figure 6 shows the relation between the bias voltage V_{b} and the offset voltage $V_{\text{off}}(\sigma)$ in case of $V_{\text{cm\_i}} = 600$ mV. The simulation condition is the same as above. The simulation result shows that the offset voltage can be optimized by changing V_{b}. In this simulation, $V_{\text{off}}(\sigma)$ can be minimized when $V_{\text{b}} = 0.2$ V. The bias voltage V_{b} had better to be set low because the conversion gain G_1 is higher when the overdrive voltage of the input transistors is set lower. However, we should pay attention that too much small overdrive voltage causes a deterioration of the latch speed.

III.   MEASUREMENT RESULTS

A prototype comparator had been fabricated in a 90 nm 9M1P CMOS technology with a chip area of 0.0354 mm^2 as shown in Fig. 7. The chip area includes 64 comparators with SR latches to create a static output, the output selector circuit, input switches and decoupling capacitors. The core comparator size is only 152 μm^2. The offset voltage of the comparator is measured on 64 samples, $V_{\text{DD}} = 1.2$ V and $f_{\text{c}} = 500$ MHz. Simulated power consumption of the comparator is 39 μW. The measured power consumption of 64 comparators, I/O buffers, and clock driver all together is 4.8 mW.

Figure 8 shows the measurement result of the offset voltage versus the bias voltage V_{b} in case of $V_{\text{cm\_i}} = 0.6$ V. The measurement results show that the offset voltage can be suppressed by decreasing the bias voltage V_{b}. In case of $V_{\text{b}} = 0.15$ V, the offset voltage becomes minimum value: $V_{\text{off}}(\sigma) = 3.8$ mV.

The measurement result of the relation between the input common mode voltage V_{cm_i} and the offset voltage V_{off} (σ) is shown in Fig. 9. The bias voltage V_b is 0.15 V in this measurement. In case of V_{cm_i} = 0.5V, offset voltage is slightly higher. However, the offset voltage V_{off} (σ) is kept at around 4 mV even if the input common mode voltage is changed. Therefore, measurement results show that the proposed comparator can suppress the affect of the input common mode variation. The measured offset voltage is slightly higher than simulation result. This is because dummy metal affects to mismatch of the load capacitance that causes the comparator offset.

IV. CONCLUSION

A low offset, small area comparator using new dynamic offset cancellation technique is proposed. The proposed comparator consumes no static power. Measured results show the input offset voltage is improved from 12.8 mV to 3.8 mV by using proposed technique at 500 MHz conversion frequency.

Moreover, the proposed comparator has an advantage that the offset voltage does not change by increasing the input common mode voltage compared with the conventional comparator. The offset voltage of the proposed comparator increases by only 0.4 mV when the input common mode voltage changes from 0.6 V to 0.8 V, in contrast to the 2.0 mV increase for the conventional comparator.

REFERENCES

[1] B. Razavi, "Principle of data conversion system design," in IEEE press.

[2] G. Van der Plas, S. Decoutere, and S. Donnay, "A 0.19pJ/Conversion-step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process," in ISSCC Dig. of Tech. Papers, pp.566-567, Feb. 2006.

[3] E. Alpman, H. Lakdawala, R. L. Carley, and K. Soumyanath, "A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP digital CMOS," in ISSCC Dig. of Tech. Papers, pp. 76-77, Feb. 2009.

[4] K. Kotani, T. Shibata, and T. Ohmi, "CMOS Charge-Transfer Preamplifier for Offset-Fluctuation Cancellation in Low-Power A/D Converters," IEEE Journal of Solid-State circuits, vol. 33, no. 5, pp. 762-769, May. 1998.

[5] T. Kamimura, H. Horie, K. Ohhata, K. Yamashita, "Offset canceling method of high speed comparator for GS/s AD converter," IEICE General Conference Proceedings, C-12-34, p. 113, Mar. 2007.

[6] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs" in Proc. IEEE A-SSCC, 9-2, pp 269-272, Japan, Fukuoka, Nov. 2008.
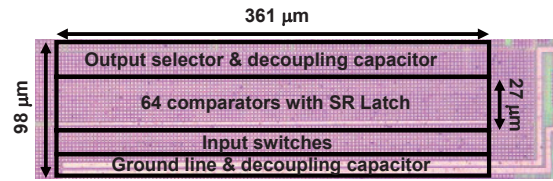
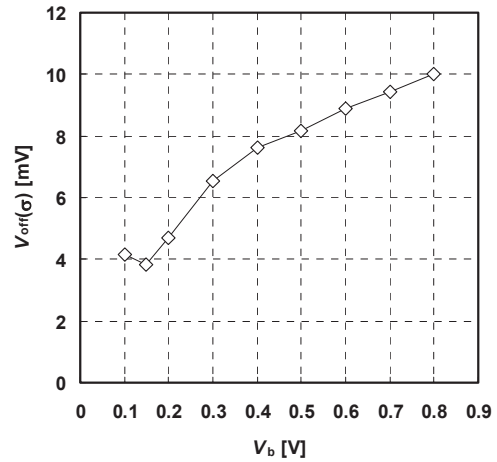Fig. 7. Chip photo of the proposed comparator.

Fig.8. Measured offset voltage V_{off} (σ) vs. the bias voltage V_b in case of V_{cm_i} = 0.6 V.
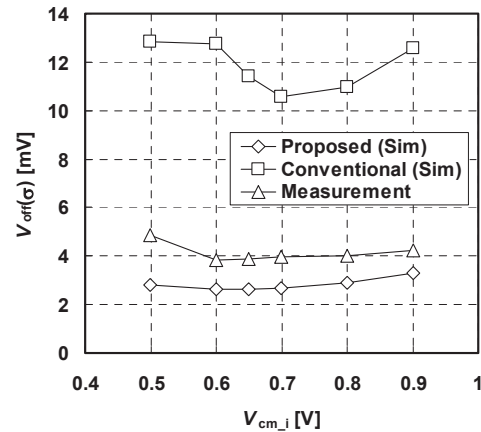

Fig. 9. Measured offset voltage V_{off} (σ) vs. input common mode voltage of the comparator in case of V_b = 0.15 V.