A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC

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***Abstract*—A 6 bit, 7 mW, 700 MS /s subranging ADC fabricated in 90 nm CMOS technology with SNDR of 34 dB for Nyquist input frequency is presented. The subranging architecture using CDACs, gate-weighted interpolation scheme, and digitally offset calibrating double-tail latched comparators has demonstrated an ultra low FoM of 250 fJ/conv. steps. and attractiveness for embedded IP for low power SoCs.**

I. INTRODUCTION

6 to 7 bit, several hundred MS/s to around 1GS/s ADCs are required for disk drive front-ends, backplane and ultra-wideband receivers.

Ultra-low power operation is the most important rather than increasing resolution and operating frequency for conventional ADC IP cores embedded in consumer SoC. This is because total power reduction is very crucial for portable applications and for addressing green IT regulation.

Conventionally flash architecture has been used for these targets; however it has an essential limitation to reduce conversion energy [1, 2]. An open-loop pipelined ADC has been also tried to this target [3]. SAR architecture has been recognized as the most energy efficient architecture, however not easy to increase the conversion rate up to GS/s operation. Multi-bit conversion in SAR ADC can increase conversion rate up to GS/s range [4] and interleaving technique can increase the conversion rate up to several tens of GS/s [5]. However reality looks difficult to keep the conversion energy low enough. Increase of occupied area and extra circuits; such as complicated clock generation and distribution will increase dynamic power dissipation, so much.

Subranging architecture looks good solution for this target, however the result has not been attractive. The FoM is 800 fJ/conv.steps [6].

Extreamly small FoM of 50 fJ/conv. steps has been attained in 5 bit 1.8 GS/s ADC using folding and subranging architecture and digitally calibrated dynamic comparators [7]. This architecture however looks difficult to increase resolution since the course conversion is realized by signal polarity swapping.

This paper will demonstrate the subranging architecture using CDACs, gate-weighted interpolation scheme, and digitally offset calibrating double-tail latched comparator is one of the strong candidates for this target.

II. ADC ARCHITECTURE

Figure 1 and figure 2 show our proposed subranging ADC architecture and timing chart.

The proposed ADC has one 4 bit course conversion unit and two 3 bit fine conversion units to make one bit redundancy. Two set of capacitive DACs (CDAC) are used like published ADC in [8] to generate voltages for fine conversion, instead of conventional resistor ladders, in order to reduce power dissipation and settling time, simultaneously. Furthermore, this CDAC acts as a sample and hold circuit (S&H) like CDAC in SAR ADCs. Double-tail latched dynamic comparators are used to reduce power consumption dramatically.

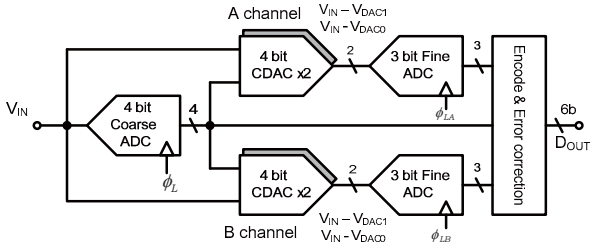

Fig.1. Proposed subranging ADC architecture.

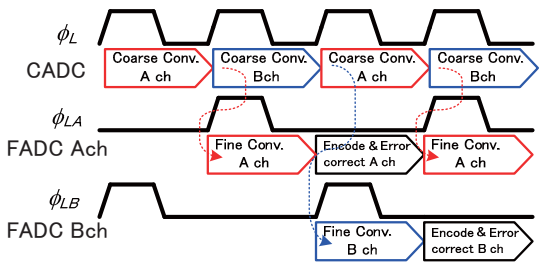

Fig. 2. Timing chart of the proposed ADC.

Gate-weighted interpolation technique in saturation region of MOS transistor is introduced to the dynamic comparators to reduce the number of S&H circuits and input capacitance, more over to realize the fine conversion without any reference voltages. A digital offset calibration technique is implemented to the fine conversion unit to increase the accuracy.

The course conversion unit is operated with conversion frequency and the fine conversion units is operated with half conversion frequency to relax the requirement for settling time and timing margins. Therefore power dissipation does not increase even if the circuit size is increased twice.

The fine conversion uses interpolation method shown in figure 3. A set of two differential outputs from CDAC_a and CDAC_b are sifted by 0.5 course LSB to realize overwrapping scheme (over range and under range) for fine conversion [9].

The interpolated voltages are composed with a set of two differential outputs from CDAC_a and CDAC_b and gate-weighted interpolation method. The interpolated voltages for the fine 3 bit conversion; V_{Pi} and V_{Ni} are;

$$V_{Pi} = \frac{(8-i)V_{INPa} + iV_{INPb}}{8} \quad (1a)$$

$$V_{Ni} = \frac{(8-i)V_{INNa} + iV_{INNb}}{8} \quad (1b),$$

where i is the number of interpolated voltage, V_{INPa} and V_{INNa} are the differential voltages from CDAC_a and V_{INPb} and V_{INNb} are the differential voltages from CDAC_b.

Thus no reference voltages are required for the fine conversion and consistence between course and fine conversion range is realized self-consistently.

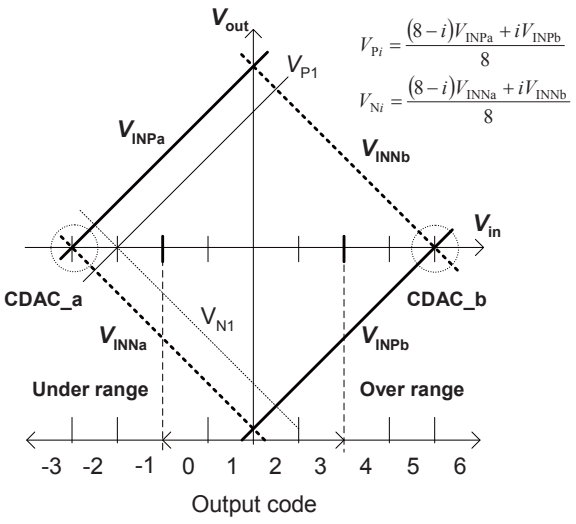

Fig. 3. Interpolated voltages and output code in fine conversion.

III. BUILDING BLOCKS

A. CDAC with S&H

CDAC is composed with 17 unit capacitances and one capacitance to generate offset voltage for over-range as shown in figure 4, where one side circuitry of differential scheme is illustrated. The unit capacitance is 15 fF and it can sample and hold the input signal like SAR ADC. Sampling switches uses bootstrapping technique to reduce on-resistance and the signal distortion.

A conventional reference generator using RDAC has a serious trade off between settling time and power consumption. Pre-charging technique might improve this trade off [10], however RDAC consumes power essentially, in contrast, CDAC does not consume any static power and free from this trade-off.

Figure 5 shows simulated DAC settling characteristics for about 160 mV voltage step, where switch becomes on at the time of 4.62 ns. The simulated settling time to the quarter LSB for 6 bit resolution (0.4%) is about 60 ps and power consumption is 360 μW at the operating frequency of 1 GHz.

CDAC has another advantage to the RDAC. Since it can act as a S&H circuit, power consuming S&H circuits that conventionally use sampling switch circuit and source follower buffer can be avoided.

B. Double-tail latched comparator

Double-tail latched comparator with saturation region gate-weighted interpolation circuits and capacitive offset calibration circuits shown in figure 6 are developed.

The improved double-tail latched comparator has been demonstrated to decrease the input noise to 0.7 mV at sigma, which is enough for 6 bit ADC [11].

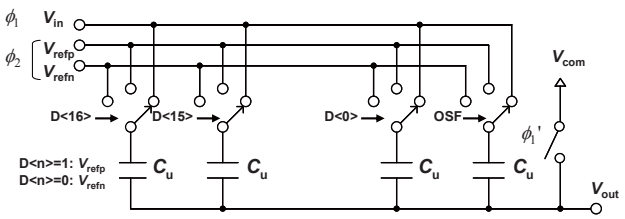

Fig. 4. CDAC with S&H circuit.

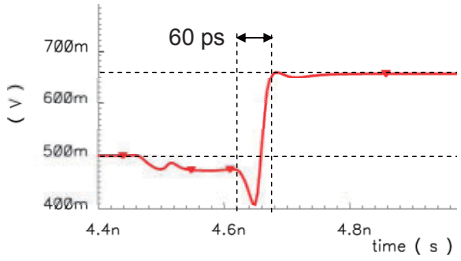

Fig. 5. Settling characteristics of CDAC.

Gate-weighted interpolation method is very effective to reduce the number of S&H circuits and input capacitance [12]. Conventional method however uses on-conductance of transistor in linear region; in contrast, we realized the interpolation in salutation region.

Drain current in saturation region of classical long channel MOS transistor exhibits square of (V_{gs}-V_T) characteristics and causes non-linearity error when using gate-weighted interpolation circuits. However, drain current of recent scaled MOS transistor is proportional to (V_{gs}-V_T), due to the heavy velocity saturation effect. The drain Current I_D can be expressed as,

$$I_D = \alpha W\left(V_{gs} - V_T^{'}\right) \quad (2),$$

where, α is a coefficient, W is gate width, and $V_T^{'}$ is effective threshold voltage.

The simulated non-linearity error is only less than 0.3% if $V_{gs} - V_T^{'} > 0.25\,\mathrm{V}$. Thus we used 2 bit interpolation for the course conversion. Also, we used 3 bit interpolation for fine conversion to realize A to D conversion without any reference voltages. The unit gate size is 2.4 µm/0.12 µm.

Also, we introduced offset calibration technique by adjusting capacitance [13] of the output nodes for 1st stage of the double-tail latched comparator. 4 bit binary weighted PMOS varactors are used. The gate size of unit varactor is 200 nm x 100 nm. Monte Carlo simulation shows the large mismatch of about 38 mVpp without calibration can be suppressed to 7 mVpp by this offset calibration The sigma value is about 0.9 mV and small enough for the quantization voltage of about 16 mV.

Figure 7 shows layout of this calibrating double-tail latched comparator. The size is only 5 µm x 65 µm, even if 4 bit registers are involved.

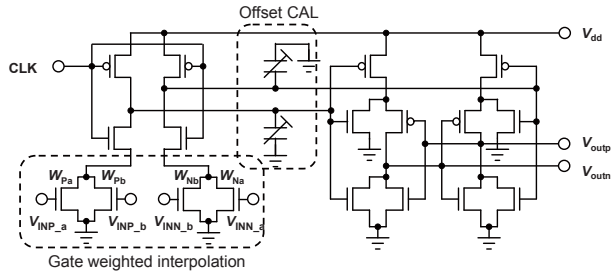

Fig. 6. Double-tail latched comparator.

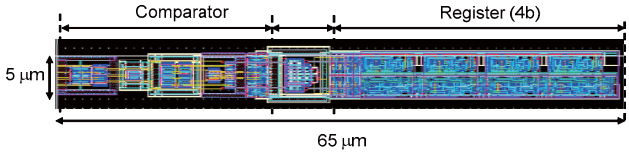

Fig. 7. Layout of the double-tail latched comparator.

The propagation delay at the input drive voltage of 1 mV is 140 ps and consumed energy for one conversion is 63 fJ/conv.. The input referred noise voltage is about 0.7 mV at sigma of which value is reduced to 64% for the comparator without offset calibration. The increase of node capacitance reduces input referred noise voltage. The power consumption of reference resistor ladder for the course conversion is 0.3 mW.

IV. EXPERIMENTAL RESULTS

The ADC has been fabricated in a 90 nm CMOS technology. Figure 8 shows the chip microphotograph and layout of the ADC, which occupies an active area of 0.13 mm^2.

Figure 9 shows the measured DNL and INL at the conversion rate of 700 MSps after the offset calibration. The DNL is less than +/- 0.6 LSB and INL is less than +/- 0.8 LSB.

Figure 10 shows a spur free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) versus the sampling rate when the input signal frequency is about 50 MHz. The SNDR keeps higher than 34 dB (5.3 bit) until 700 MS/s, however suddenly drops down to 20 dB (3.0 bit) at 800 MS/s.

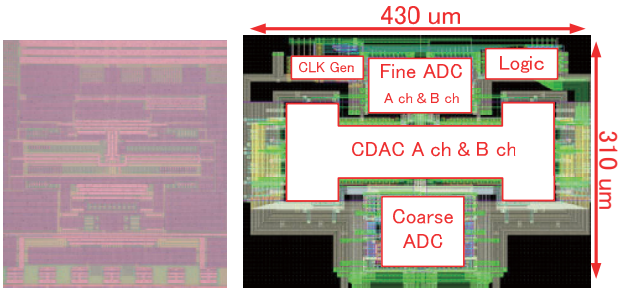

Fig. 8. Chip micrograph and layout

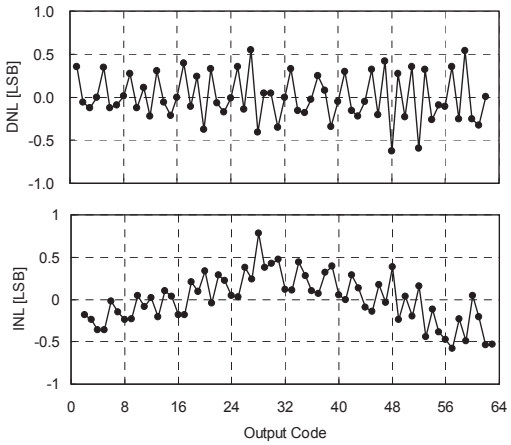

Fig. 9. INL and DNL at 700 MSps after CAL.

Figure 11 shows dependency of SNDR on the input frequency at 700 MS/s. The curve keeps SNDR of 34 dB (5.3 bit) until the Nyquist frequency of 350 MHz. The power consumption is only 7 mW at the conversion rate of 700 MS/s. The FoM is calculated only 250 fJ/conv. steps.

Table I summarizes ADC performance of our work and previously published ADCs for similar targets.

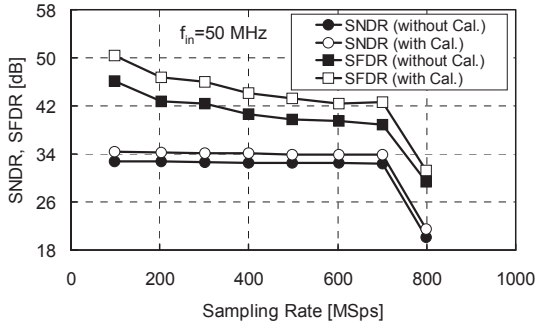

Fig. 10. SFDR and SNDR vs. sampling rate.

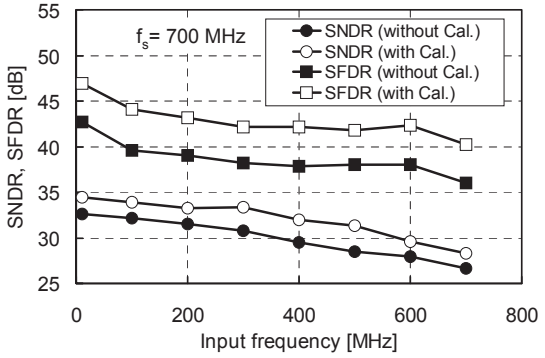

Fig. 11. SFDR and SNDR vs. input frequency.

TABLE I

ADC PERFORMANCE SUMMARY.

	[1]	[2]	[3]	[4]	[6]	This work
Resolution (bit)	6	6	6	6	6	6
fs (Gs/s)	0.8	1.2	0.7	1.25	1	0.7
SNDR (DC/Nyq.)	35/32	34/33	31/30	34/28	35/33	35/34
Pd (mW)	12	75	24	32	30	7
Active area (mm^2)	0.13	0.43	0.052	0.09	0.18	0.13
Vdd (V)	1.2	1.2	1.2	1.2	1.2/1.0	1.2
FoM (pJ)	0.44	2.17	1.31	1.22	0.8	0.25
CMOS Tech. (nm)	65	130	130	130	90	90
Architecture	Flash	Flash	Pipeline	2b-SAR	Subrange	Subrange

V. CONCLUSION

We have demonstrated the subranging architecture using CDACs, gate-weighted interpolation scheme, and double-tail latched comparator is very effective for ultra low energy operation with high speed conversion. However measured results indicate the offset calibration isn't sufficient yet and conversion speed is lower than the expectation. We believe the measured results do not reach the potential performance. Further optimization will provide more attractive results.

ACKNOWLEDEMENT

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