60 GHz Injection Locked Frequency Quadrupler with Quadrature Outputs in 65 nm CMOS Process

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***Abstract*— This paper presents a LC-based sub-harmonic injection-locked frequency quadrupler which multiplies a 15 GHz input to 60 GHz quadrature(I/Q) output signals. The proposed quadrupler can use a lower-frequency PLL for incident signal than doublers and triplers, which is very advantageous to implement a wide-tuning and low-phase-noise PLL. The proposed frequency quadrupler is implemented by using a 65 nm CMOS process. It consumes 5.9 mW with a 0.6 V supply voltage, and the core layout area is 300 μm $\times$ 60 μm.**

***Index Terms*— 60 GHz, mm-wave, CMOS, injection-locked, frequency mulitiplier, quadrupler, and frequency synthesizer.**

I. Introduction

Spurred by the possibility of reaching very high data rates at high frequencies, recent interest in the millimeter-wave frequency band (30-300GHz) has resulted in a growing research field [1]–[3] to make cost effective integrated millimeter-wave transceivers. One of the main applications is for the IEEE 802.15.3c millimeter-wave short range radio standard. A license-free 60 GHz band used in Europe and the USA, is allocated in Japan as shown in Fig. 1. Many problems, however, still abound this field as the challenges of designing transceivers at such frequencies bring about various problems negligible at the lower radio frequencies. One of the blocks which poses a challenge is the frequency synthesizer and its important component, the voltage controlled oscillator. In general, millimeter-wave voltage controlled oscillators (VCO) should achieve many characteristics similar to VCOs at lower cellular bands. These include low phase noise, low power consumption, reasonable output power level, reasonable tuning range and a relatively low VCO gain (sensitivity to tuning capacitor) such that when it is used within a PLL the design consideration for the loop filter does not become too stringent to achieve a reasonable spur level. However, all these factors become increasingly difficult at millimeter-wave frequencies. At millimeter-wave frequencies the resonator becomes increasingly sensitive to capacitance, decreasing the tank impedance at a faster rate than at lower frequencies as the capacitance size increases. Further current may be increased, to increase the transconductance of the differential pair, however, this increase in transconductance has limitations, and in order to obtain required phase noise characteristic, the size of the differential pair must be further increased. This increase in current and the differential pair size, however, also increases its power consumption and associated parasitic capacitance which may be neglected at lower frequencies, but are significant at millimeter wave frequencies, resulting in diminishing returns.

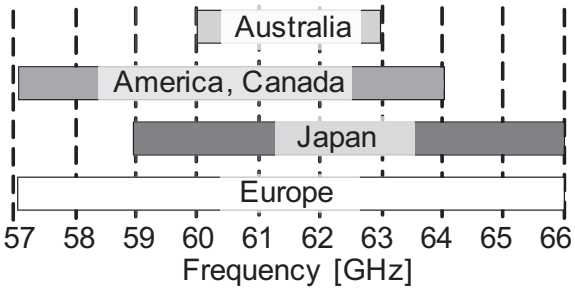


Fig. 1. The license-free 60 GHz band.

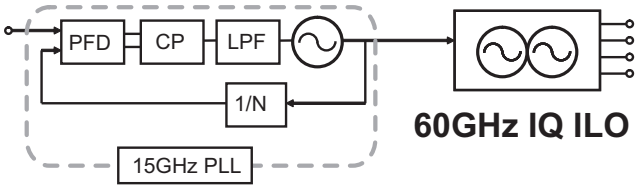
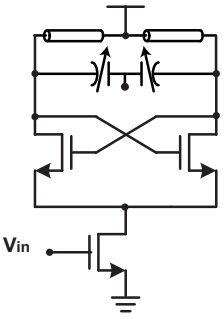


Fig. 2. The proposed PLL archtecture

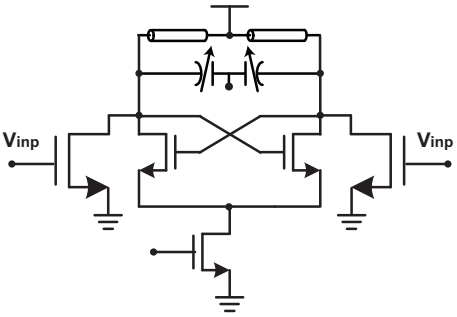
To try to solve this problem, using frequency multiplier has been proposed [4]. The architecture consists of frequency multiplier and low frequency incident PLL. Phase noise characteristic of frequency multiplier depends on phase noise characteristic of input signal, and low power and wide tuning range frequency synthesizers can be achieved easily. The higher multiplying ratio is advantageous in power consumption and phase noise characteristics of the incident PLL. On the other hand, quadruplers using the harmonic response require larger power consumption because the quadrupler usually consists of two doublers. Thus, an injection locked frequency quadrupler is proposed in this paper, which uses the direct injection technique for multiply-by-4 operation as shown Fig. 2.

II. Design optimization of injection-locked oscillators

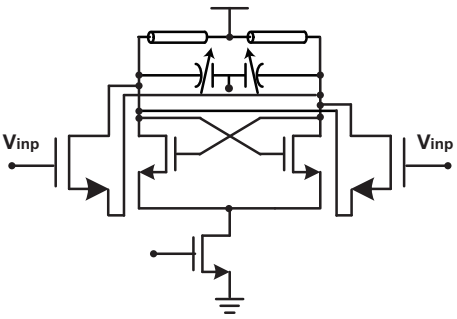
The limited locking range of the conventional CMOS injection-locked oscillator shown in Fig. 3 (a) is apparently caused by the inefficient injecting path through the tail transistor. Especially at higher frequencies, the injecting current of



(a) Injection from tail transistor.



(b) Injection directly from switch transistors placed in each output node.



(c) Injection directly from switch transistors placed between each output node.

Fig. 3. Simplified schematics of various injection locked oscillators.

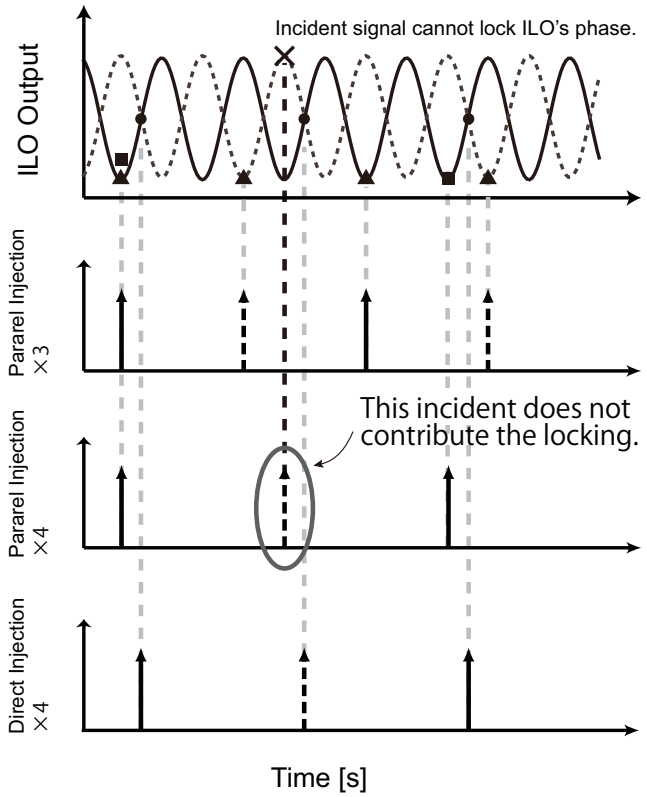


Fig. 4. Injection phase.

tail transistor vanishes into the capacitance at the tail node. As a further drawback of the conventional differential injection-locked frequency divider, the tail transistor has to have larger gate width to provide the large input transconductance, which causes larger power consumption. The approach of [4], [5], injecting currents directly into the LC-resonator, was further optimized and resulted in an improved direct injection scheme based on a MOS transistor switch in the LC-resonator. The circuit can avoid the feed-through of the input signal. The incident signal is provided through the extra transistor, which can be designed much smaller than the tail transistor due to the more efficient injection. The switch transistor is usually implemented by an NMOS transistor for high frequency operation.

There are some differences between the parallel and direct injections. In the parallel injction topology as shown in Fig.3 (b), the switch transistors operate to fix the output node voltage to the ground. On the other hand, in the direct injection topology as shown in Fig.3 (c), the switch transistors operate to equalize each output node voltage. Fig. 4 shows the injection phase of the parallel and direct injections. In the parallel injection topology, the locking current is injected while the voltage output is close to the ground level. On the other hand, the locking current in the direct-type is injected at the crossing points. Furthermore, the possible multiplying ratio is also different as shown in Fig. 4. When multiplied by odd-number, *e.g.* 3, parallel injection is better because each differential incident signals can lock injection-locked oscillator (ILO) output. On the other hand, for even-number injections, only one side in differential signal can contribute the injection locking as shown in Fig. 4, so the parallel injection is not so good for the even-number injection. Thus, in this paper, direct injection is employed for multiplying ratio of 4. In the direct injection topology, both incident signals can contribute the injection locking as shown in Fig. 4.

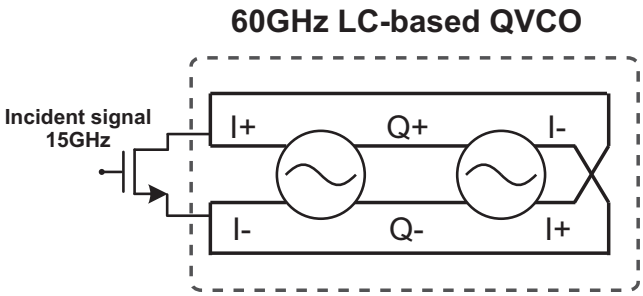


Fig. 5. Block diagram of the ILO.

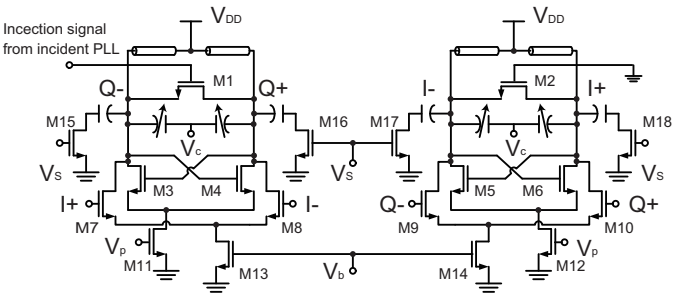


Fig. 6. The circuit schematic of the proposed ILO.

III. The proposed injection-locked frequency quadrupler

Fig. 5 shows the block diagram, and a NMOS-cross-coupled quadrature LC-VCO is employed for high frequency operation and a low supply voltage, which has an NMOS switch transistors M1 for injection locking and M2 for considering parasitic capacitance of switch transistor. A single-side incident signal is injected because parasitic capacitance of switch transistors is limited at higher frequency *e.g.* 60 GHz. Fig. 6 shows the schematic of the proposed ILO, and switched capacitor is utilized for coarse tuning to obtain required frequency tuning range and PMOS varactors for continuous tuning. M7 ~ M10 tune each output signal phase of the ILO, and M11, M12 and M13, M14 tune current of phase tuning transistors and cross-couple transistors.

IV. Measurement result

Fig. 7 shows a chip micrograph of the proposed ILO, which is fabricated by using a 65 nm CMOS process. The core size is 300 μm × 60 μm.

The measurement setup of the output spectrum is shown in Fig. 8. On wafer probes were used to probe the die directly, while DC probes provides the bias. The output signal is amplified by a V-band amplifier. The signal is then mixed with a harmonic mixer to a low IF by a local oscillator provided by the spectrum analyzer, and the output spectrum is measured.

Fig. 9 shows the output spectrum of ILO without spurious tones. Fig. 10 shows measured locking range of ILO. Table I summarizes the measured results. The locking range may be narrow, but can be extended by tuning bias condition of ILO as 56.3 to 63.3 GHz.

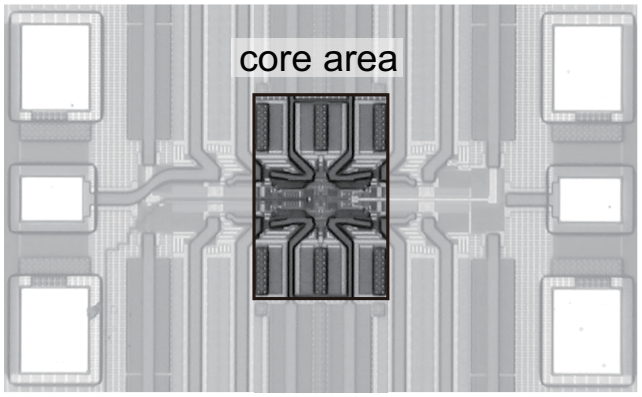


Fig. 7. Chip micrograph of fabricated ILO.

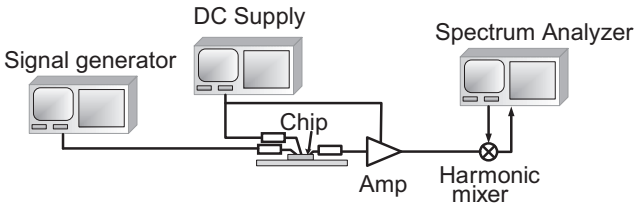


Fig. 8. Measurement setup.

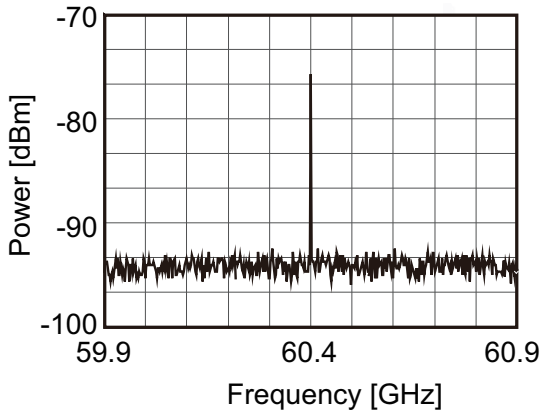


Fig. 9. ILO output spectrum.

TABLE I
ILO performance summary.

	This work	ISSCC2008 [4]
Technology	CMOS 65nm	CMOS 90 nm
Supply voltage V_{DD}	0.6 V	1.0 V
Injection method	direct	parallel
Multiple ratio	4	3
Incident PLL	15 GHz	20 GHz
Tuning range	56.3 ~ 63.3 GHz	59.7 ~ 60.6
Locking range with fixed bias condition	60.36 ~ 60.44 GHz	56.5 ~ 64.5 GHz
Power consumption	3.1 ~ 6.8 mW	9.6 mW

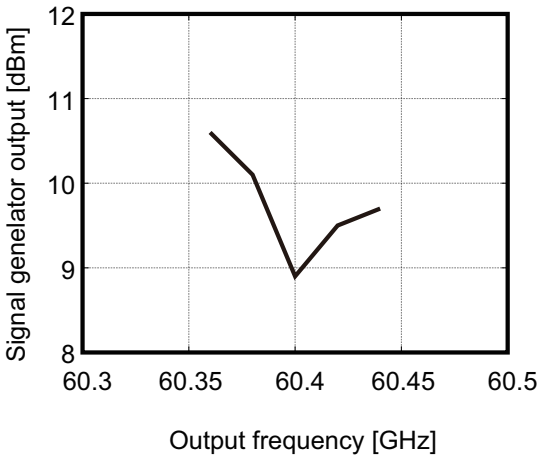


Fig. 10. Measurement result of locking range

V. Conclusion

A low-power sub-harmonic injection-locked I/Q quadrupler, which is implemented by using a 65 nm CMOS process, is presented to multiply lower frequency signal. The proposed topology consists of a transmission-line-based resonator and an NMOS cross-coupled pair and switched capacitors and PMOS varactors and NMOS switches directly coupled to the tank. The proposed frequency quadrupler achieves 56.3 ~ 63.3 GHz continuous frequency tuning with 80 MHz locking range. The ILO can be locked widely by suitable bias condition tuning. The frequency quadrupler consumes 3.1 ~ 6.8 mW with a 0.6 V power supply.

Acknowledgment

This work was partially supported by MIC, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS Receiver Front-End With Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, April 2008.

[2] C. Doan, S. Emami, D. Sobel, A. Niknejad, and R. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Communications Magazine*, vol. 42, no. 12, pp. 132–140, Dec. 2004.

[3] E. Laskin, M. Khanpour, R. Aroca, K. Tang, P. Garcia, and S. Voinigescu, "A 95GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65nm Digital CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2008, pp. 180–605.

[4] W. L. Chan, J. R. Long, and J. J. Pekarik, "A 56-to-65 GHz Injection-Locked Frequency Tripler with Quadrature Outputs in 90nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2008, pp. 480–481.

[5] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1170–1174, July 2004.