60GHz Injection Locked Frequency Quadrupler with Quadrature Output in 65nm CMOS Process

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Outline

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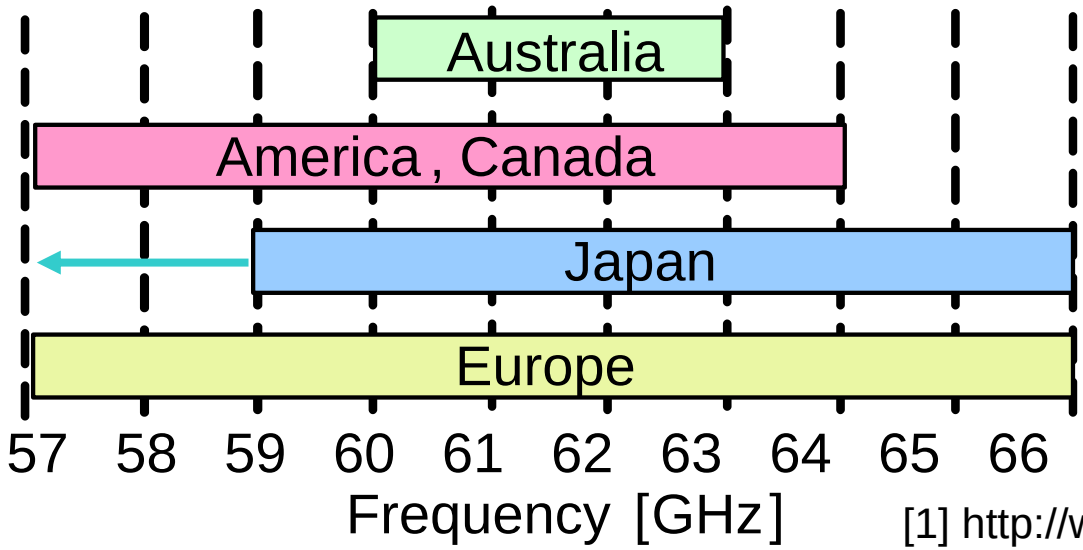
- **Background**
- **Principle of 60GHz synthesizers**
- **Design and measurement design**
- **Summary**

Motivation

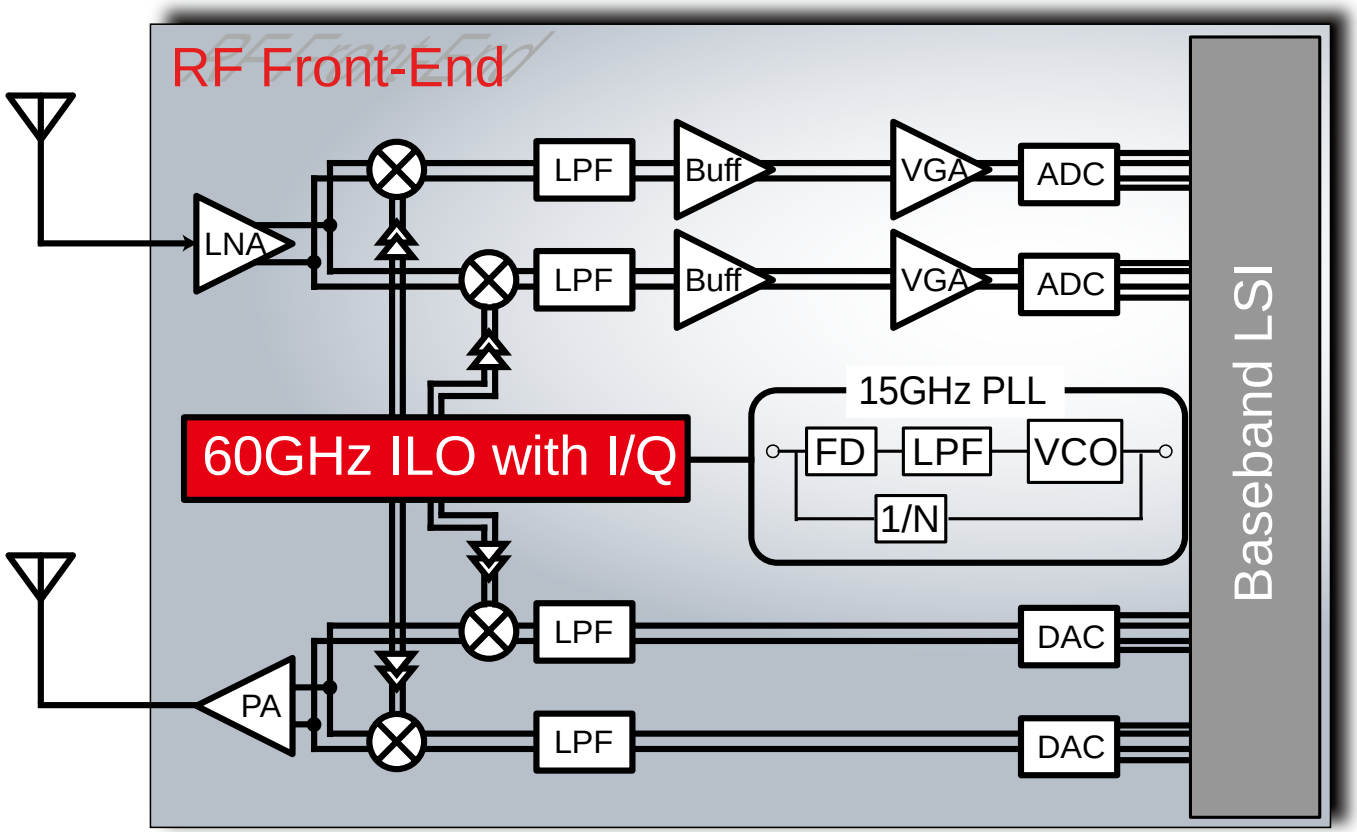
60GHz unlicensed band



[1] http://www.tele.soumu.go.jp

- **9GHz-BW around 60GHz**
  - ⇨ **Several-Gbps wireless communication**
- **Use of CMOS process**
  - ⇨ **Fab. cost is very important to generalize it. RF&BB mixed chip can be realized.**

Our target



60GHz 2.16GHz-full 4ch direct-conversion by CMOS
QPSK 3Gbps & 16QAM 6Gbps & 64QAM 9Gbps
IEEE 802.15.3c conformance

Performance of CMOS

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Advantages

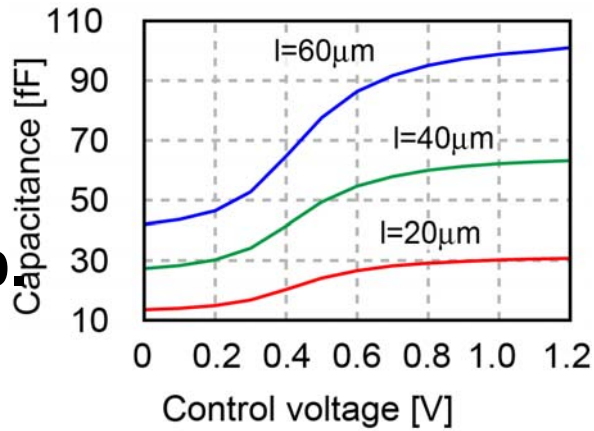
- Mixed with digital components
  - Cost
  - Digital assist
- Higher f_T and f_{max}

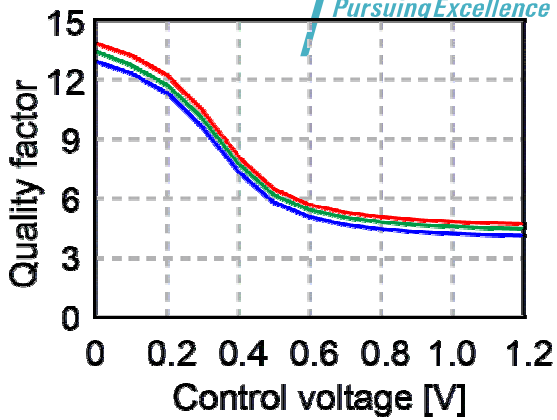
Weak

- Low gain
- Lossy passive devices
- Larger noise
- Increase the cost as more miniaturization

Performance of passive devices

- **MOS varactor**
  - **-Small C_{max}/C_{mim}**
  - **-Large parasitic cap**
  - **-Low quality factor**





- **Switched capacitor array**
  - **-Low quality factor**

- **Inductor**
  - **-Small inductance**
  - **-Large loss due to skin effect**

Possibilities for quadrature 60GHz LO

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- **60GHz VCO with RC polyphase filter**
  - + Smaller layout area
  - - Phase mismatch due to wide required frequency range
  - - Larger loss due to parasitic loading and small R

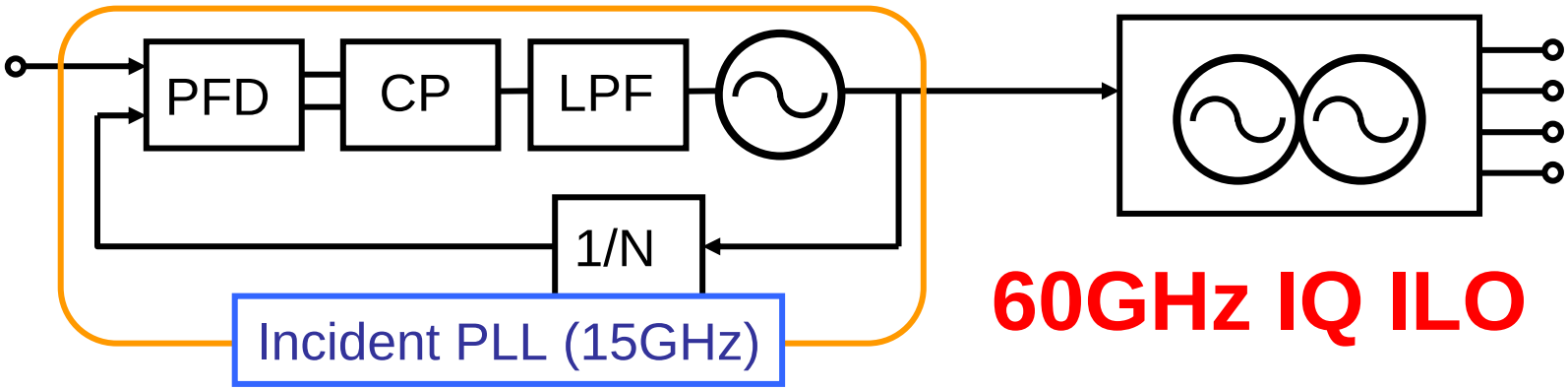
- **60GHz QVCO**
  - + Robust and reliable
  - - Narrower tuning range
  - - Worse phase noise

- **VCO with harmonic doublers**
  - + Better phase noise
  - - Larger power consumption

Quadrature LC-VCO

15GHz x 2 x 2 =60GHz
or
30GHz x 2 =60GHz

Injection locked oscillator



Using injection locked oscillator

- **Phase noise･･･Depends on incident PLL**
- **Frequency tuning range･･･Required**
- **Circuit area･･･Larger**

Performance of passive devices

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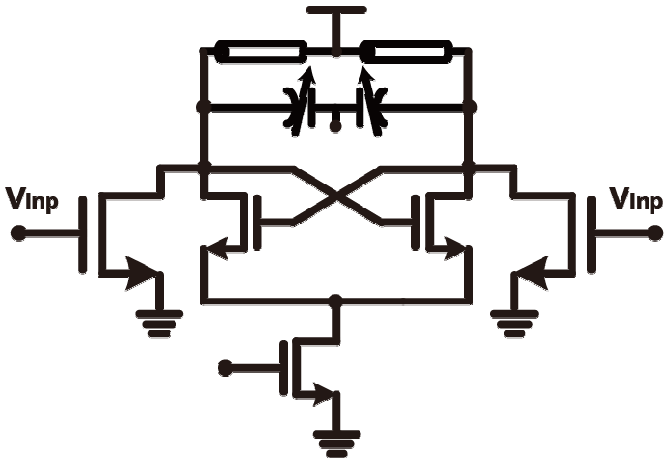
Multiple ratio		2	3	4
Output [GHz]		57 - 66		
Input [GHz]		28.5 - 33	19 - 22	14.2 - 16.5
Quality factor of	Inductor	22	22	22
	Capacitor	17	26	**35**
Capacitance		severe	middle	capable
Phase noise		poor	middle	**good**
Locking		so-so	severe	severe

Multiple ratio is determined by phase noise of incident VCO

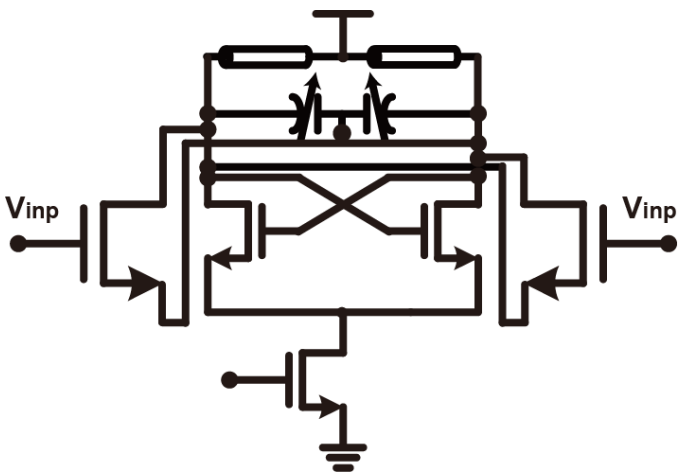
Comparison of injection method



Parallel-type

feature:

- **Locked at low output voltage**
- **Hard to multiple by even number**

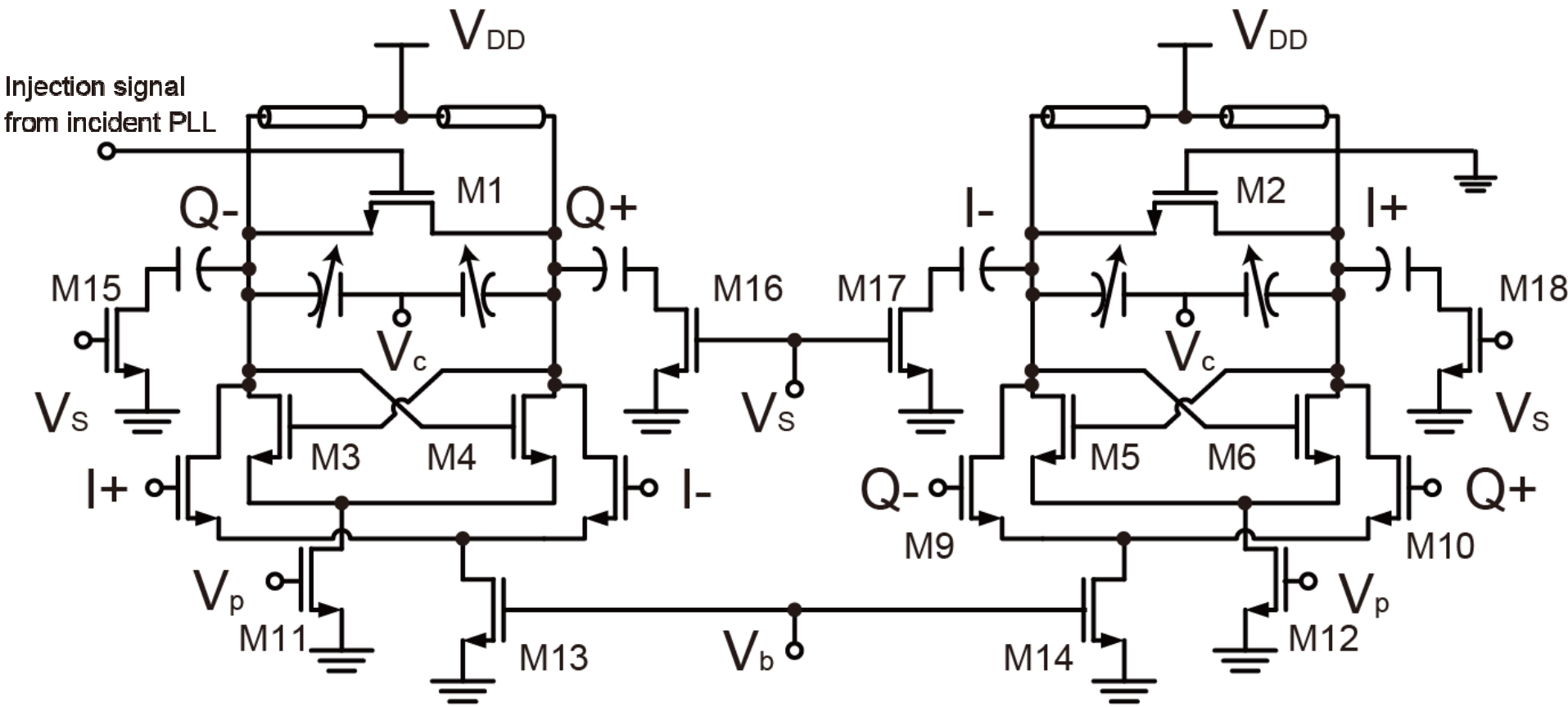


Direct-type

feature:

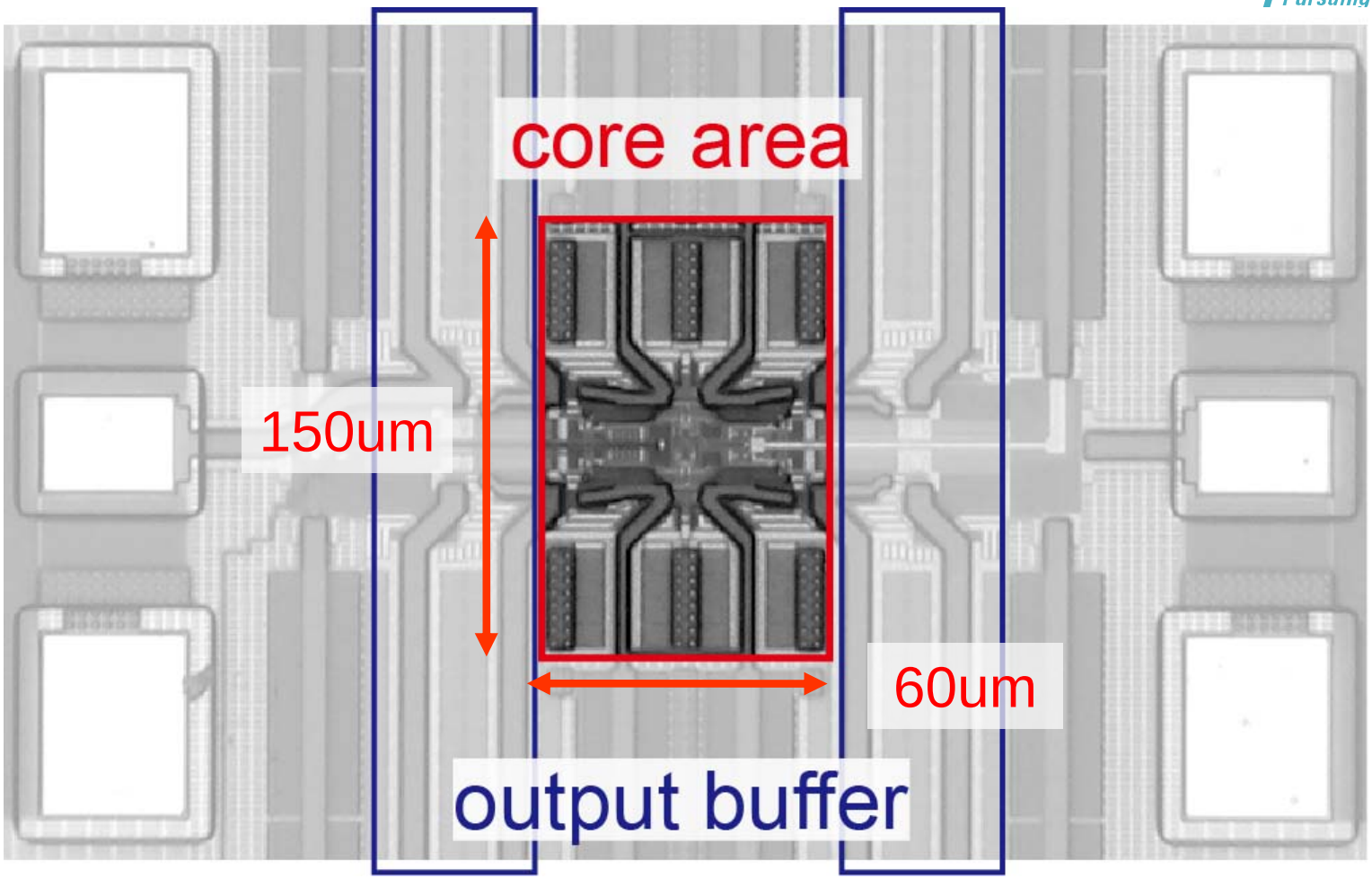
- **Locked at cross point**
- **Able to multiple by even number**

Schematic of the ILO



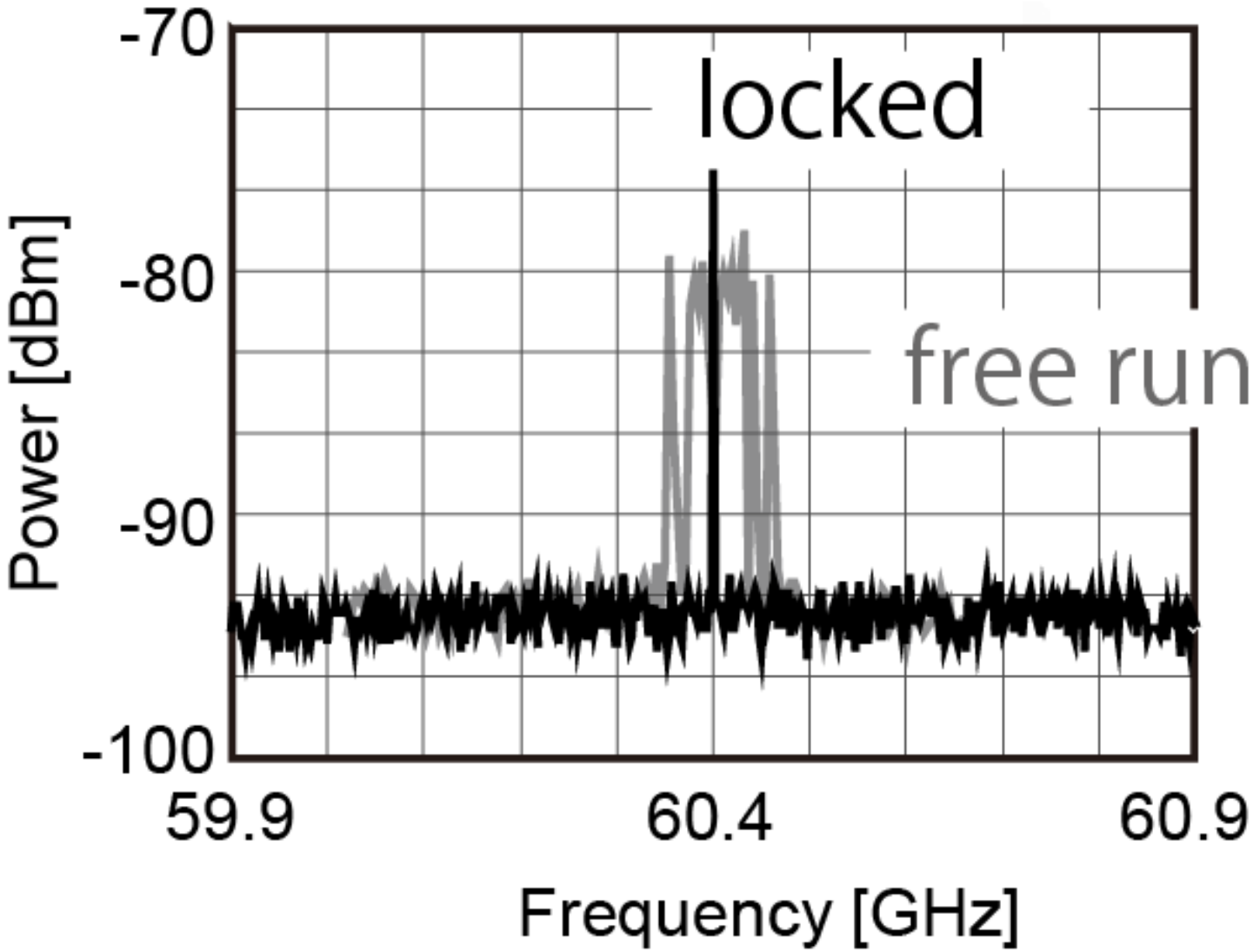
Target frequency range : 57 to 66 GHz

Chip micrograph

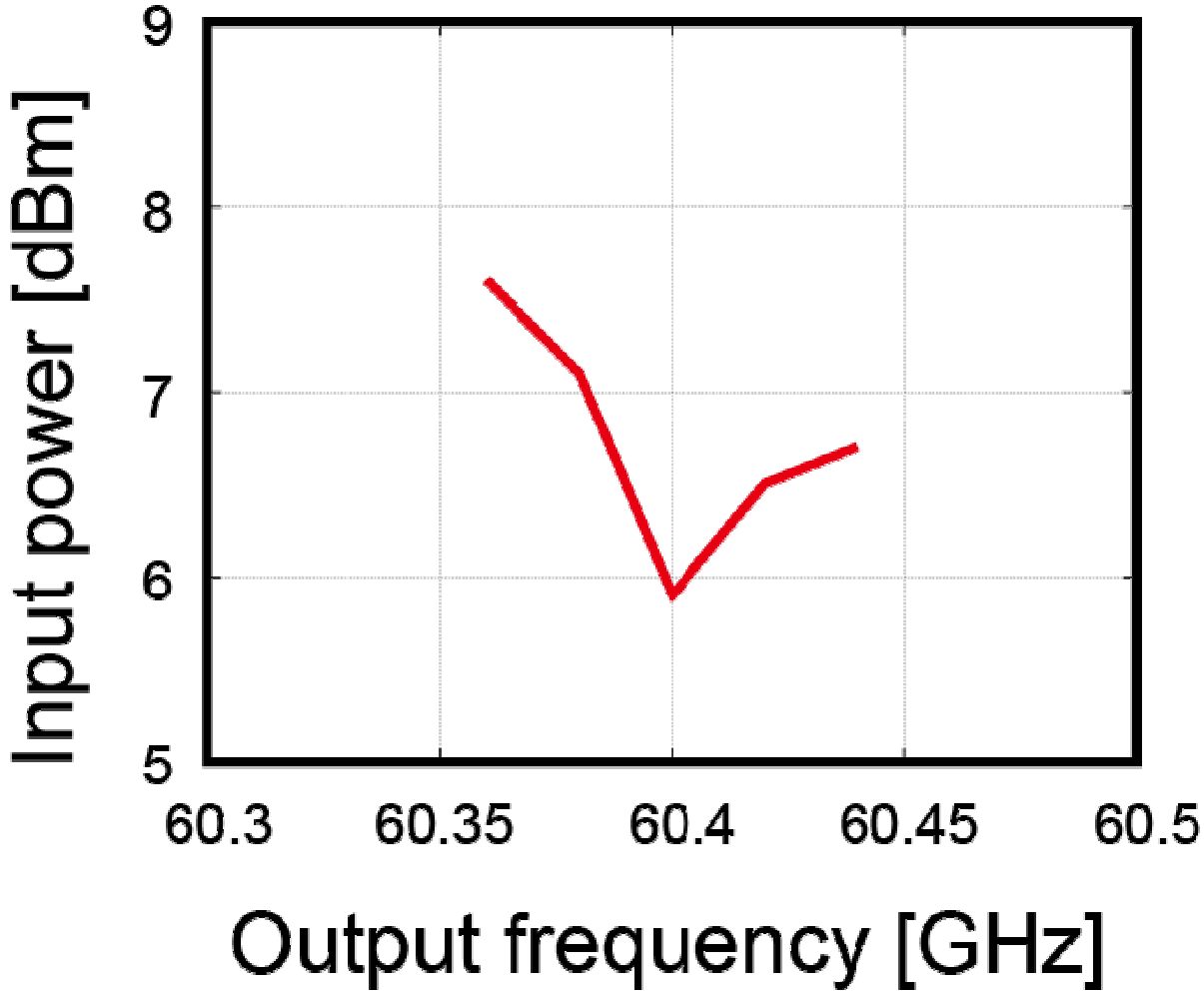


Fabricated by using 65nm CMOS process

Measured spectrum



Measured efficiency



- Input matching is not included in TEG

ILO measurement summary

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	This work	ISSCC2008[1]
Technology	CMOS 65nm	CMOS 90nm
Power supply	0.6 [V]	1.0 [V]
Injection method	Direct	Parallel (with Polyphase filer)
Multiple ratio	4	3
Input	15 [GHz]	20 [GHz]
Tuning range	56.3 - 63.3 [GHz]	60.0 [GHz] (fixed)
Locking range	60.36 - 60.44 [GHz]	56.5 - 64.5 [GHz]
Power consumption	3.1 - 6.8 [mW]	9.6 [mW]

[1] W. L. Chan, et. al, ISSCC2008

Conclusion

- **A transmission-line-based frequency quadrupler using direct injection technique is proposed.**
- **The proposed ILO can achieve wide tuning range with small power consumption.**

60GHz channel plan

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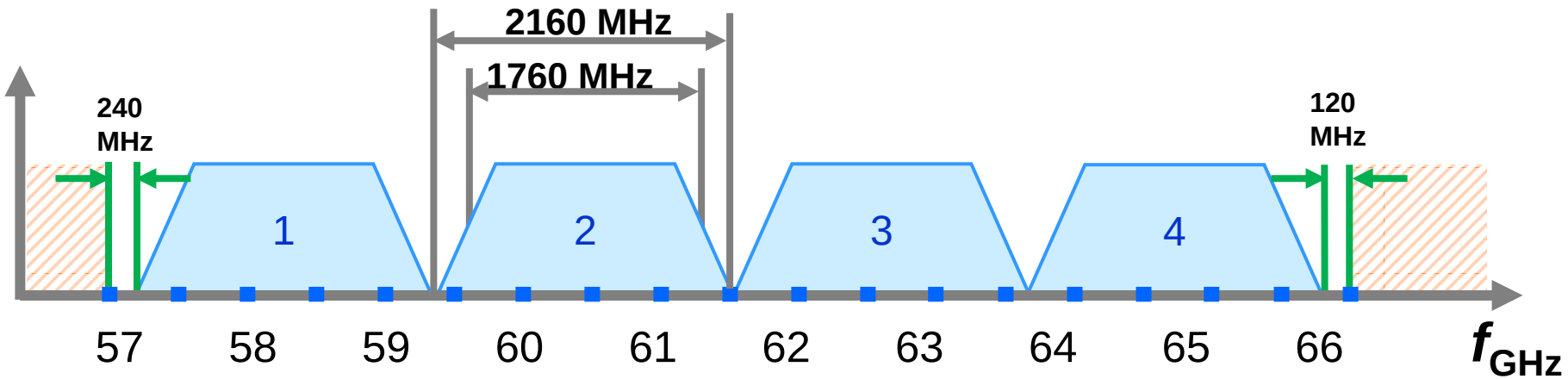
IEEE802.15.3c

Ref: IEEE 802.15-09-192-003c with draft doc.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)	Roll-Off Factor
A1	57.240	58.320	59.400	1760	0.227
A2	59.400	60.480	61.560	1760	0.227
A3	61.560	62.640	63.720	1760	0.227
A4	63.720	64.800	65.880	1760	0.227



4 channels of 2.16GHz-BW

Measurement setup