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Technology Trend of ADCs

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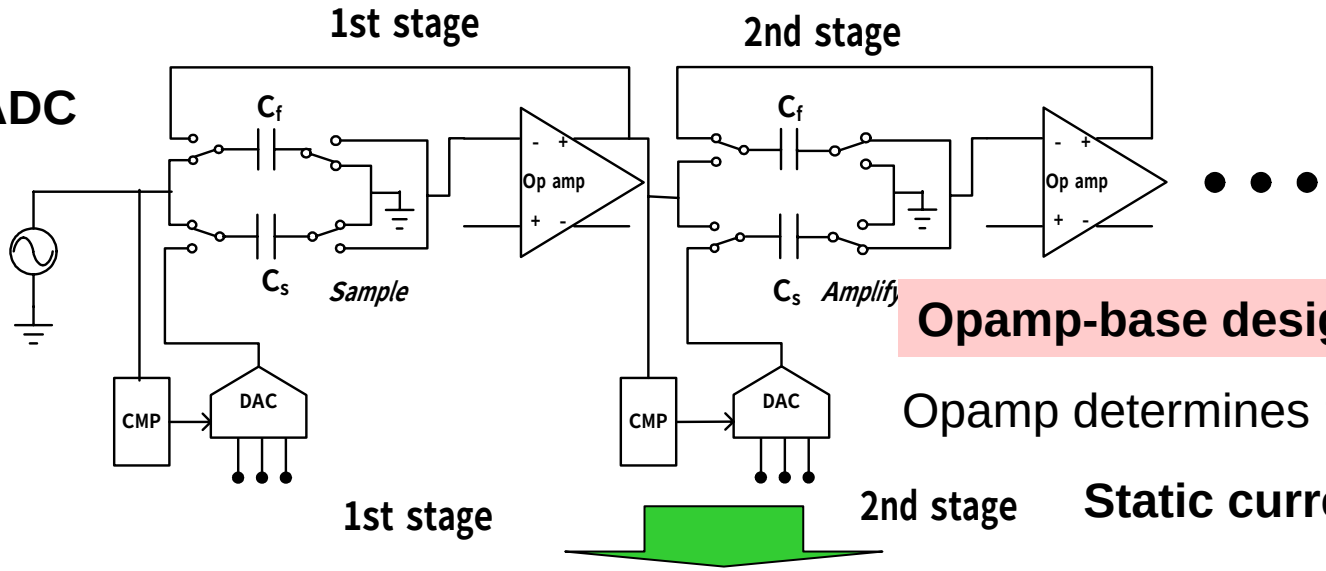
Mega-technology trend in ADCs

A major conversion scheme of ADCs is now changing from pipeline to SA

Pipeline ADC



Opamp-base design

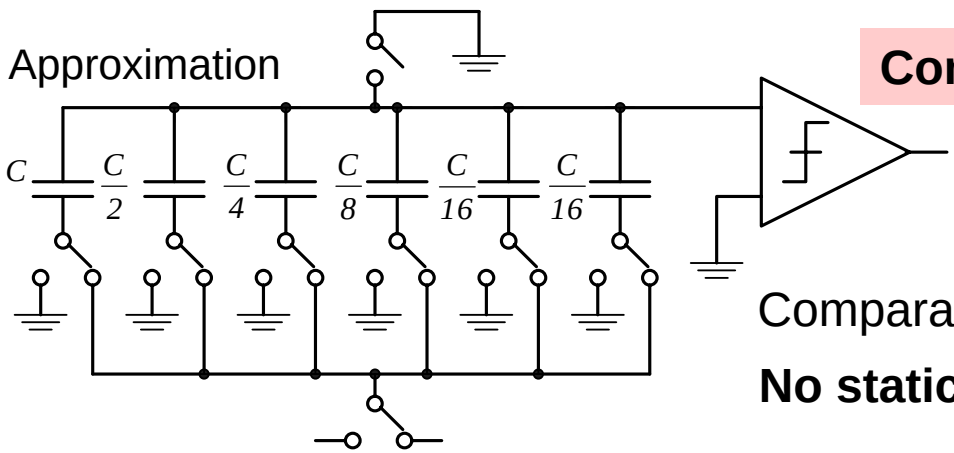
Opamp determines performance

Static current flows

1st stage → 2nd stage

SA ADC

SA: Successive Approximation



Comparator-base design

Comparator determines performance

No static current flows

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Issues of pipeline ADCs

(current major ADC architecture)

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Pipeline ADC

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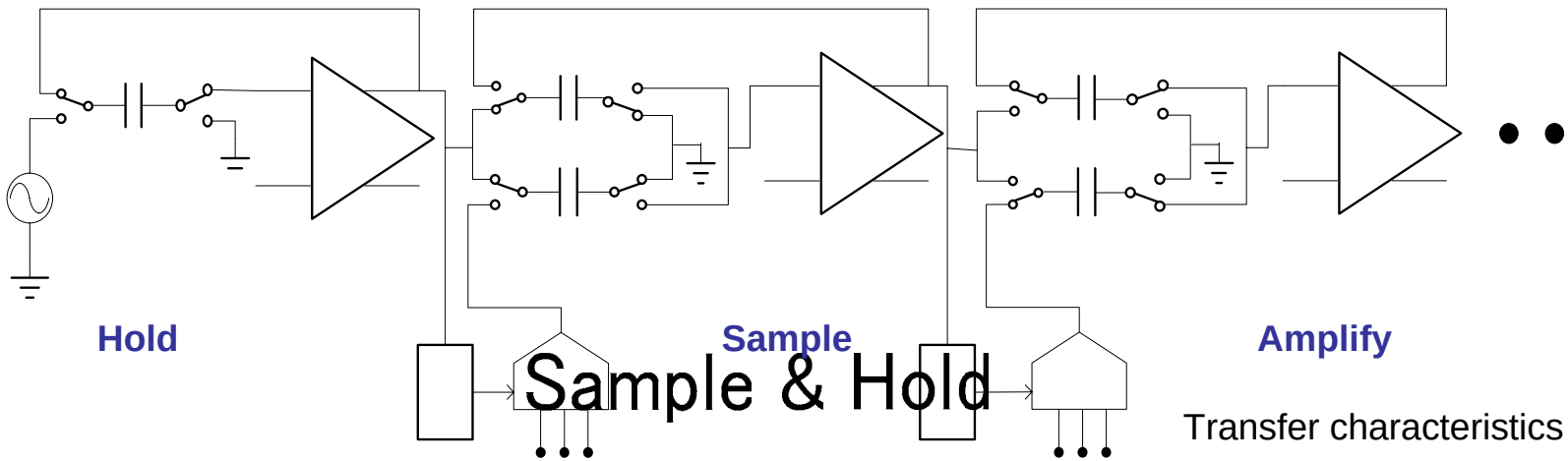
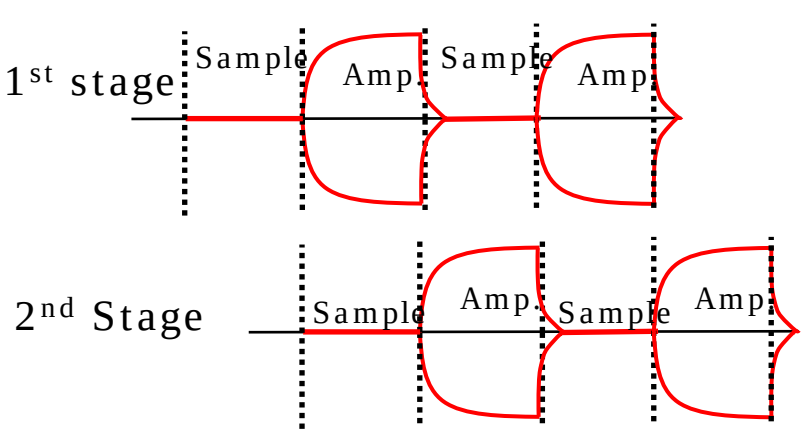
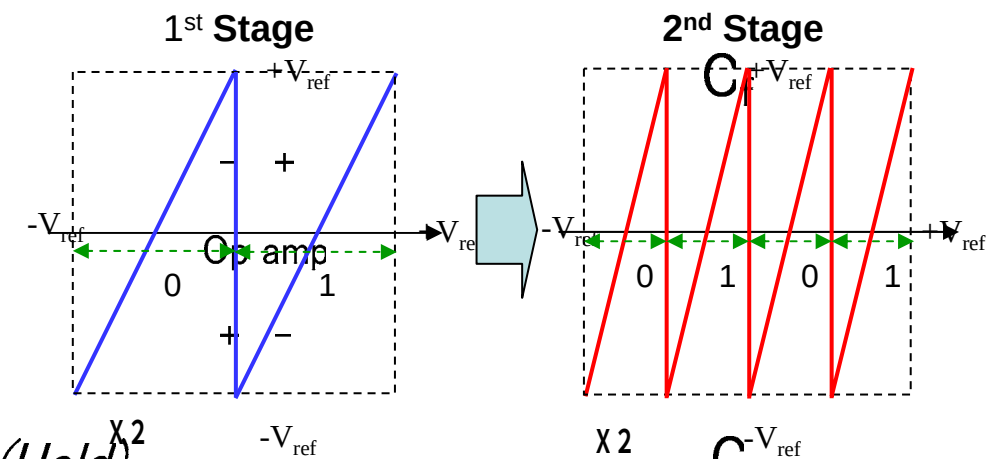
Folding I/O characteristics makes higher resolution along with pipeline stages.







Issues of pipeline ADCs

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Major issues of pipeline ADCs are caused by OpAmp.

Scaled CMOS (90nm) can't realize high OPamp Gain.

$$G_{DC}(dB) > 6N + 10$$

$$10b : 70dB$$

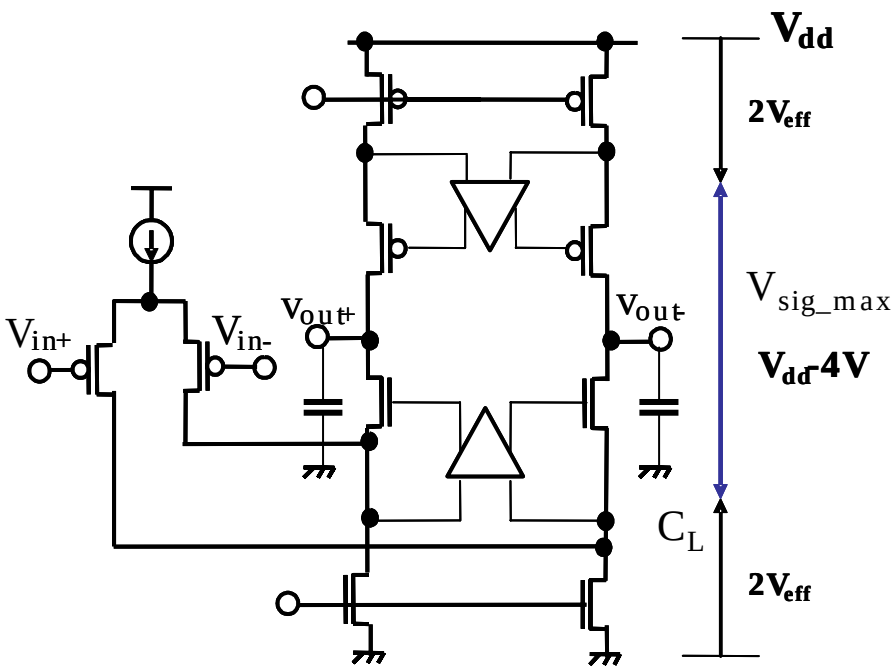
$$12b : 82dB$$

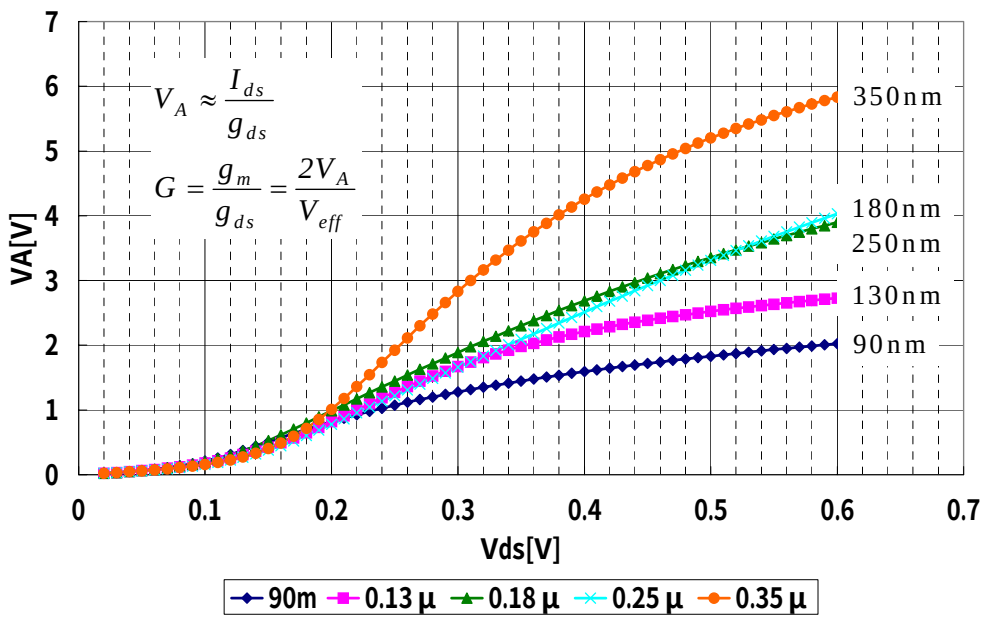
Sub-100nm CMOS

$$G_{DC} \approx \left(\frac{V_A}{V_{eff}}\right)^n \approx \left(\frac{1}{0.15}\right)^n \approx 16dB \times n$$

$$n < 5$$

$$G_{DC} < 80dB$$





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Conversion speed of pipeline ADC

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Speed of pipeline ADC is proportional to the OPamp current basically.

$$f_c \approx \frac{3GBW_{\_close}}{N} \propto \frac{I_{ds}\beta(I_{ds})}{C_L(I_{ds})}$$

$$GBW_{\_close} = \frac{g_m \cdot \beta}{2\pi C_L} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)}$$

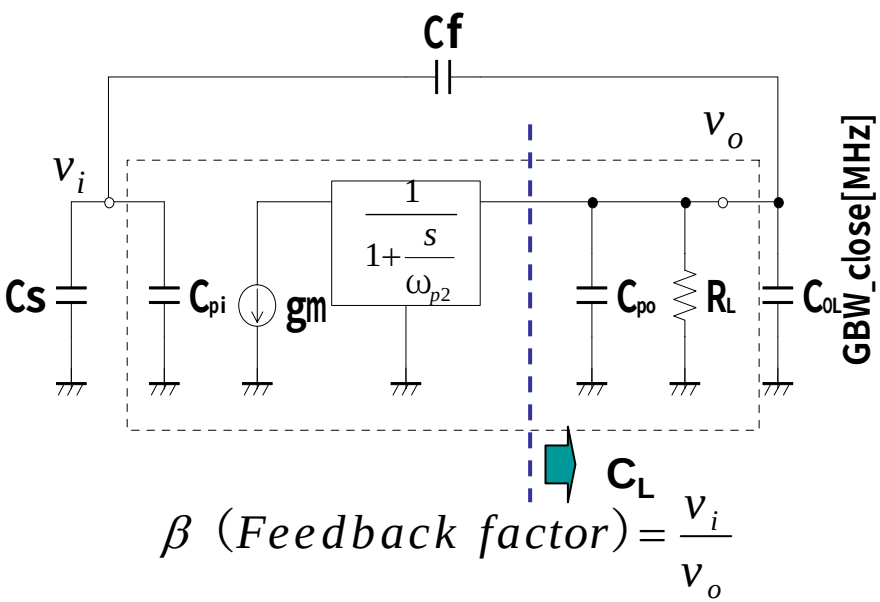
$$= \frac{I_{ds}}{\pi C_o V_{eff}} \frac{1}{\left(2+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi} I_{ds}}{C_o}\right)}$$

A. Matsuzawa, "Analog IC Technologies for Future Wireless Systems," IEICE, Tan on Electronics, Vol. E89-C, No.4, pp. 446-454, April, 2006.

$$g_m = \frac{2I_{ds}}{V_{eff}}$$

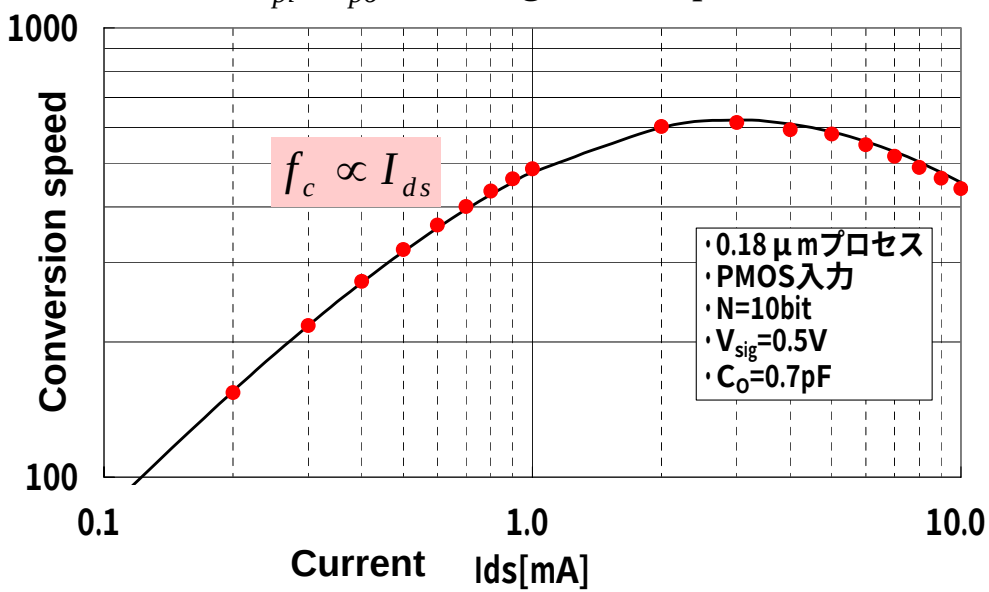
$$C_{pi} = \alpha_{pi} I_{ds}, \quad C_{po} = \alpha_{po} I_{ds}$$

Performance model



$$\beta\ (Feedback\ factor) = \frac{v_i}{v_o}$$

α_{pi}, α_{po} are design rule dependent



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Capacitances: Signal and parasitic

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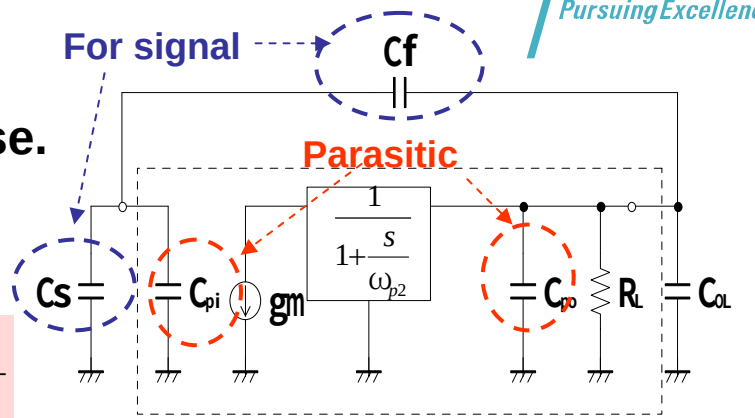
Parasitic capacitance can be reduced by technology scaling,
However, capacitance for signal will increase.

$$C_o \geq 1.66 \times 10^{-19} \left(\frac{2^N}{V_{sig}} \right)^2 \qquad V_{sig} = 2\left(V_{dd} - 4V_{eff}\right)$$

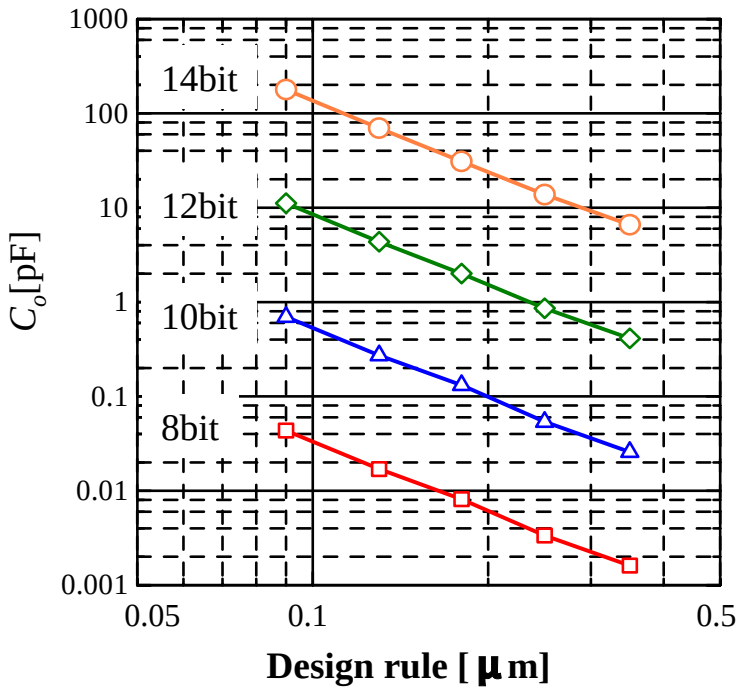
$$V_{eff} = 0.15V$$

$$C_o \propto \left(\frac{2^N}{V_{sig}} \right)^2$$

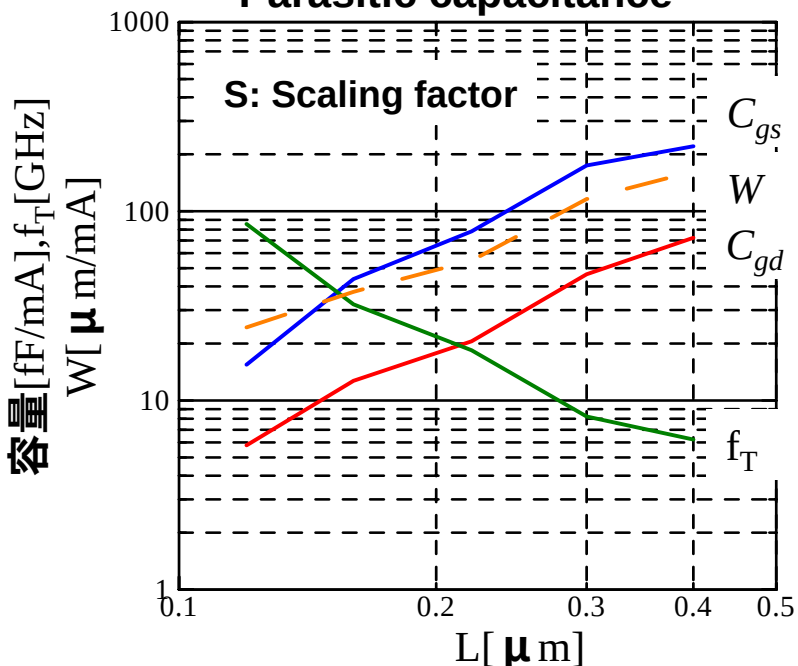
$$C_p \propto \frac{1}{S^2}$$



Required capacitance for signal



Parasitic capacitance



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Performance summary

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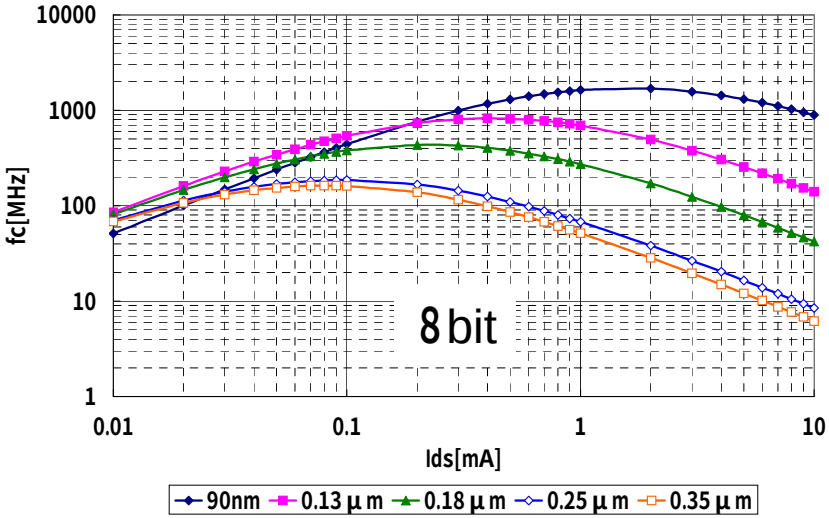
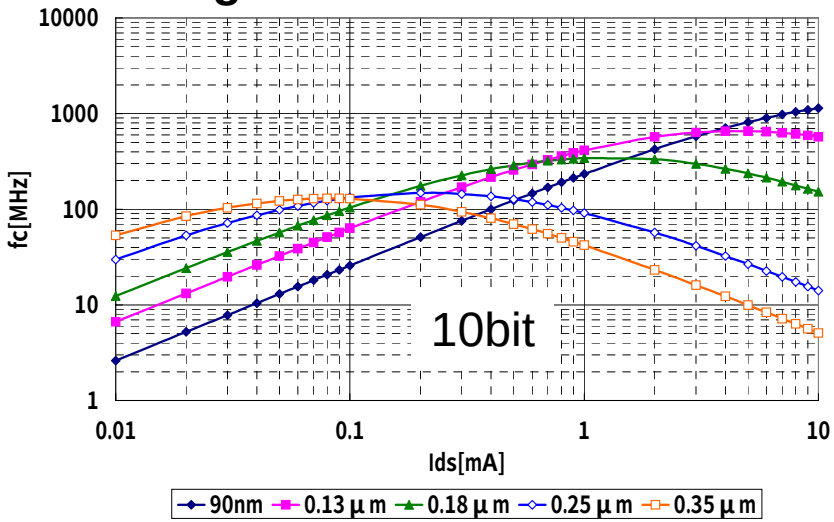
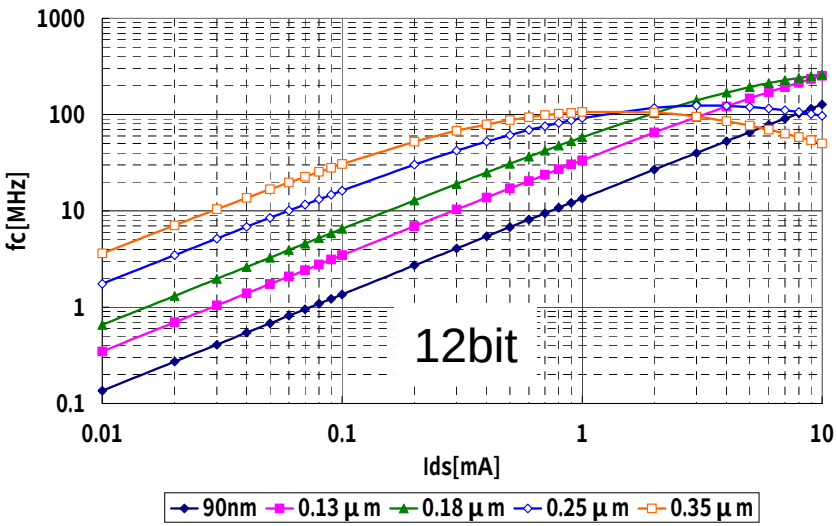
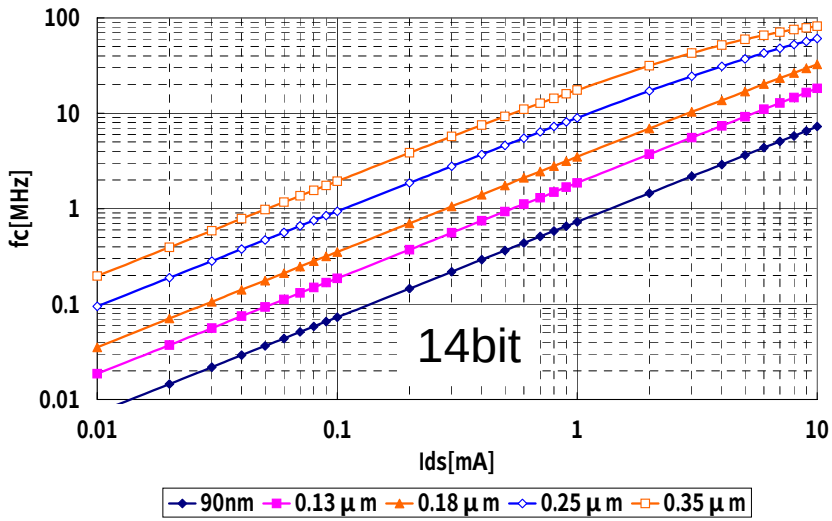
Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.









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Speed and power

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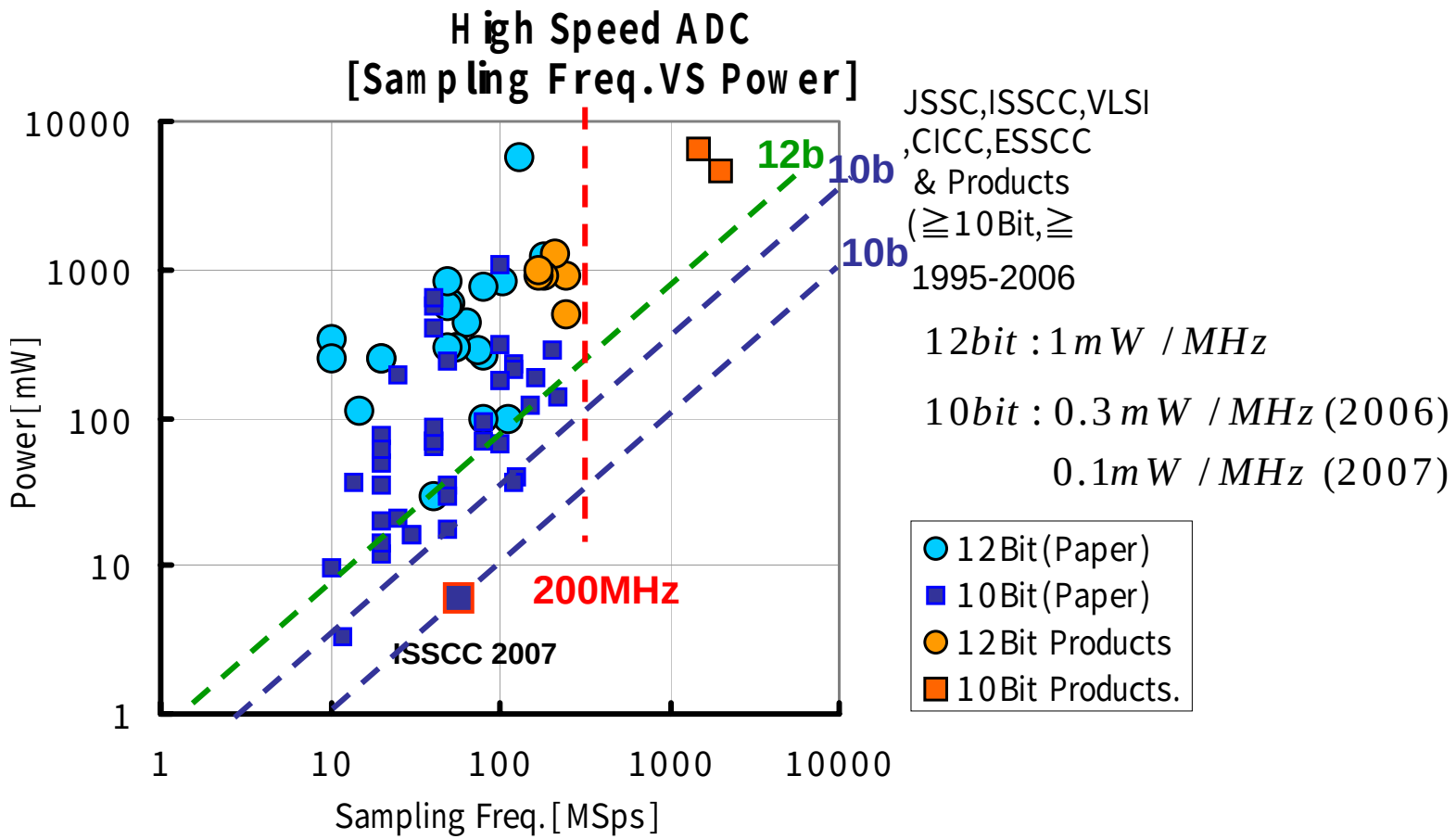
Conversion speed has saturated at 200 MHz
Lower mW/MHz is needed for low power operation.



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Revolution of SA ADCs

(Low FoM ADC architecture)

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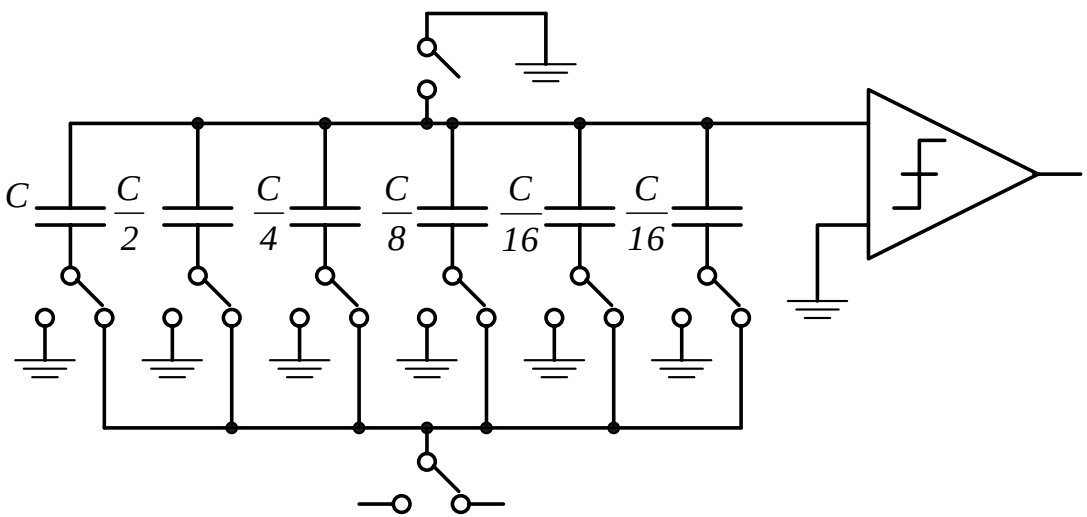
SA ADC

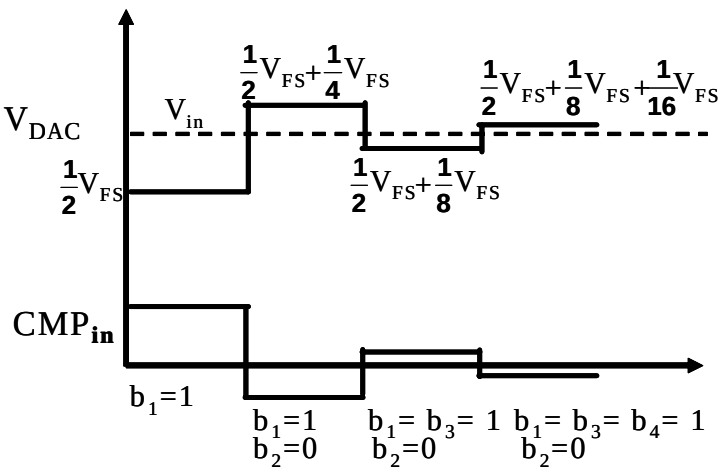
Successive Approximation ADC is free from OpAmp design issues and looks suitable for sub-100nm CMOS era.

Require only capacitors, switches, comparator, and logics.

No quiescent current → extremely low power



Binary search algorithm



Binary weighted Capacitor array

Performance overview of SA ADCs

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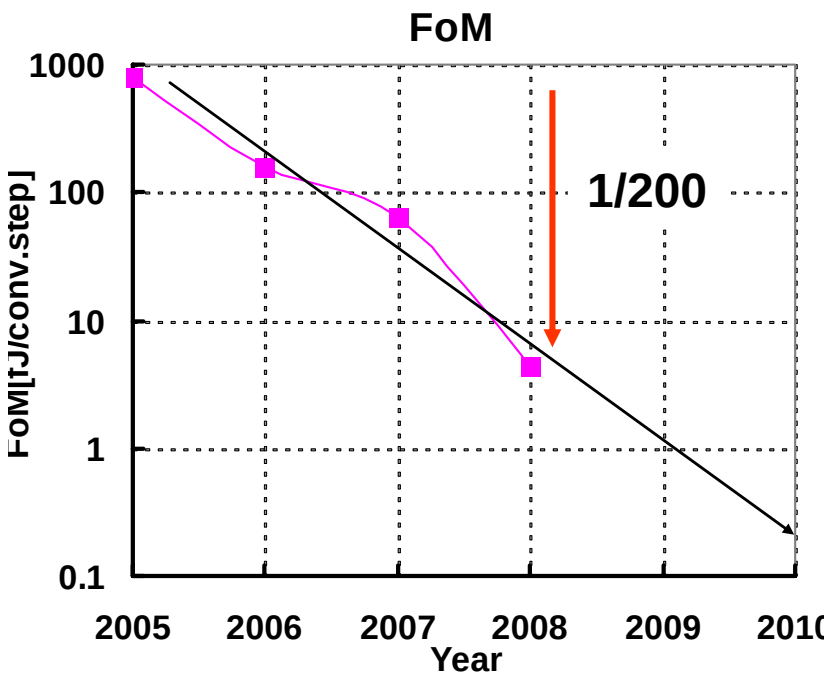
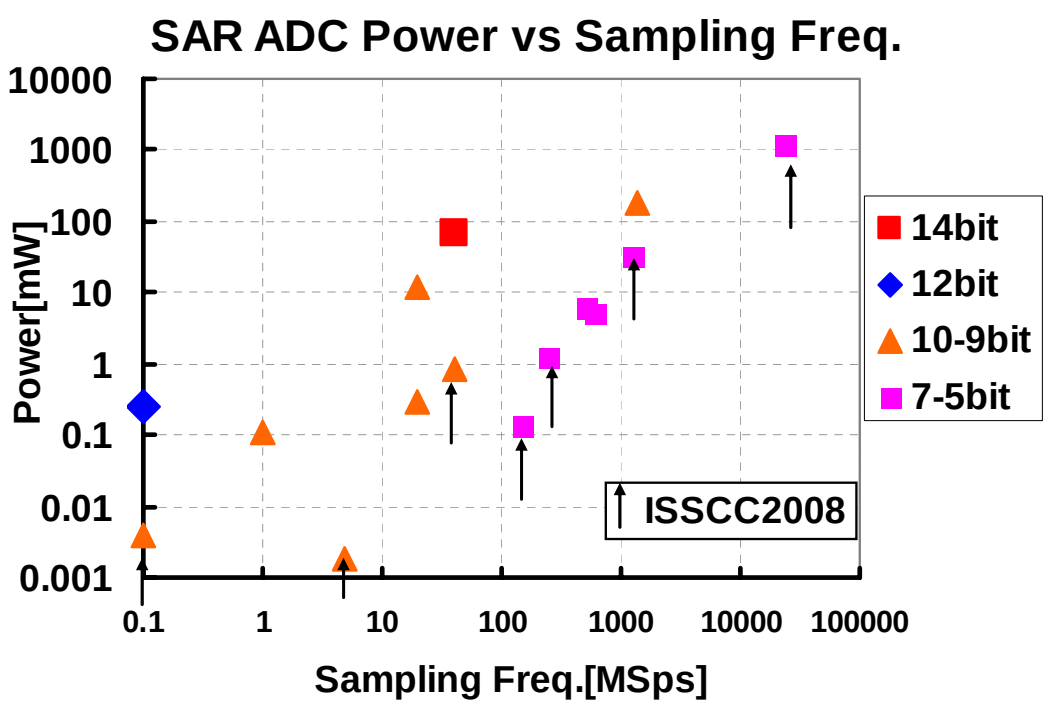
SA ADCs become dominant in every performance range.
In particular FoM has rapidly lowered.

1/200 during past three years.

Courtesy Y. Kuramochi





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SA ADC: The most simplest ADC

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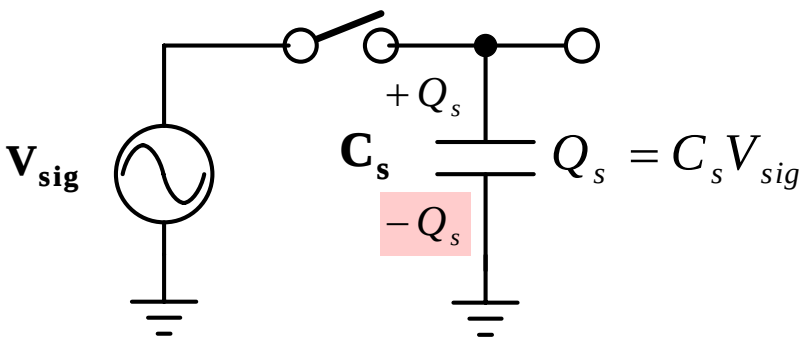
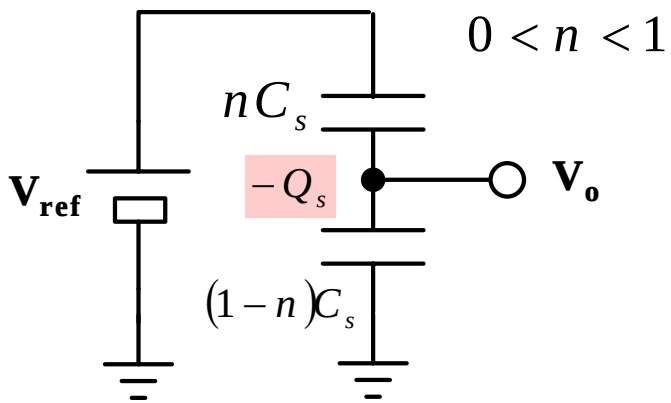
The most simplest ADC architecture:
No static current and the passives determine the SA ADC performance.
In contrast, OPamp determines the performance of pipeline ADC.

Sample and hold



Quantization
Comparing between reference voltage and signal



$$nC_s(V_o - V_{ref}) + (1-n)C_s V_o = -Q_s$$
$$\therefore nC_s V_{ref} - C_s V_o = Q_s = C_s V_{sig}$$
$$\therefore V_o = -(V_{sig} - nV_{ref})$$

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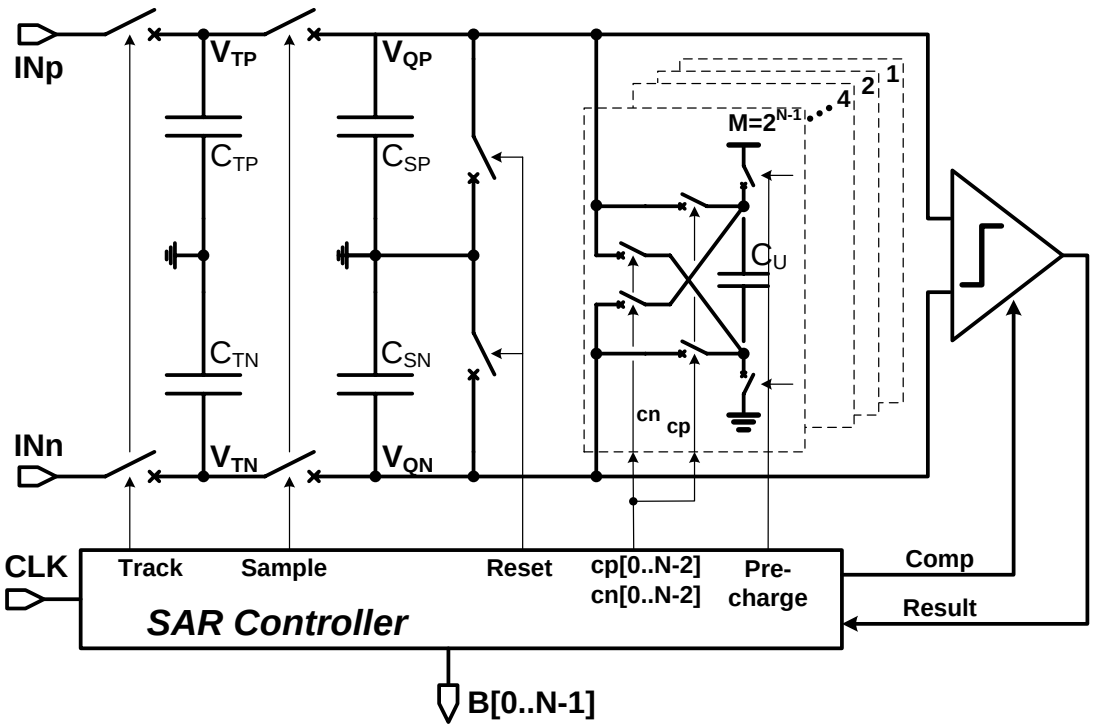
Recent SA ADC

SA ADC must be the best solution for scaled analog technology.
No OpAmp is needed.

No static power consumption.
Higher signal swing and small capacitance



$$Q_{REF} = \sum_i 2^i C_U \cdot V_{DD}$$

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

Analog operation with capacitances

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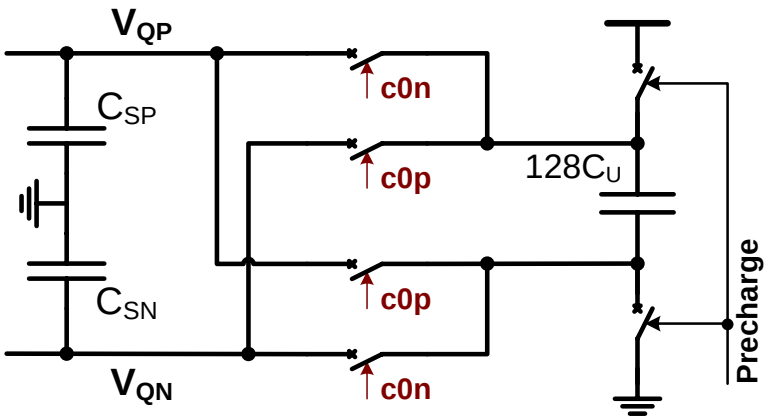
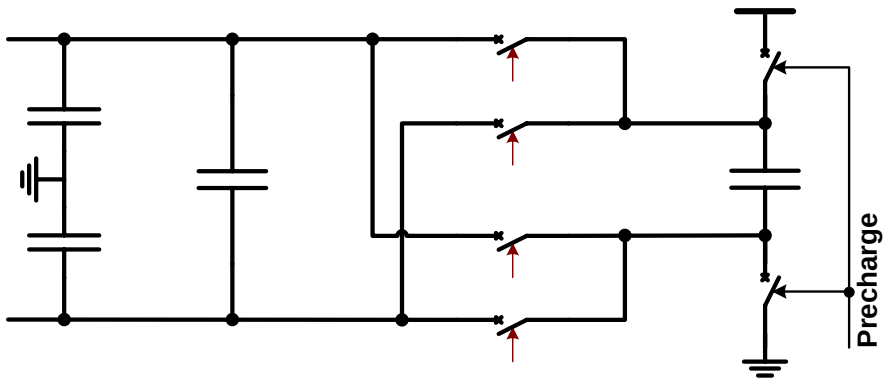
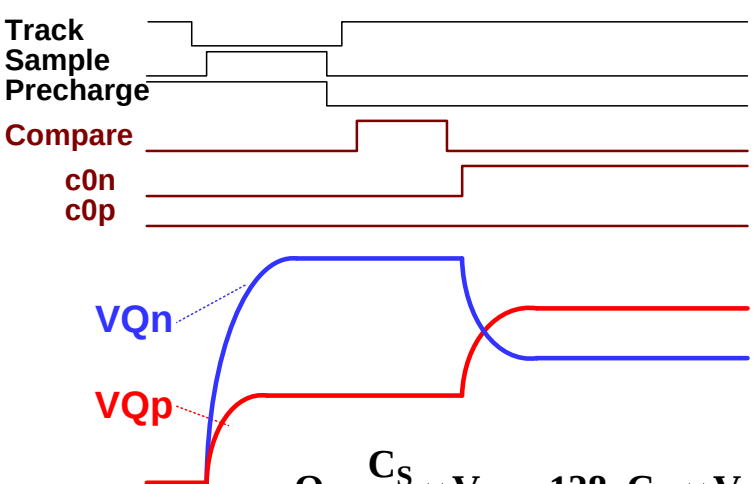
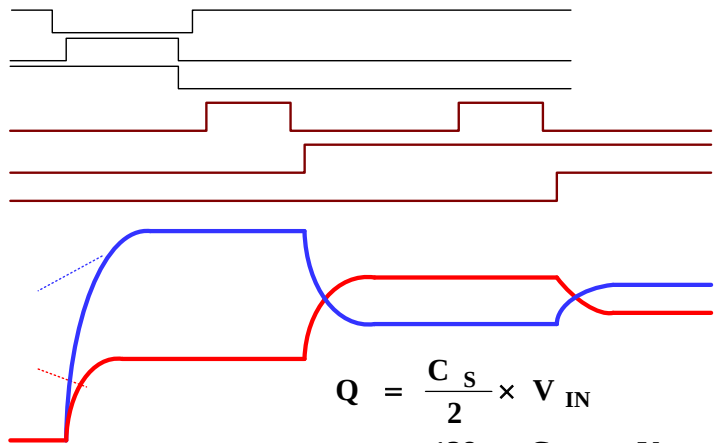
Capacitances can realize analog operation for SAR ADC.
No static current is required and higher signal swing can be used.







$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD}$$



$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD} + 64 \cdot C_U \times V_{DD} \pm \ldots$$

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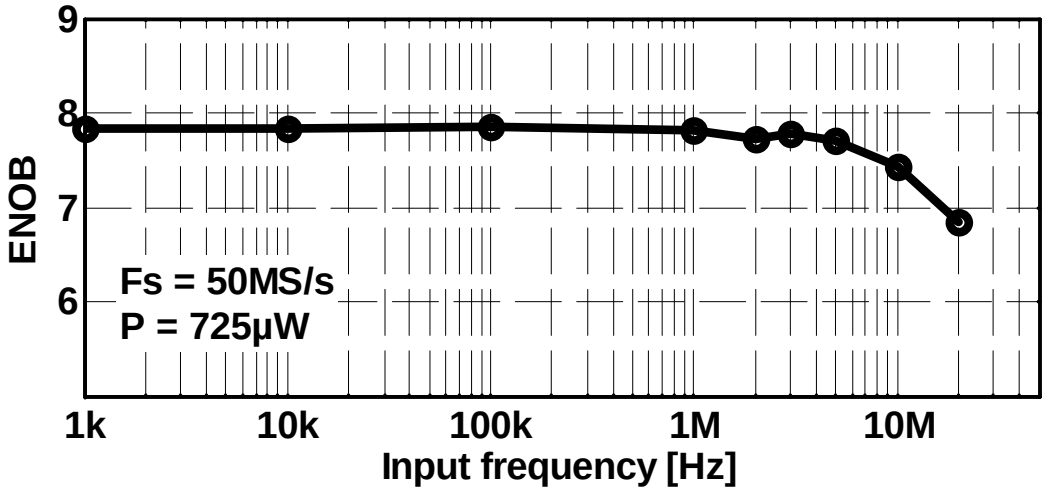
Results

Amazing small FoM=65fJ/step has been attained.



8bit, 0.3mW at 20MHz

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

ISSCC06 Paper #	Arch.	Fs [MS/s]	ENOB	P [mW]	FoM [fJ]	FoM includes		
						Ref.	Clock	Dec.
3.1	CTΔΣ	40	12	50	300	-	Yes	Yes
3.4	ΔΣ	4.4	12.6	13.8	500	-	No	No
12.1	PL	100	9.4	39	570	-	-	-
12.3	Subr.	50	10.4	30	440	-	-	-
12.4	PL-CBSC	7.9	8.7	2.5	760	-	-	-
12.5	SAR	0.1	10.5	0.025	170	No	No	-
12.7	PL	50	9.2	15	510	-	-	-
31.1	Flash	1250	3.7	2.5	160	-	-	-
31.5	SAR	300	5.3	2.65	220	No	Yes	-
This work	**CS-SAR**	**20**	**7.8**	**0.29**	**65**	**Yes**	**Yes**	-

World lowest FoM ADC

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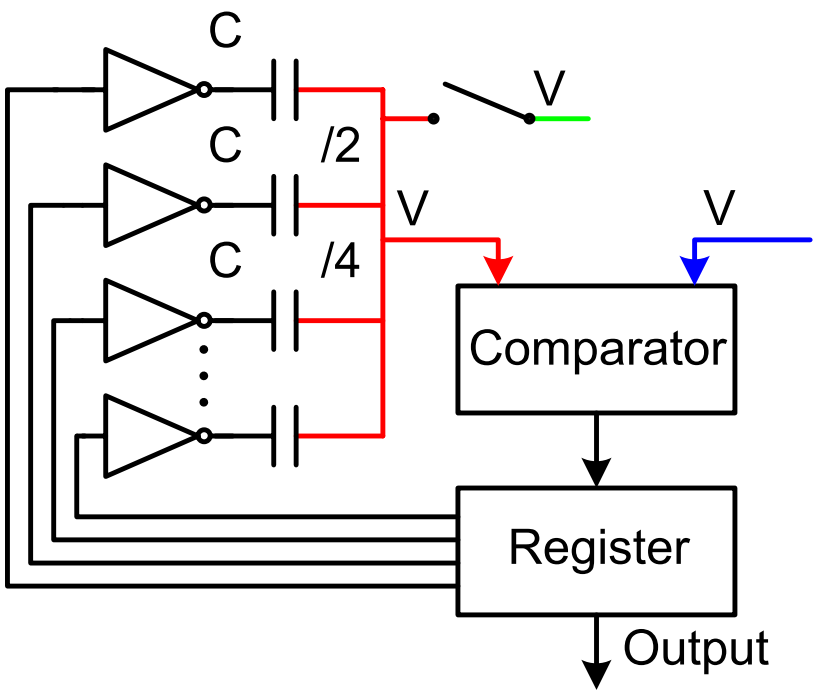
Extremely low FoM of 4.4fJ/conv-step. SA ADC has been realized

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, “A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

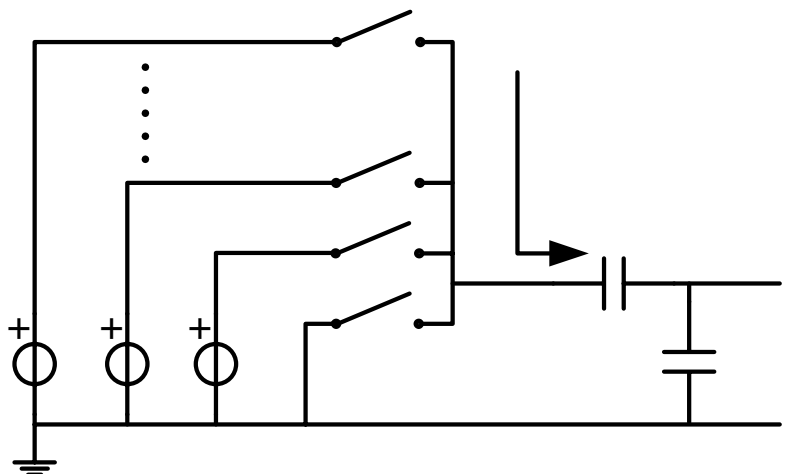
Multi-step charging can reduce energy more

$$E_{diss} = n \cdot \frac{1}{2} \cdot C_{eq} \cdot \left(\frac{V_b}{n} \right)^2 = \frac{1}{n \cdot 2} \cdot C_{eq} \cdot V_b^2$$

Simple SA architecture



Multi-step charging (Adiabatic charging)



Comparison with state-of-the-art ADCs

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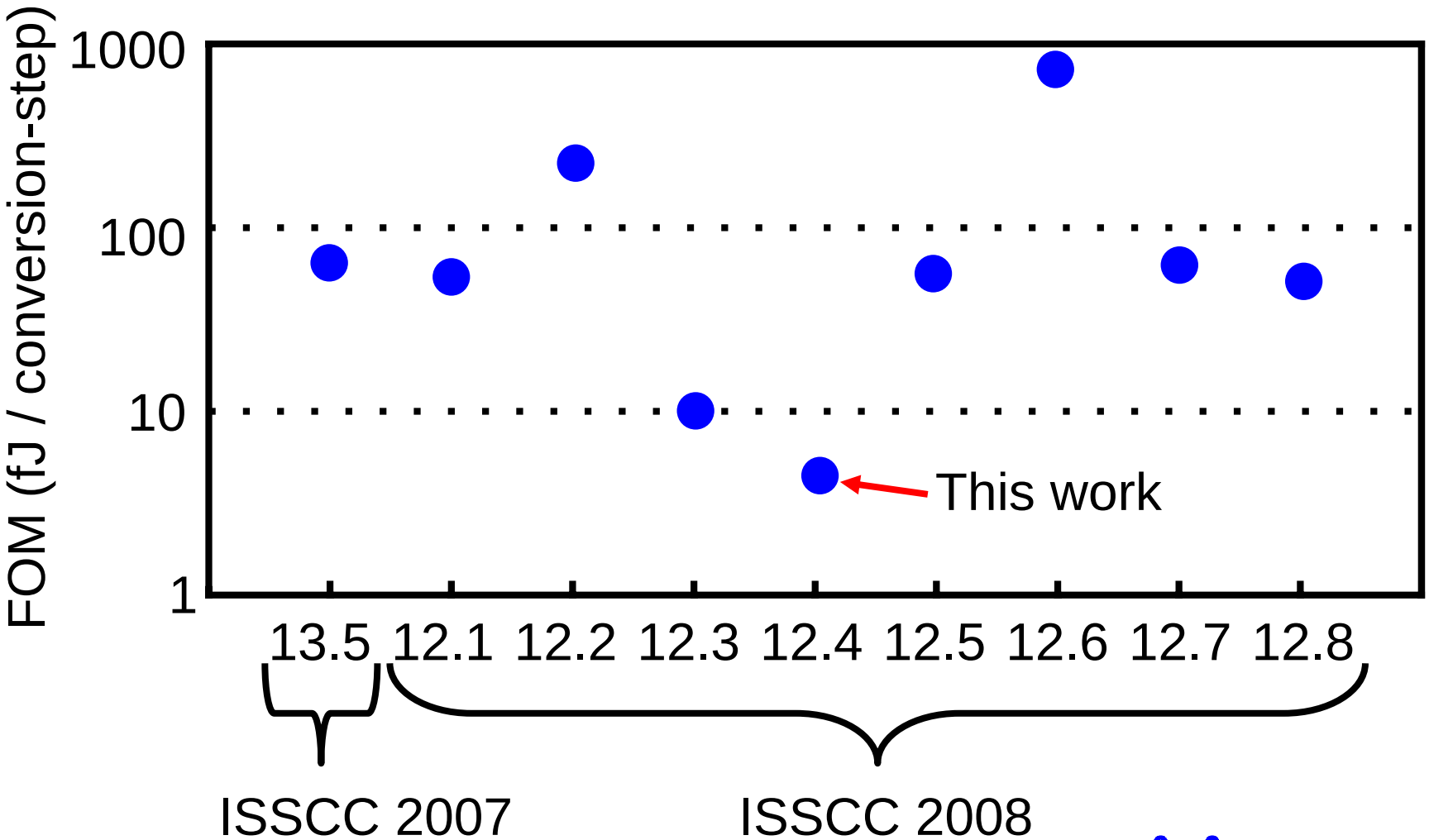
Low FoM <100fJ/conv.-step ADCs become major.



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Reduction of area of SA ADC

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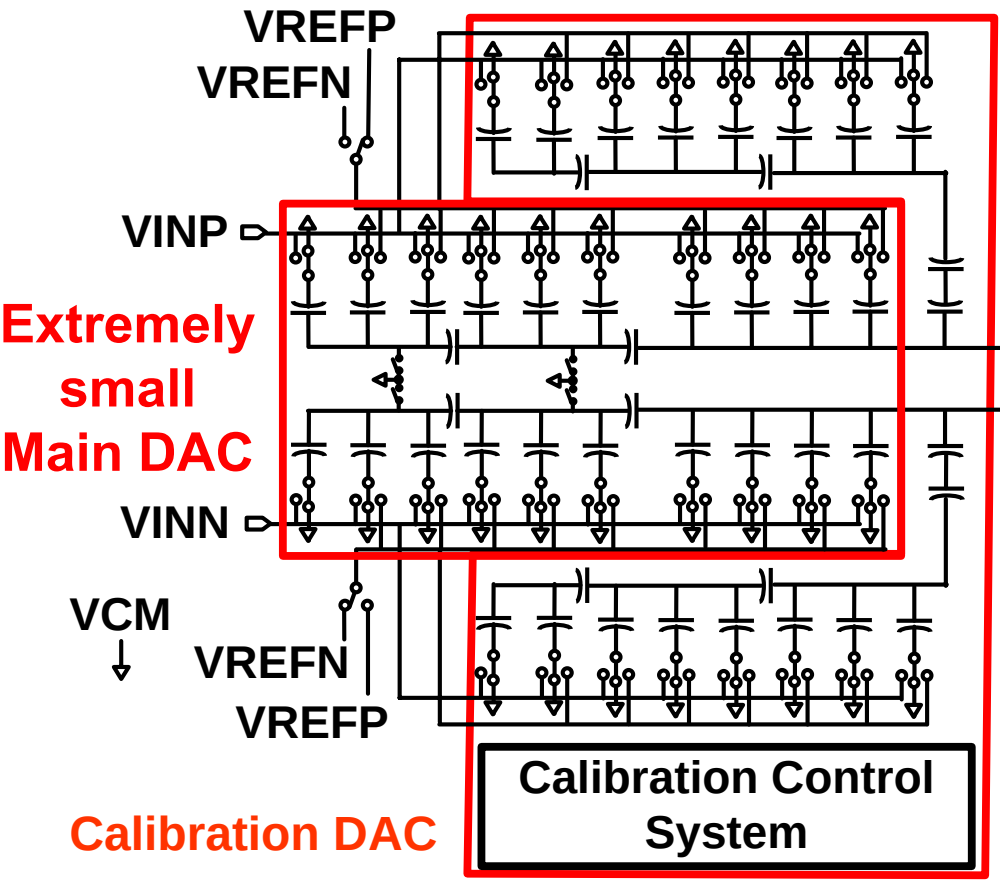
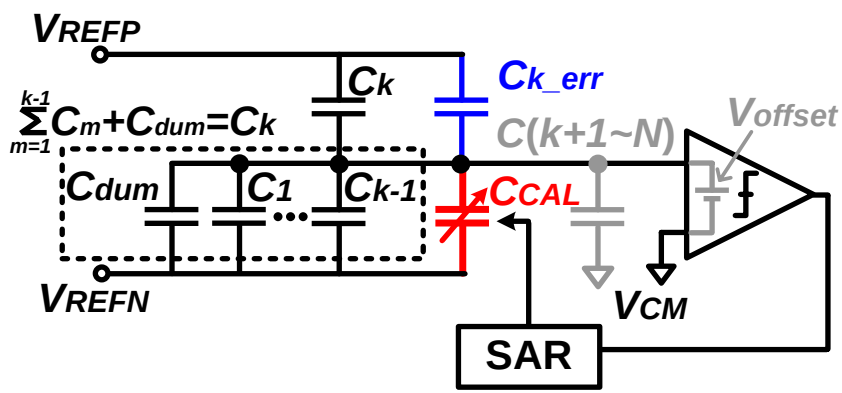
One issue of current SAR is not small occupied area.
This is due to large capacitance ratio; $C_{MSB}/C_{LSB}=2^N$
Serial capacitors can reduce this ratio,
however parasitic capacitors degrade accuracy. We solved it by calibration.



Yasuhide Kuramochi, Akira Matsuzawa, and Masayuki Kawabata
"A 0.05-mm2 110-uW 10-b Self-Calibrating Successive Approximation ADC Core in 0.18-um CMOS"
A-SSCC, 8-1, pp 224-227, Korea, Jeju, Nov, 2007.



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Effect of digital calibration

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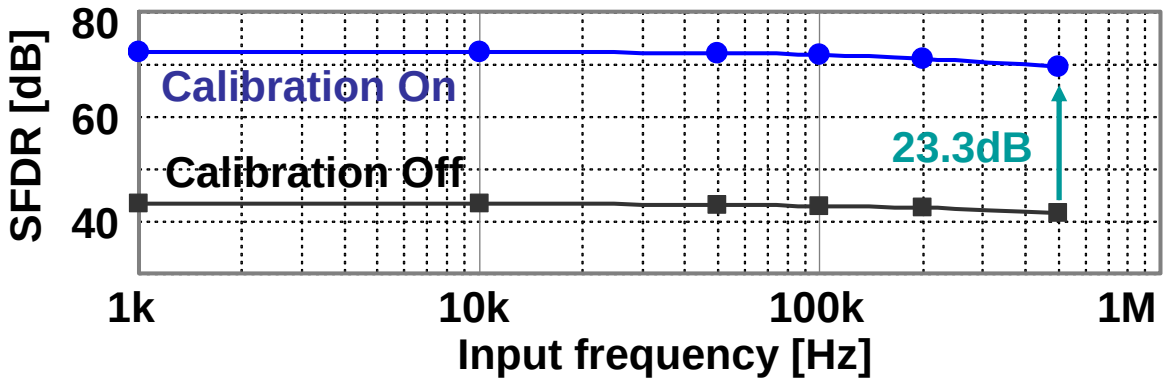
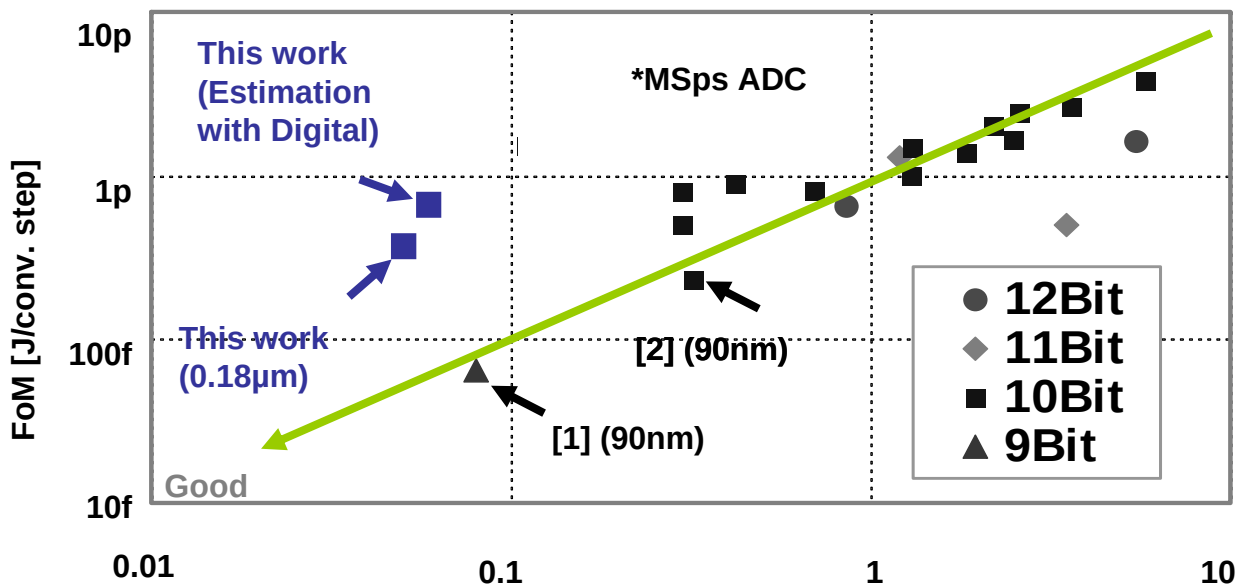
We can realize 10b ADC with high SFDR of 72dB ADC in world smallest chip size, by using digital calibration technique.



[1] J. Craninckx, et. al. *ISSCC 2007*
[2] Y. Jeon, et. al., *ISSCC 2007*



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Fight back of pipeline ADCs

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Optimization of OpAmp in Pipelined ADC

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90nm CMOS, near sub-threshold operation, and SC level-shift have realized 10bit 80MHz ADC with 0.8V operation and small power of 6.5mW

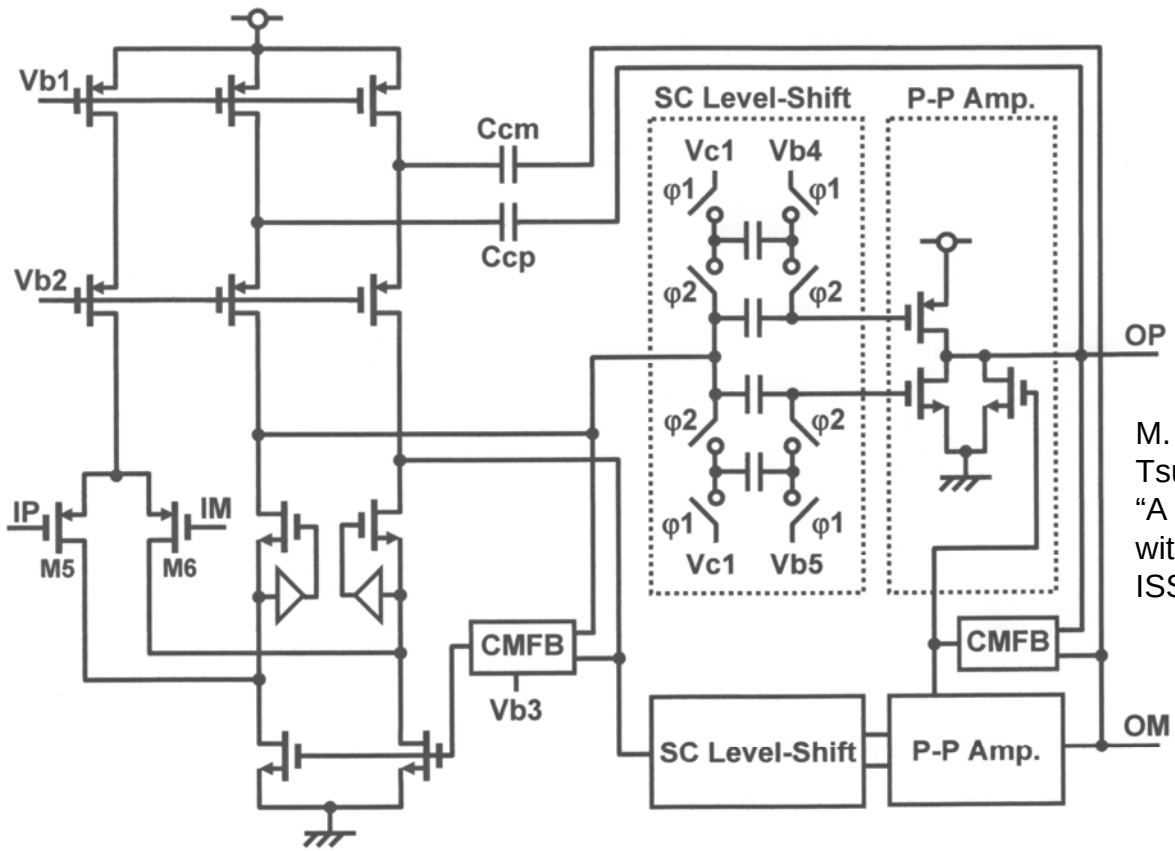

Figure 25.1.2: Schematic of two-stage amplifier.

M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto
"A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing," ISSCC, Dig. Tech. paper, pp. 452-453, 2007.

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Results

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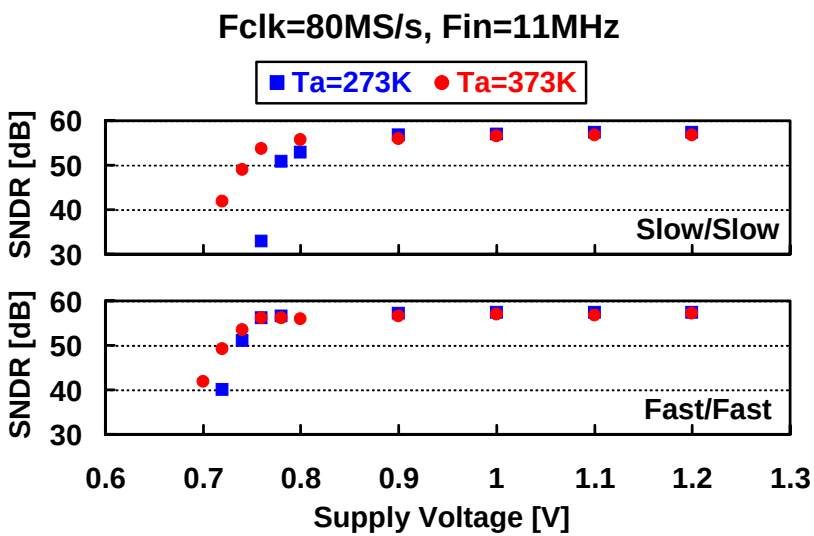
Excellent FoM has been attained in spite of pipeline ADC.

FoM=200fJ/step 0.08mW/MHz

Technology	1P10M 90nm CMOS with MIM Capacitors	
Resolution	10bit	
Conversion Rate	80MS/s	
Active Area	1.18mm x 0.54mm	
Input Range	1.2Vp-p Differential	
Supply Voltage	0.8V	1.2V
SNDR	55.0dB @2MHz 51.4dB @41MHz	56.9dB @2MHz 55.6dB @41MHz
Total Power Consumption	6.5mW	13.3mW
INL	< 1.0LSB	< 0.5LSB
DNL	< 0.8LSB	< 0.4LSB



Optimization of V_{eff}

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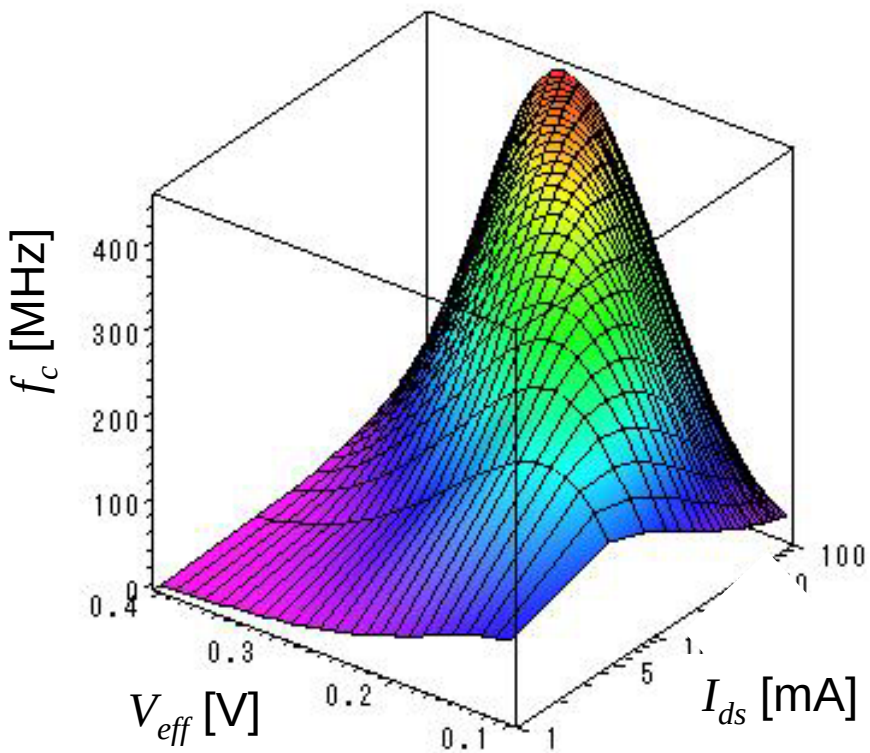
Optimum V_{eff} is a function of resolution, current, and design rule.
The lower V_{eff} is recommended for scaled CMOS technology.

M. Miyahara, A. Matsuzawa, "A Performance Model for the Design of Pipelined ADCs with Consideration of Overdrive Voltage and Slewing", IEICE TRANS. ELECTRON, vol. E91-A, No.2, pp.469-475, Feb. 2008.

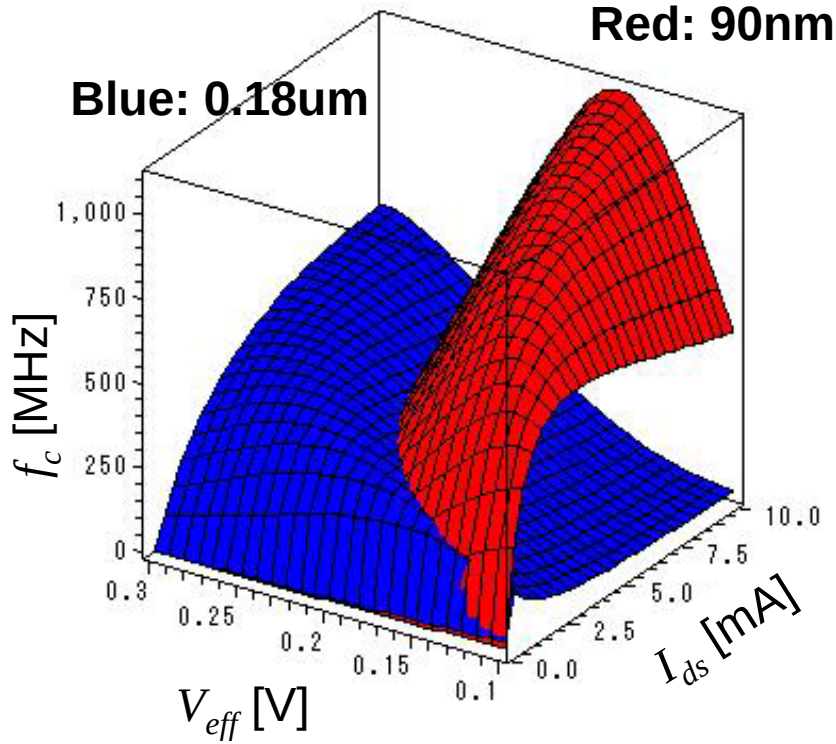
12 bit, 0.18um CMOS



10 bit

Red: 90nm

Blue: 0.18um



Process improvement of MOS transistor

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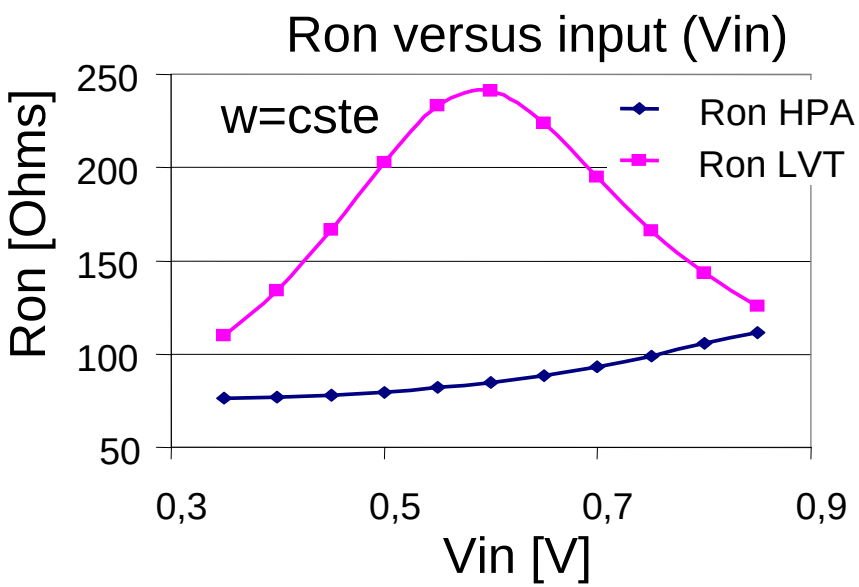
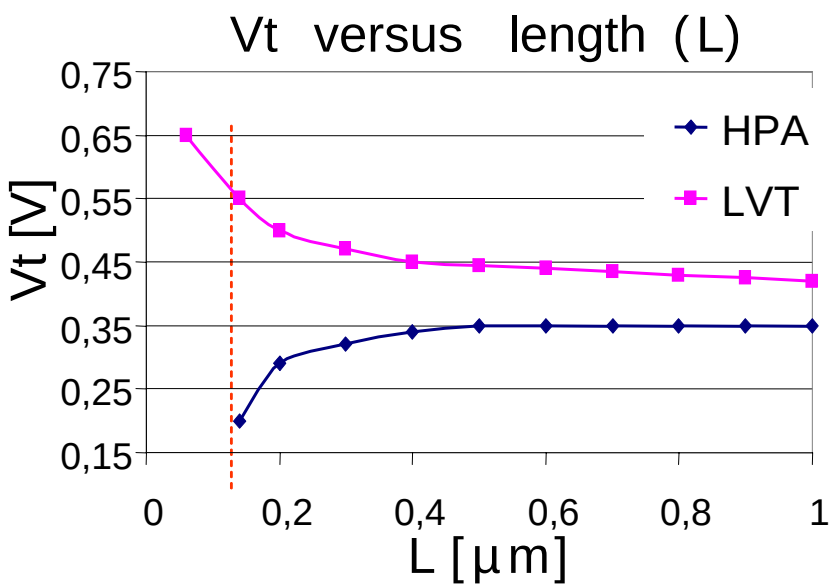
No pocket transistor with low threshold voltage transistor offers low on-resistance for switches

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet, "A 1.2V 4.5mW 10b, 100MS/s Pipeline ADC in a 65nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.250-251, Feb. 2008.

Lmin (HPA)=0.14um





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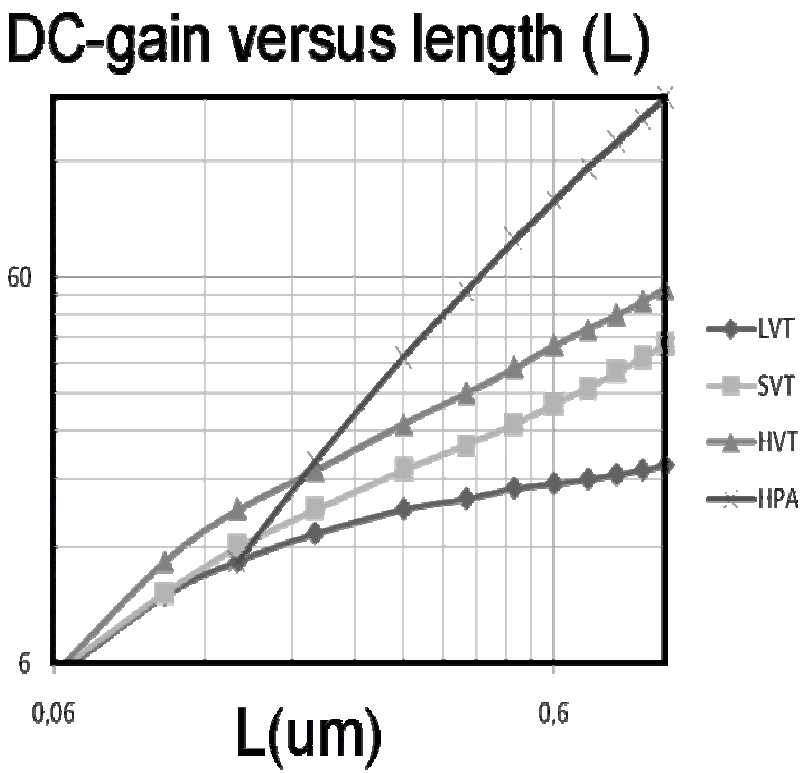
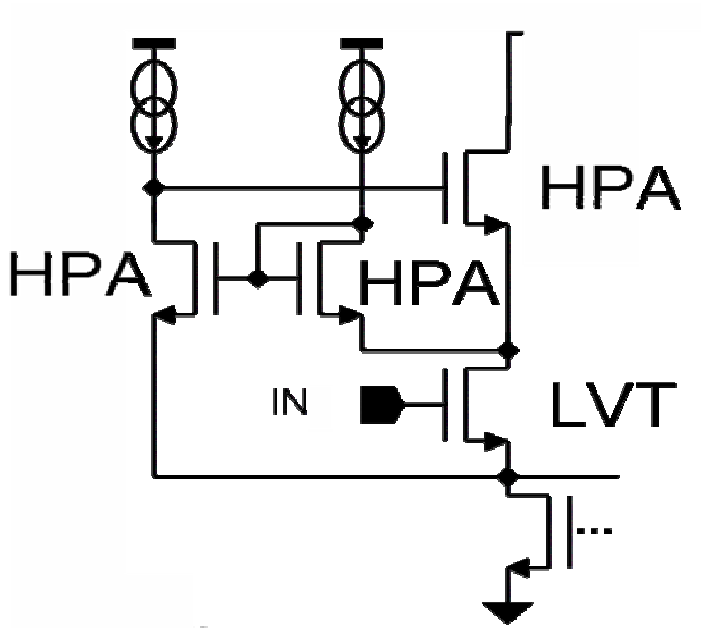
Optimization of MOS transistor

TOKYO TECH Pursuing Excellence

No-pocket MOS transistor can increase output resistance and results in increasing the DC gain.





Summary of performance

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This pipeline ADC has attained excellent low FoM compatible with SA ADC

Resolution	**10 bit**
Sampling speed	**100MS/s**
Input range	**1.0Vppd**
Power Consumption	**4.5mW**
SNDR	**59dB**
DNL	**+/-0.1 LSB**
INL	**+/-0.2 LSB**
Active area	**0.07mm^2**
Technology	**ST CMOS 65nm**

FoM= 62fJ/conv.-step

Tech (nm)	VDD (V)	Fs (MHz)	Power (mW)	SNDR (dB)	FOM (pj/step)	References
130	1.2	120	90	57.1	1.25	B.Hemes ISSCC-2004
90	1.2	12	3.3	52.6	0.76	R.Wang ISSCC-2005
90	1.2	100	35	56.9	0.6	G.Geelen ISSCC-2006
90	1.0	100	33	55.3	0.69	K.Honda JSSCC-2007
90	0.8	80	6.5	55	0.17	M.Yoshioka ISSCC-2007
65	1.2	100	4.5	59	0.062	This work

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Our original work

What determines FoM

OpAmp based design vs. comparator based design

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OpAmp based vs. comparator based

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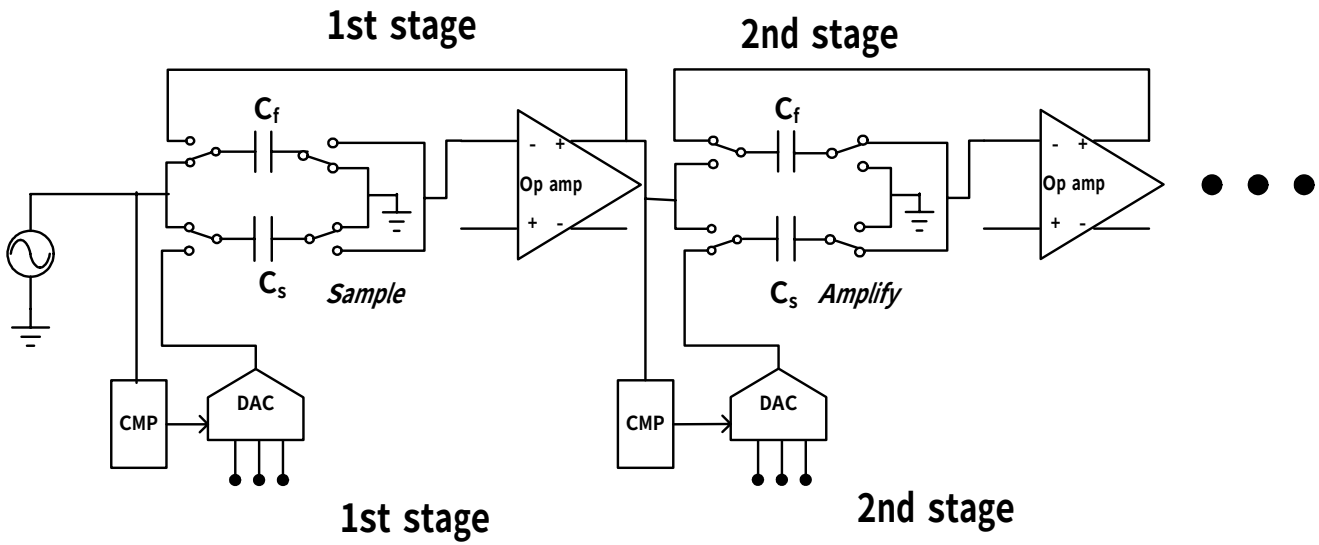
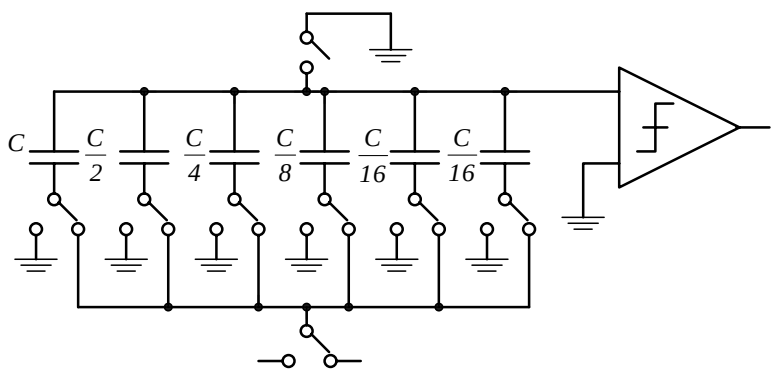
Pipelined ADC

Opamp base



SA ADC

Comparator base



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Noise of OpAmp

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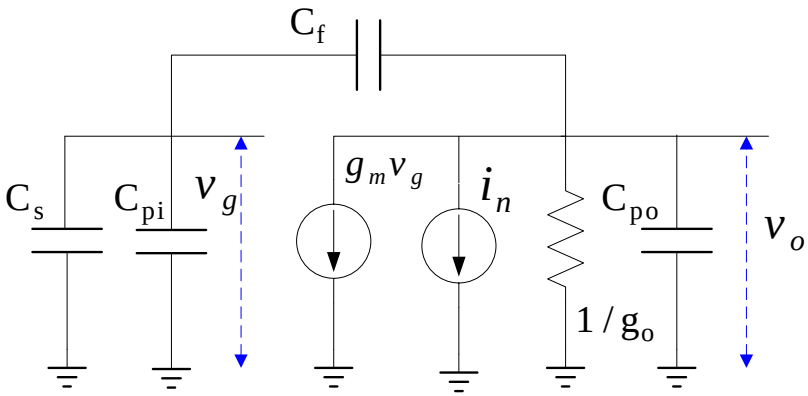
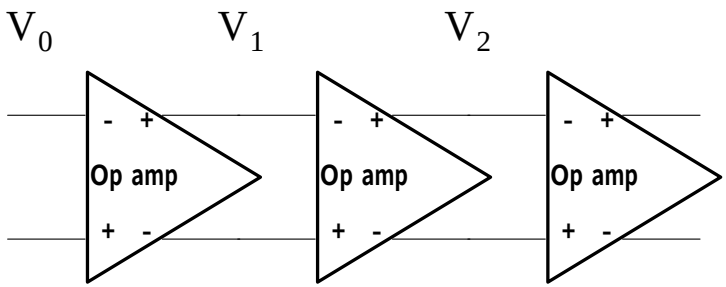
Amplification phase





$$v_{no}^2 = \int_0^\infty \frac{i_n^2}{(g_m\beta)^2 + (\omega C_L)^2} df = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f}$$

$$v_{no}^2 = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f} \qquad C_f = C_s = C_o$$

V_0: $v_{no}^2 \approx \frac{kT}{C}$

V_1: $v_{n1}^2 = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C}$

V_2: $v_{n2}^2 = 2\, v_{n1}^2$

$\beta \rightarrow \beta$

$C_L \rightarrow \frac{C_L}{2}$

$v_{ni}^2 = 2 \cdot v_{ni-1}^2$

n=2: Cascode
n=3: Folded Cascode

$$v_{nt}^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1}\left(\frac{1}{2^2}\right)^i \cdot v_i^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1}\frac{2^i}{2^{2i}} \cdot v_1^2 \approx 2\frac{kT}{C_o} + \frac{\gamma n kT}{\beta C_L}$$

FoM calculation

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We can estimate FoM for pipeline ADC.

Noise → Capacitance, Freq → Current

$$v_{nt}^2 = 2\frac{kT}{C_0} + \frac{\gamma n kT}{\beta C_L} \approx \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_0}$$

$$V_{qn}^2 = \frac{1}{3}\left(\frac{q}{2}\right)^2 = \frac{1}{3}\left(\frac{V_{dd} - 2V_{eff}}{2^N}\right)^2 \quad if \quad V_{nt}^2 = V_{qn}^2 \quad \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_o} < V_{qn}^2$$

$$C_0 > \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{V_{qn}^2}$$

$$f_{close} > \frac{Nf_c}{3} \quad \therefore \frac{g_m \beta}{2\pi C_L} > \frac{Nf_c}{3} \therefore g_m > Nf_c \frac{2\pi}{3\beta} C_o \quad g_m \approx \frac{2I_{ds}}{V_{eff}}, \quad I_{ds} > Nf_c \frac{2\pi}{3\beta}\frac{V_{eff}}{2} C_o$$

$$P_d \approx 2.5 \times (2 \times 2 \times I_{ds} \times V_{dd}) = 10 I_{ds} V_{dd}$$

$$FoM = \frac{P_d}{f_c \times 2^{N-0.5}}$$

Estimated FoM for pipeline ADCs

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We are reaching the theoretical limit of FoM

Measured FoM=62fJ/conv., Estimate FoM =24fJ/conv. For 10b ADC

$V_{dd} = 1.0(V)$

$V_{eff} = 0.15(V)$

$kT = 4.1 \times 10^{-21}$

$\gamma = 2$

$n = 2$

$\beta = \frac{1}{3}$

$f_c = 100MHz$

Recent ADC

$V_{dd} = 1.2(V)$

$V_{pp} = 1.0V$

$f_c = 100MHz$

$C_o = 0.4pF$

$P_d = 4.5mW$

$SNDR = 59dB$

$FoM = 62fJ$

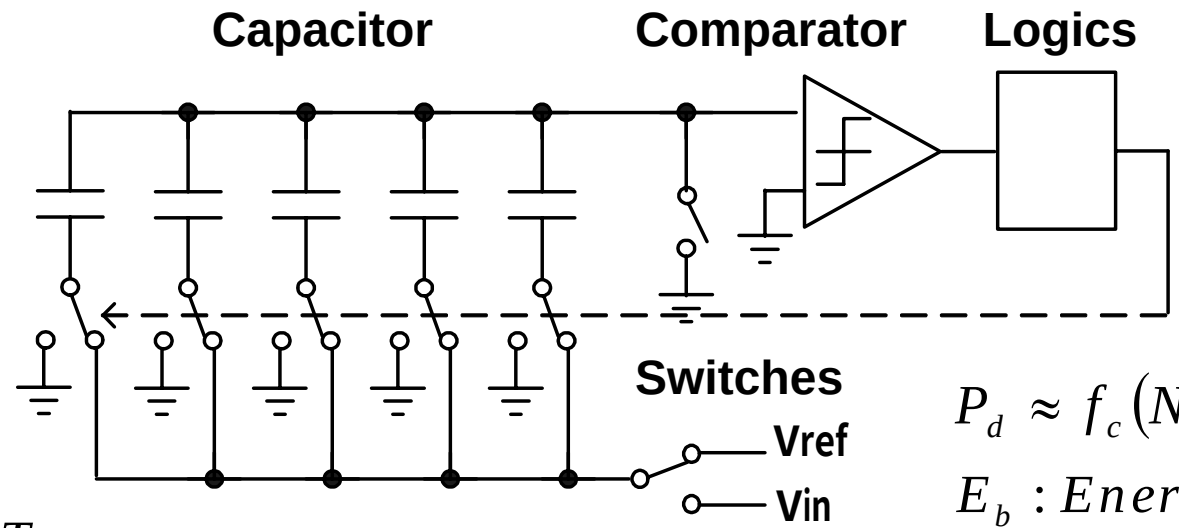
Analog portion only

Resolution	10	12	14
C_o(pF)	0.37	6.0	95
I_{dd}(mA)	1.75	33.6	628
P_d (mW)	1.75	33.6	628
FoM(fJ)	24	116	542

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet, "A 1.2V 4.5mW 10b, 100MS/s Pipeline ADC in a 65nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.250-251, Feb. 2008.

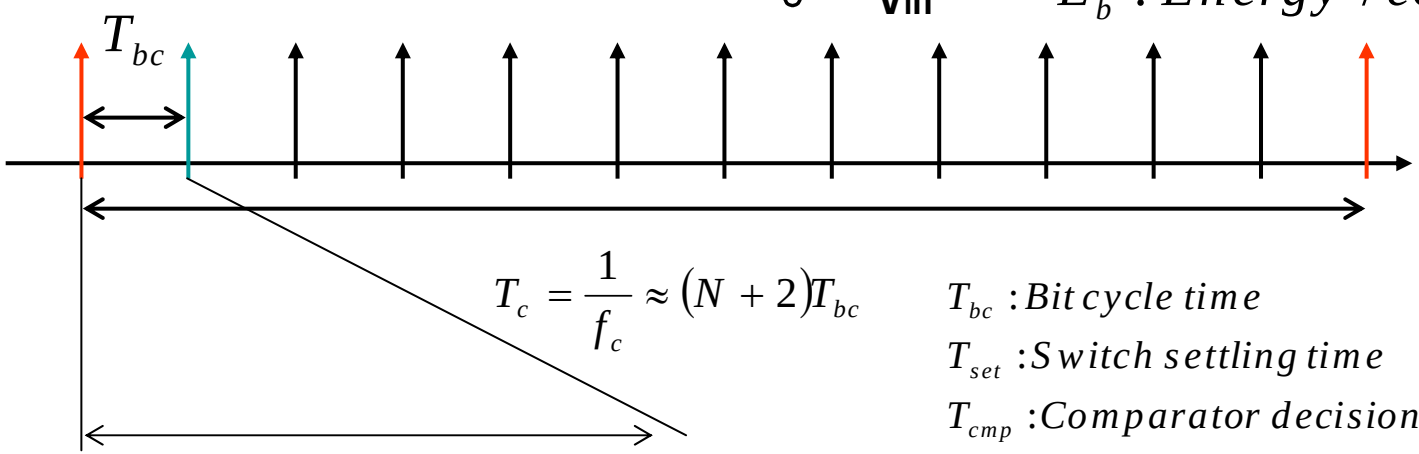
SA ADC

SA ADC needs high speed switches, comparators, and logics.



$$P_d \approx f_c (N+2) E_b$$

$$E_b : Energy / conv$$



$$T_c = \frac{1}{f_c} \approx (N+2) T_{bc}$$

$$T_{bc} = T_{set} + T_{cmp} + T_{dig}$$

T_{bc} : Bit cycle time

T_{set} : Switch settling time

T_{cmp} : Comparator decision time

T_{dig} : Logic delay time

Progress of CMOS Comparator

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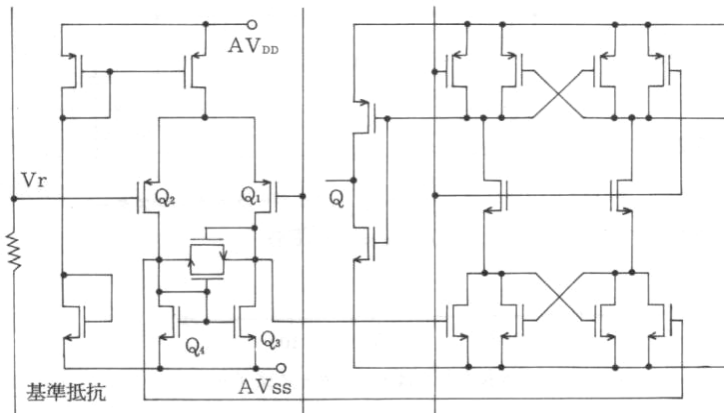
Small size MOS can be used for small mismatch circuits owing to analog compensation, however static current flows.



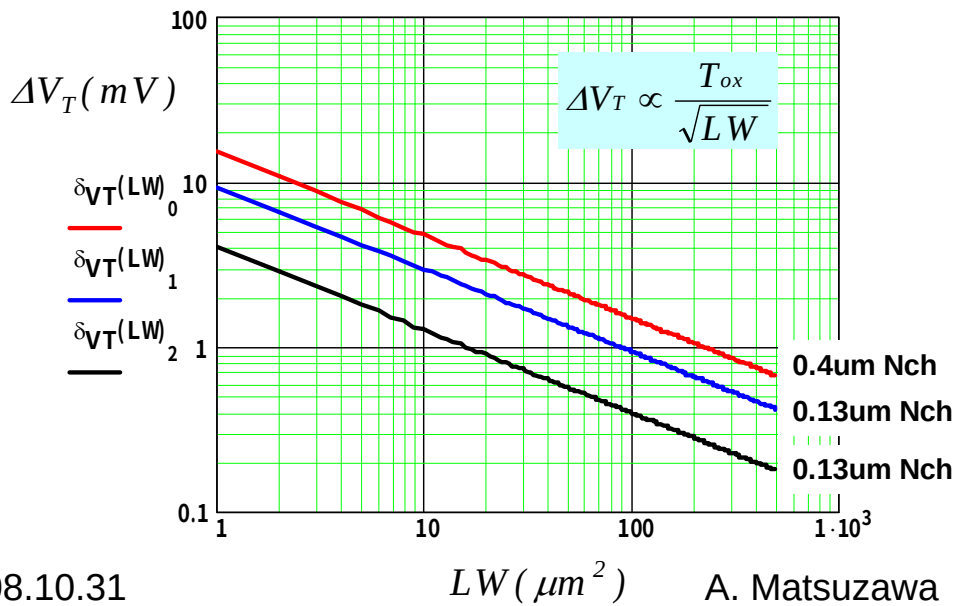
Trade off

Small mismatch ⟺ **Small area, Low power, High speed**

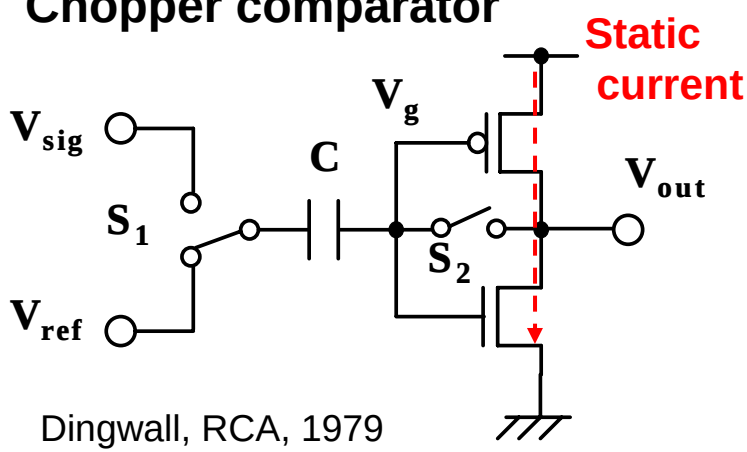
Chopper comparator solved this problem

Yukawa, et al., JSC, 1986.

Mismatch vs. gate size



Chopper comparator



Dingwall, RCA, 1979

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Comparators

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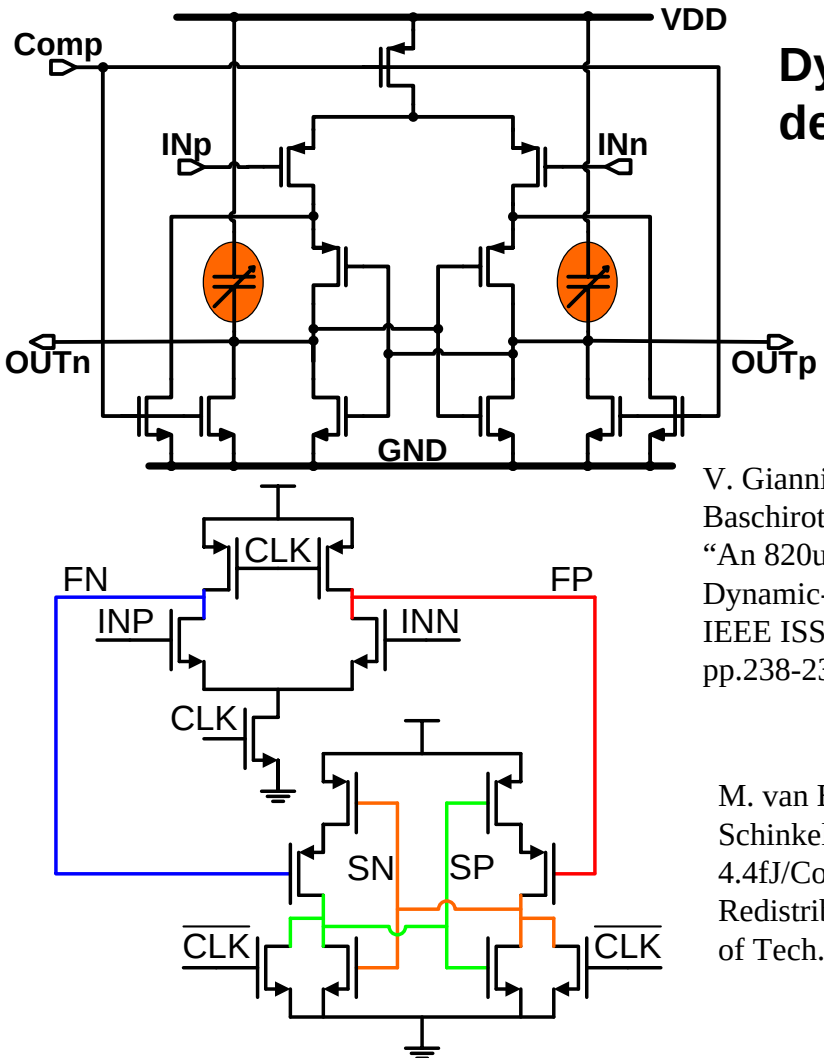
Dynamic comparators are widely used for not only SA ADCs but also Flash ADCs

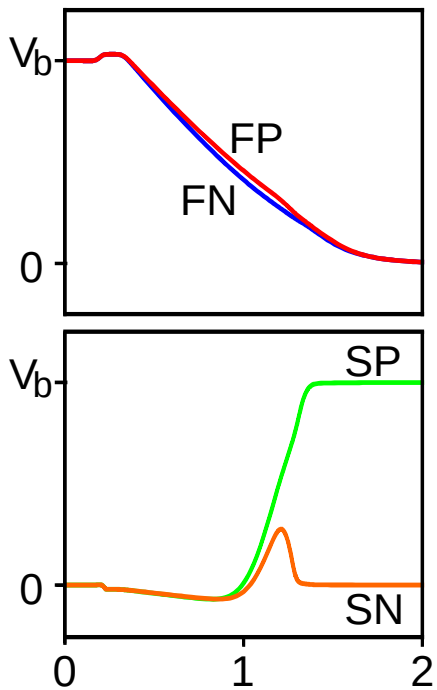


Dynamic comparators use the fast voltage fall depended on input voltage difference

V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Fast voltage fall



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Issue of comparator for SA ADCs

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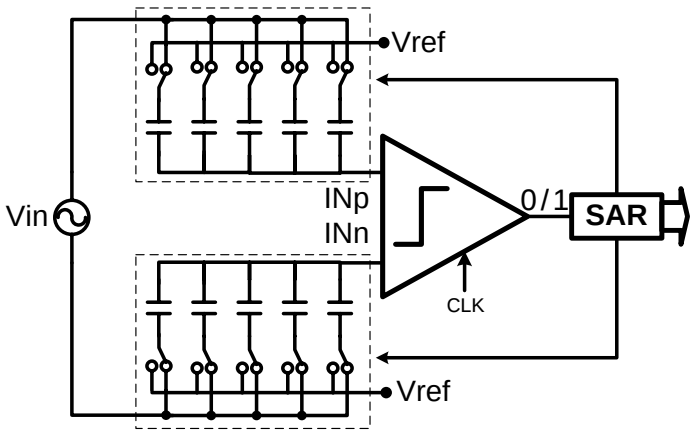
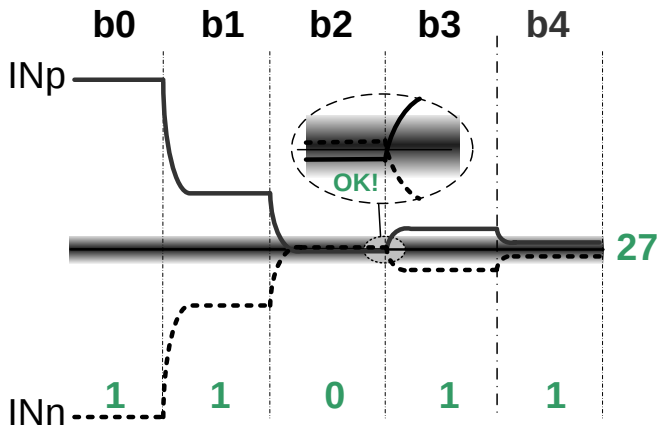
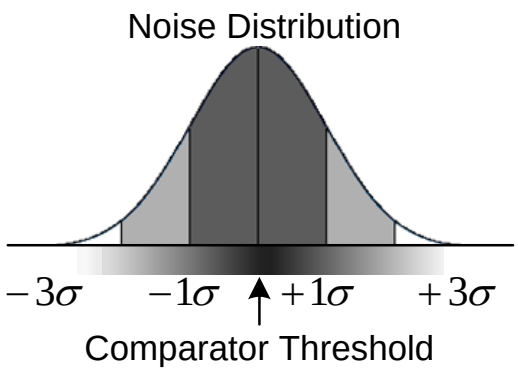
A comparator has noise and this results in conversion error.

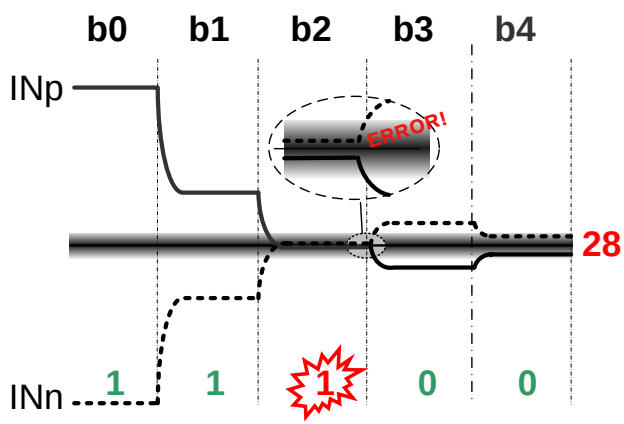
V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

5b Charge Redistribution (CR) SAR ADC









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Comparator noise and ENOB

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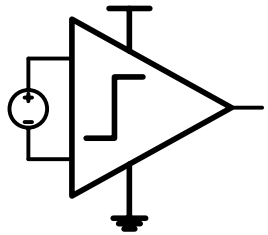
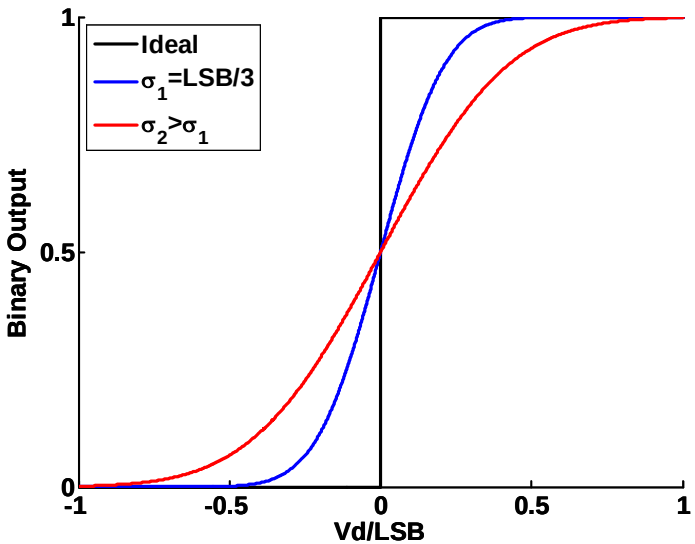
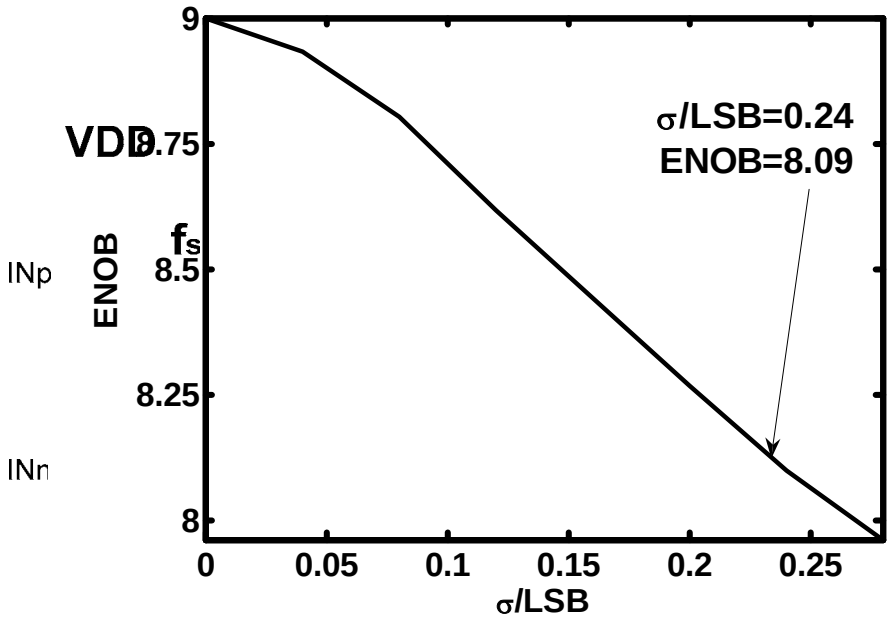
Small comparator noise is required for SA ADC



$$\sigma_V < 0.25LSB : -1bit\ \mathrm{degrade}$$

$$\sigma_V < 0.15LSB : -0.5bit\ \mathrm{degrade}$$





V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

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Analysis of comparator noise

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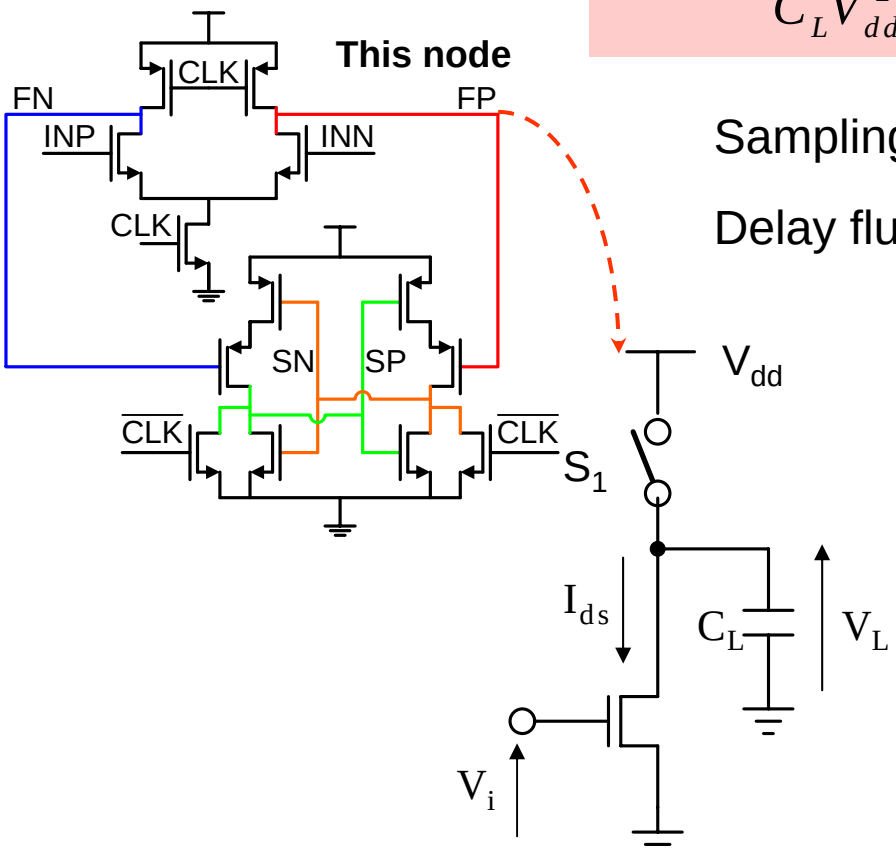
Noise of dynamic comparator is mainly determined by internal capacitance.
Thus low noise comparator consumes dynamic power

Our original work

$$\delta V_{in}^2 = \frac{4kTV_{eff}^2}{C_L V_{dd}^2}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$



Sampling noise

$$\left\langle v_n^2\right\rangle = \frac{kT}{C_L}, \delta_{td}^2 = \frac{\left\langle v_n^2\right\rangle}{\left(\frac{I_{ds}}{C_L}\right)^2} = \frac{kTC_L}{I_{ds}^2}$$

Delay fluctuation

$$\delta_{t_d}^2 = \frac{1}{I_{ds}^2}\left\langle\left(\int_0^{t_d} i_n dt\right)^2\right\rangle$$

$$\delta_{t_d}^2 = \frac{t_d}{2I_{ds}^2}S_{in} = \frac{2kT\gamma t_d}{I_{ds}V_{eff}} = \frac{kT\gamma C_L V_{dd}}{I_{ds}^2 V_{eff}}$$

$$\delta_{t_d}^2 = \frac{kT\gamma C_L V_{dd}}{I_{ds}^2 V_{eff}} + \frac{kTC_L}{I_{ds}^2} = \frac{kTC_L}{I_{ds}^2}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

$$\delta V_{in}^2 = \left(V_{eff}\frac{\Delta t_d}{t_d}\right)^2 = \left(\frac{V_{eff}}{t_d}\right)^2\delta_{td}^2 = \left(\frac{V_{eff}}{t_d}\right)^2\frac{kTC_L}{I_{ds}^2}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

$$= \frac{4kTV_{eff}^2}{C_L V_{dd}^2}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

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Sensitivity of comparator and FoM of ADC

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The larger capacitance is required to realize higher resolution ADC. This results in increase of FoM.

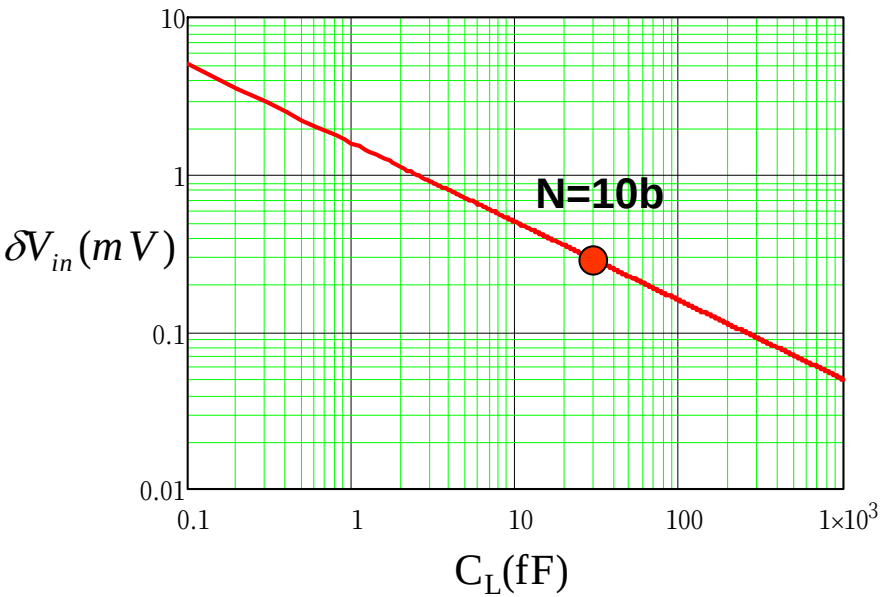
Our original work

$$\delta V_{in} \propto \sqrt{\frac{1}{C_L}} \qquad FoM \propto \frac{2(N+2)C_L V_{dd}^2}{2^N}$$

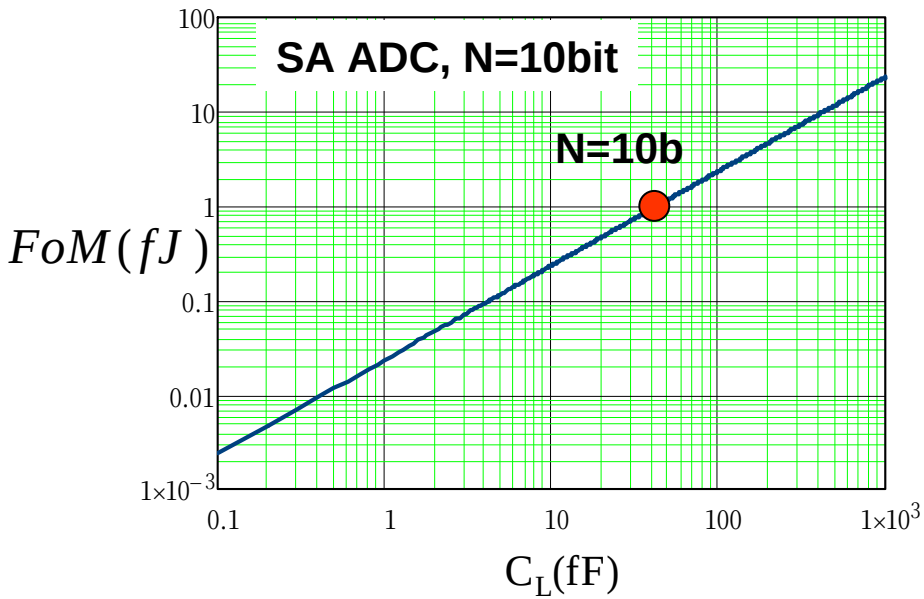
$$\delta V_{in}^2 = \frac{4kTV_{eff}^2}{C_L V_{dd}^2}\left(\gamma \frac{V_{dd}}{V_{eff}} + 1\right)$$

V_{dd}=1.0V, V_{eff}=0.3V, γ=1, T=300K

Sensitivity of comparator



FoM of ADC



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Expected FoMs for comparators

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FoM due to comparator in not negligibly small.
Recent SA ADCs are reaching the limit.

Measured FoM=4.4fJ/conv, Expected FoM is 1.4fJ/conv.

Our original work

$$\delta V_{in}^2 = \frac{4kTV_{eff}^2}{C_L V_{dd}^2}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

$$\frac{\delta V_{in}}{q} < 0.15 \rightarrow \delta V_{in}^2 < 0.3V_{qn}^2$$

$$\therefore \delta V_{in}^2 < 0.1\left(\frac{V_{dd}}{2^N}\right)^2$$

$$C_L > \frac{40kTV_{eff}^2 2^{2N}}{V_{dd}^4}\left(\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

$$C_L > 4\times10^{-20}\times 2^{2N}$$

$$p_d = 2(N+2)f_c C_L V_{dd}^2$$

f_c=100MS/s

$$\gamma = 1, V_{dd} = 1.0V, V_{eff} = 0.2V$$

$$FoM = \frac{p_d}{f_c \times 2^{N-0.5}}$$

Resolution	10	12	14
C_L(fF)	42	670	11000
P_d(mW)	0.1	1.9	34
FoM(fJ)	1.4	6.5	30

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Comparison of FoM

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FoM of SA ADC is one order of magnitude lower than that of pipeline ADC

Pipeline ADC

Resolution	10	12	14
C_o(pF)	0.37	6.0	95
I_{dd}(mA)	1.75	33.6	628
P_d (mW)	1.75	33.6	628
FoM(fJ)	24	116	542

Our original work

FoM=63fJ/Conv. step

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet, "A 1.2V 4.5mW 10b, 100MS/s Pipeline ADC in a 65nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.250-251, Feb. 2008.

SA ADC

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Technology trend of ADCs

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SA ADCs become major, but….

Architecture	Flash	Two-step parallel	Pipeline	SA
Period	78---88---	88 --- 95--	95-- 1x--	06--
Technology	Bipolar/CMOS	Bi-CMOS, CMOS	CMOS	CMOS
Parallel/Serial	Parallel	Two-step, Semi-parallel	Serial (Pipeline)	Serial
Base	Comparator	Comparator	Amplifier	Comparator
Gain	No	No (Yes Interpolation)	Yes	No
Sampling	No	Yes	Yes	Yes
Accuracy	Transistor mismatch	Comparator mismatch Comparator noise Settling	Capacitor mismatch Amplifier gain OpAmp noise Settling	Capacitor mismatch Comparator noise
Speed	Device fT	Reference+Switch Comparator+Logic	OpAmp GBW Switch	Comparator+Logic Switch
Design technique	Interpolation Averaging Folding Dynamic comparator	Redundancy Interpolation Averaging Gain boost Dynamic comparator	Redundancy (1.5b) Gain boost OpAmp sharing Calibration	Serial Capacitor Dynamic comparator Interleaving Calibration

Summary

- **Pipelined ADCs, current major ADC architecture are now facing serious issues;**
  - **Need static current**
  - **Low OpAmp gain**
  - **Low voltage operation→ larger capacitance**
  - **Scaled device is not suitable for higher resolution**

- **SA ADCs becomes attractive and looks suitable for scaled CMOS**
  - **Extremely small FoM**
  - **Simple, needs only capacitors, switches, comparators, and logics.**
  - **No static current**
  - **Free from OpAmp issues**

- **What determines FoM and which is better.**
  - **Pipeline: OpAmp SA ADC: Comparator**
  - **SA is 10x better in FoM, however the difference is not so large.**
  - **FoM is reaching theoretical limit**
  - **Attention to the sensitivity of comparator for SA ADC design.**