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Technology Trend of ADCs

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Contents

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- Issues of pipeline ADCs
- Revolution of SA ADCs
- Fight back of pipelined ADCs
- What determines FoM
- Summary

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Mega-technology trend of ADCs

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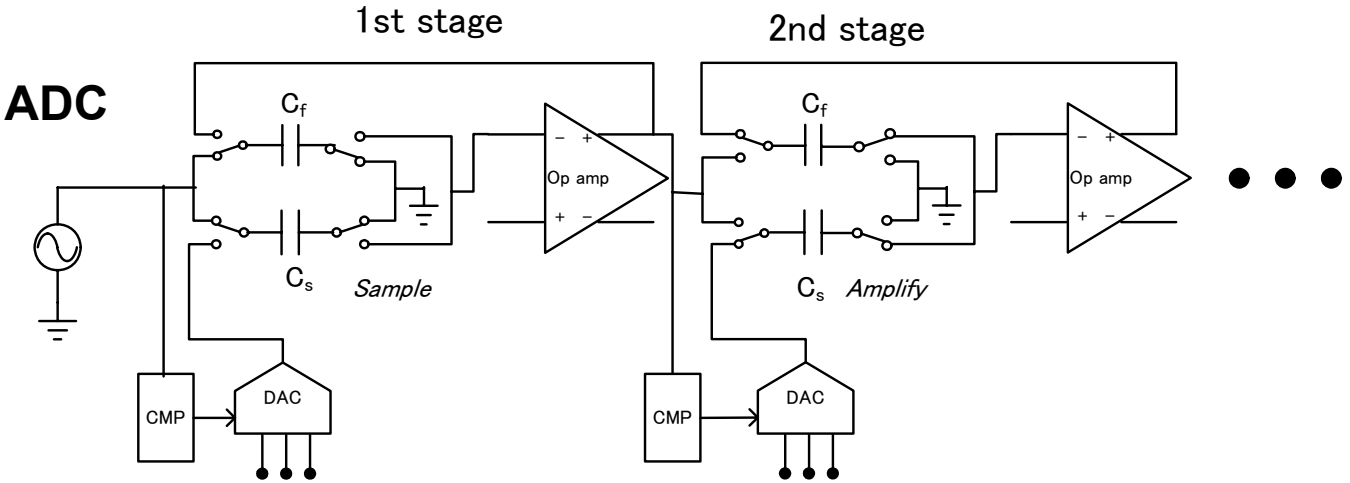
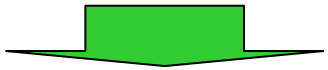
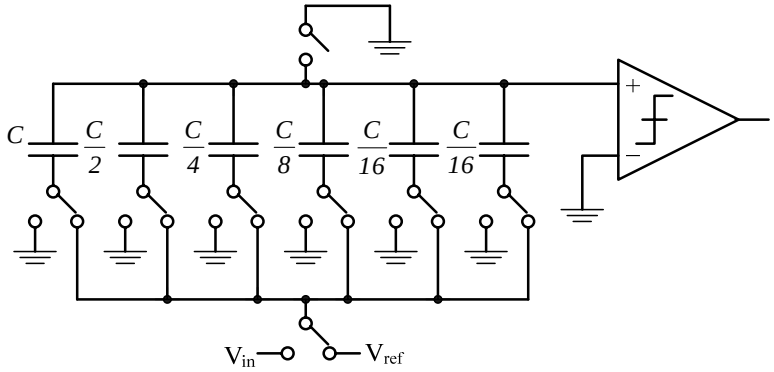
Major conversion scheme is now changing from pipeline to SA

Pipeline ADC





SA ADC



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Issues of pipeline ADCs

(current major ADC architecture)

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Pipeline ADC

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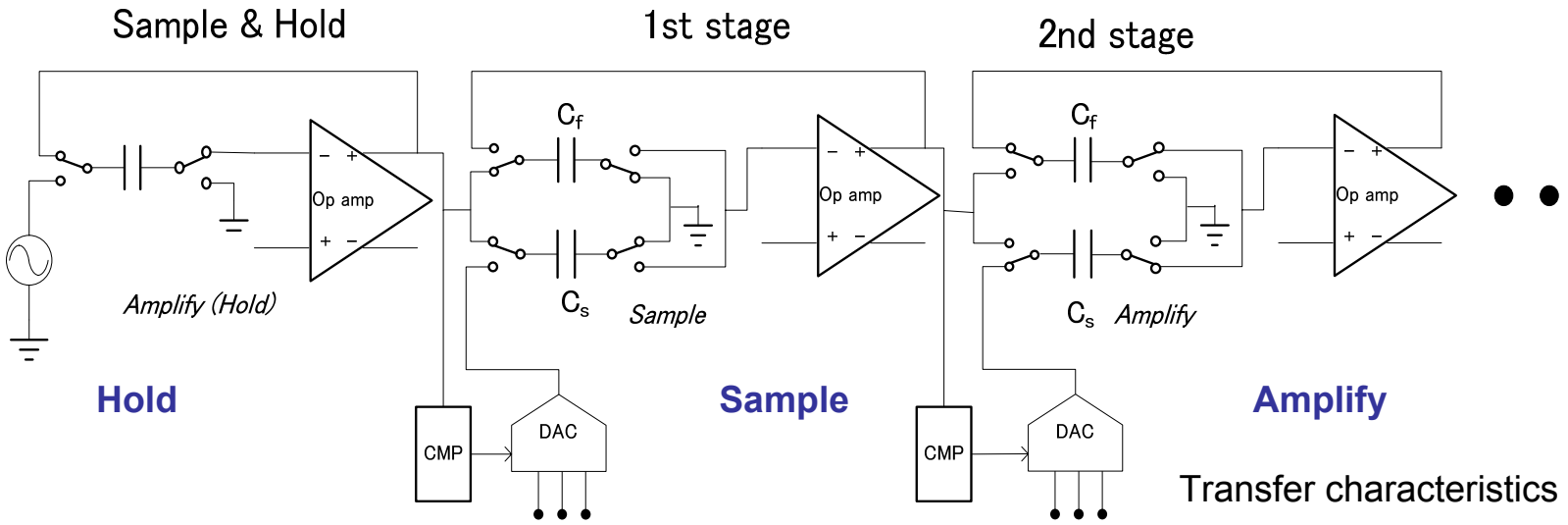
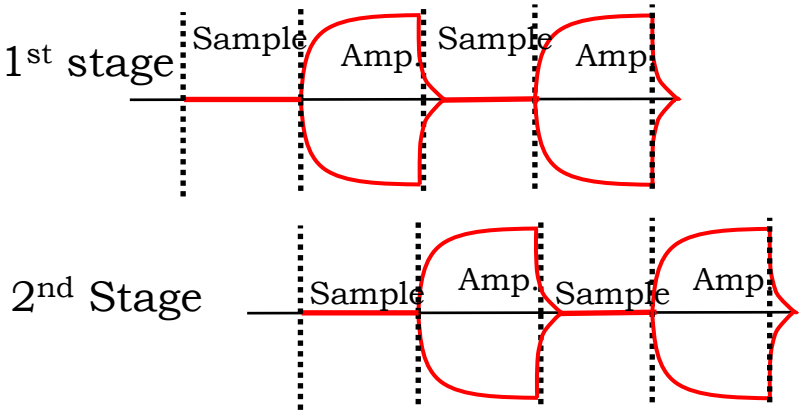
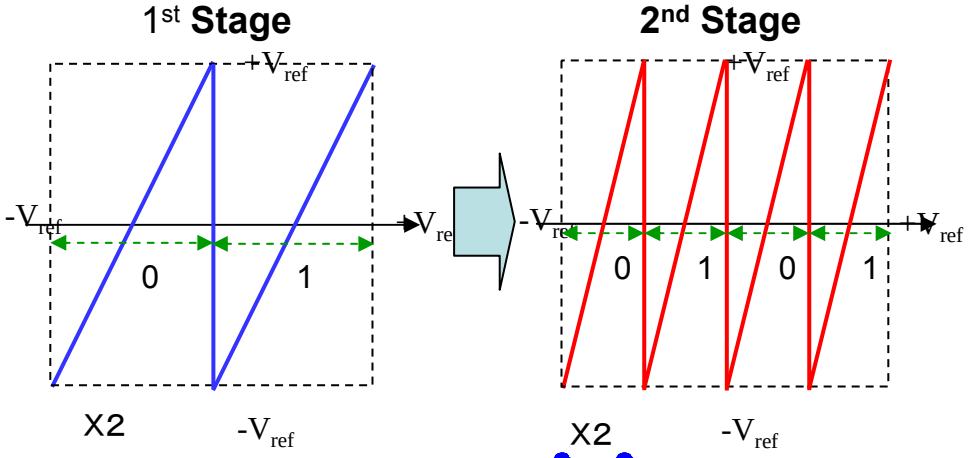
Folding I/O characteristics makes higher resolution along with pipeline stages.



Transfer characteristics





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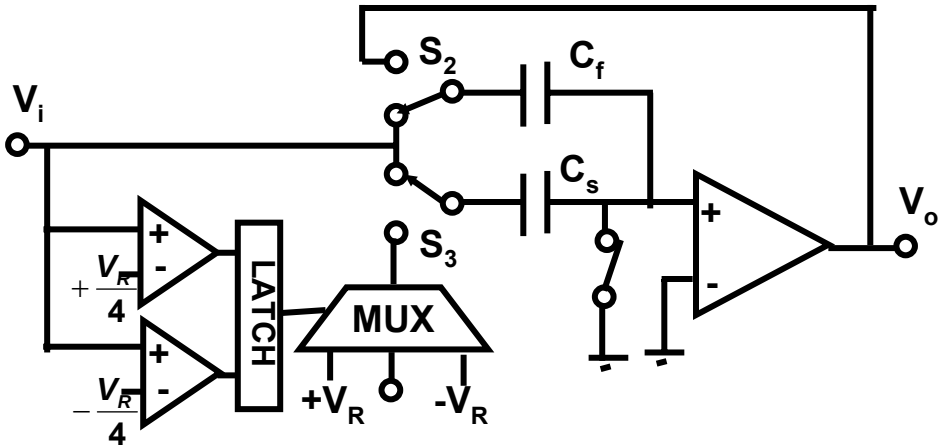
1.5-bit/stage Pipeline ADC

Amplification at each stage reduces the input referred thermal noise.
1.5b/stage architecture reduces the requirement for the comparator offset drastically.

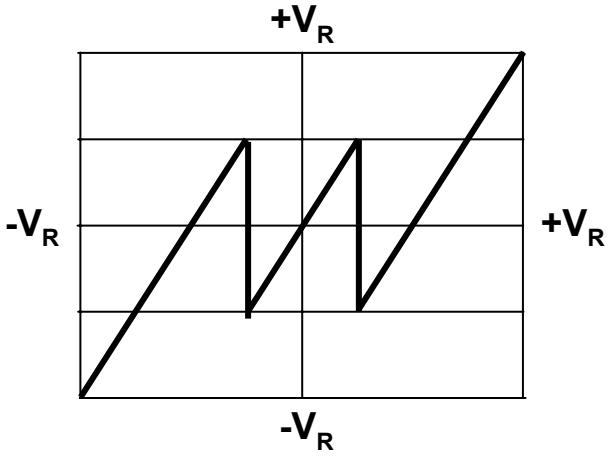
Lewis et al., *JSSC* '92
Ginetti et al., *JSSC* '92

Amplifiers determine ADC performance
Comparators don't affect the performance.



SUB-ADC **DAC** **2X GAIN**

Transfer characteristics



$$V_o = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_i + \frac{C_i}{C_f}V_{ref} & \text{if} \quad Vi < -\frac{V_{ref}}{4} \\ \left(1+\frac{C_s}{C_f}\right)V_i & \text{if} \quad -\frac{V_{ref}}{4} \le V_i \le \frac{V_{ref}}{4} \\ \left(1+\frac{C_s}{C_f}\right)V_i - \frac{C_i}{C_f}V_{ref} & \text{if} \quad V_i > \frac{V_{ref}}{4} \end{cases}$$

Unit conversion stage
for 1.5-bit/stage pipeline ADC

Issues of pipeline ADCs

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Major issues of pipeline ADCs are caused by OpAmp.

$$G_{DC}(dB) > 6N + 10$$

$10b : 70dB$

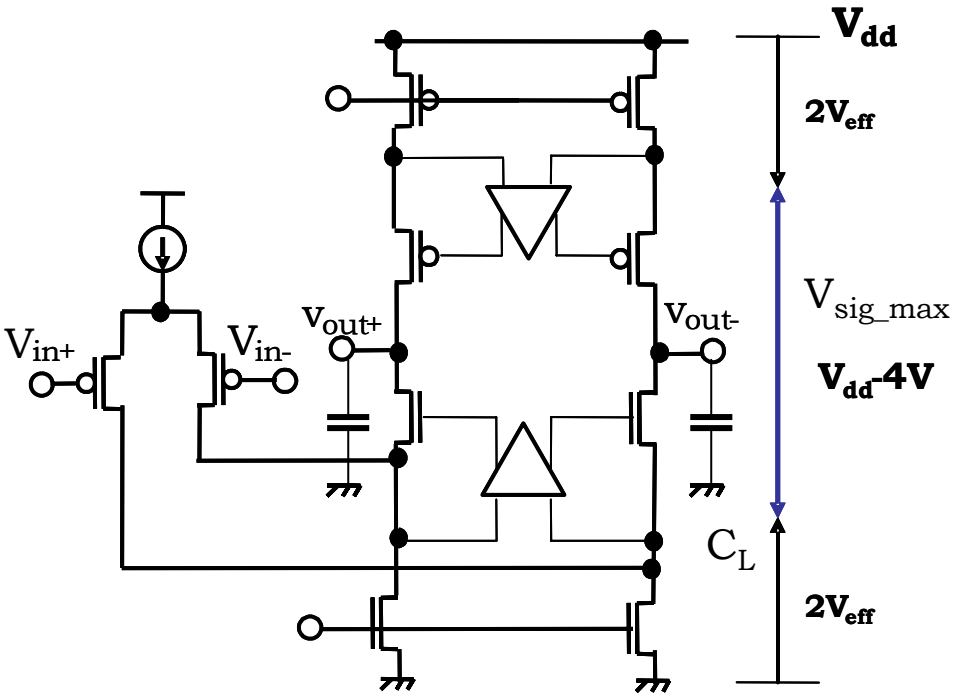
$12b : 82dB$

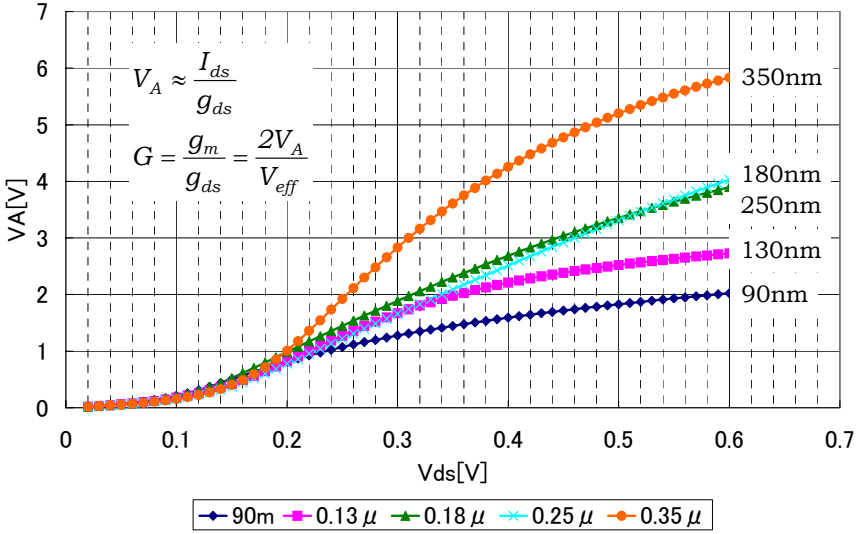
Sub-100nm CMOS

$$G_{DC} \approx \left(\frac{V_A}{V_{eff}}\right)^n \approx \left(\frac{1}{0.15}\right)^n \approx 16dB \times n$$

$n < 5$

$G_{DC} < 80dB$





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Performance model for pipeline ADC

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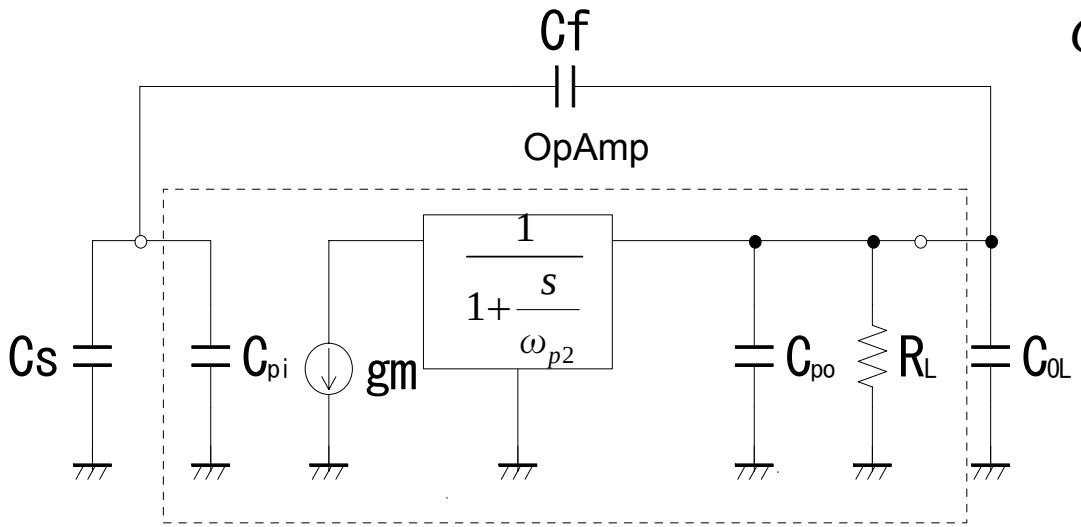
We have developed the performance model for pipeline ADC that can treat technology scaling.



$$GBW_{\_close} = \frac{g_m}{2\pi C_L}\beta > \frac{N}{3} f_c$$

$$\beta = \frac{C_f}{C_f + C_s + C_{pi}}$$

$$C_L = C_{po} + C_{oL} + \frac{C_f (C_s + C_{pi})}{C_f + C_s + C_{pi}}$$

$$C_{oL} = \frac{C_s + C_f}{2} \qquad C_o = C_s = C_f = C_{oL}$$

g_m : *Transconductance of input stage*
C_s, C_f : *Signal capacitance for feedback loop*
C_{pi}, C_{po} : *input & putput paracitic capacitance*
C_{oL} : *Load capacitance*
R_L : *Output resistance*
ω_{p2} : *Second pole of OpAmp*

$$GBW_{\_close} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2 + \frac{C_{pi}}{C_o}\right)\left(1 + \frac{C_{po}}{C_o}\right) + \left(1 + \frac{C_{pi}}{C_o}\right)}$$

$$= \frac{I_{ds}}{\pi C_o V_{eff}} \frac{1}{\left(2 + \frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1 + \frac{\alpha_{po} I_{ds}}{C_o}\right) + \left(1 + \frac{\alpha_{pi} I_{ds}}{C_o}\right)}$$

A. Matsuzawa, "Analog IC Technologies for Future Wireless Systems," IEICE, Tan on Electronics, Vol. E89-C, No.4, pp. 446-454, April, 2006.

C_p and C_o for several design rules

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C_p will be reduced by technology scaling, however C_o will be increased by operating voltage reduction.

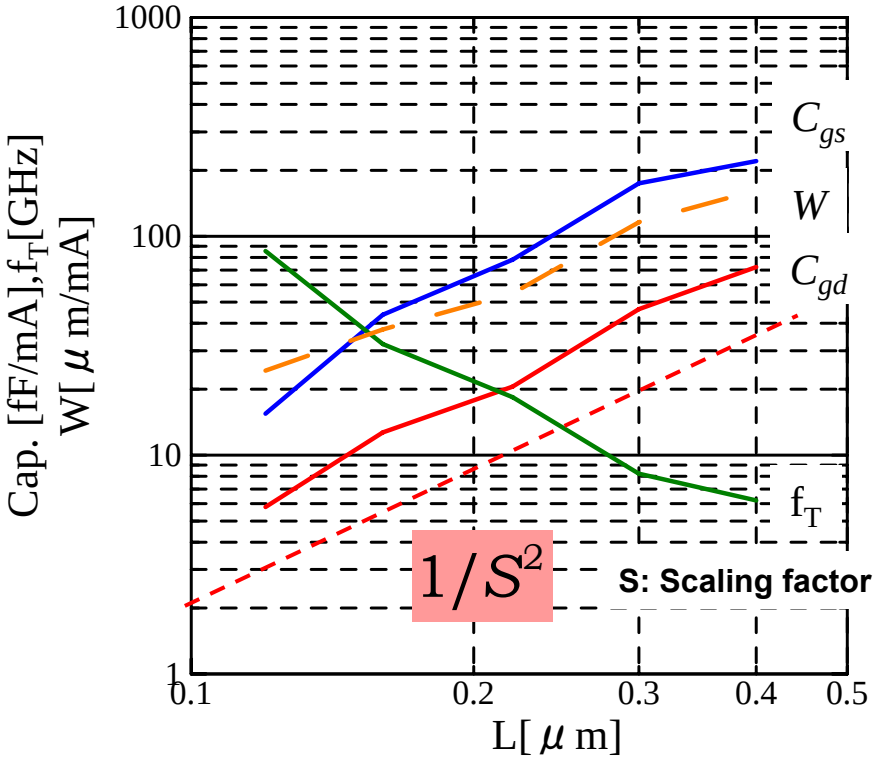
$$W = \frac{2L}{\mu C_{ox} V_{eff}^{\ 2}} I_{ds} \qquad V_{eff}=0.175\text{V}$$

$$C_o \geq 1.66 \times 10^{-19} \left(\frac{2^N}{V_{sig}} \right)^2$$

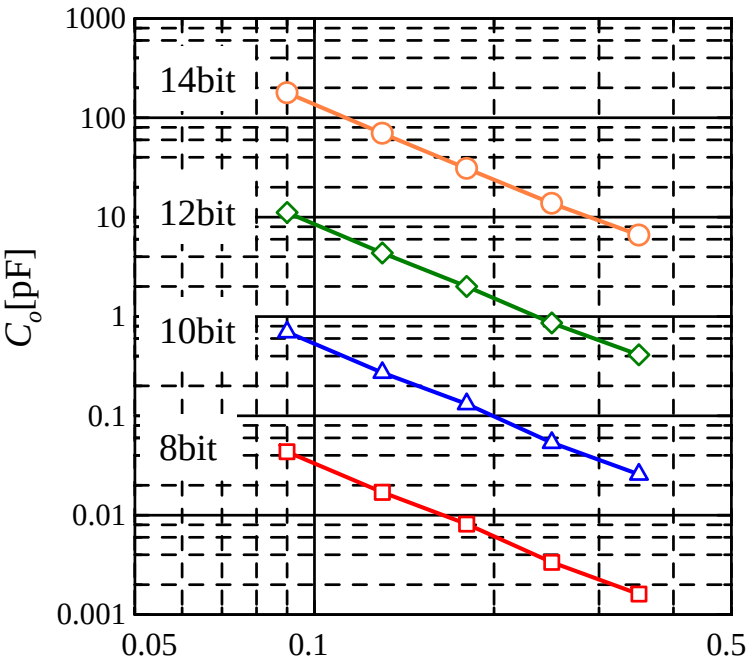
$$V_{sig} = 2\left(V_{dd} - 2 \cdot m \cdot V_{eff}\right)$$

Single stage: m=2
Double Stage: m=1

C_p/I & W/I vs. design rule



C_o vs. design rule m=2



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Performance summary

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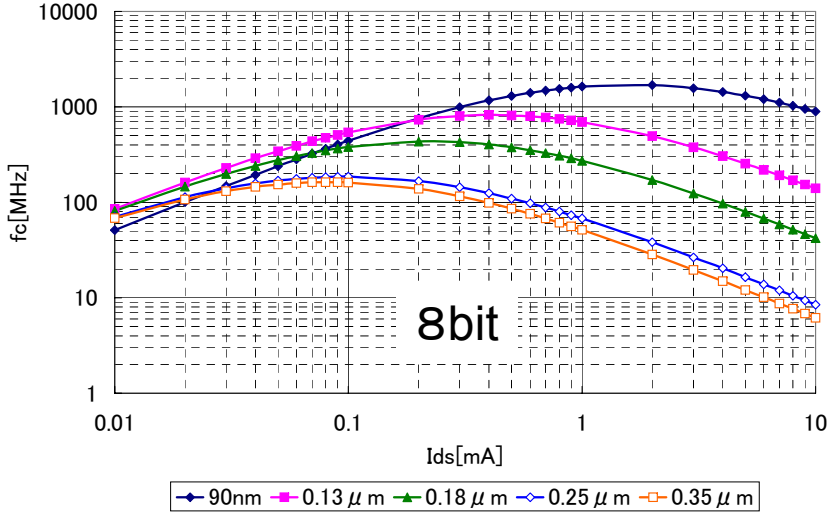
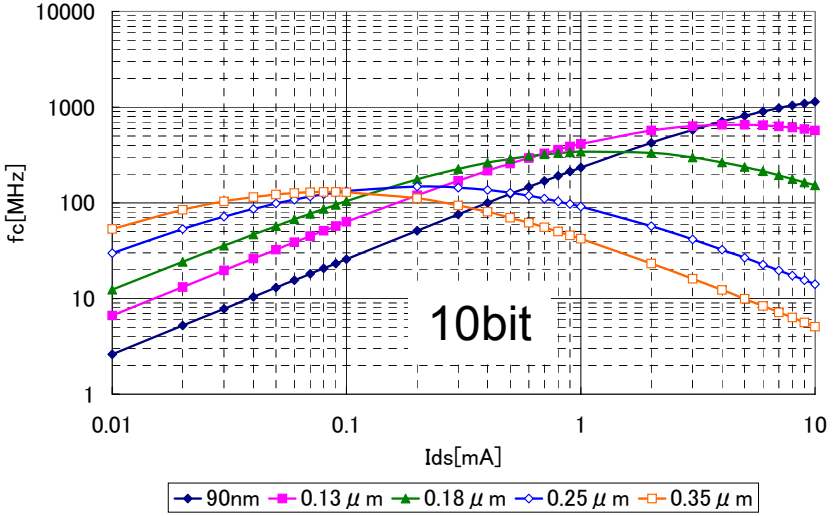
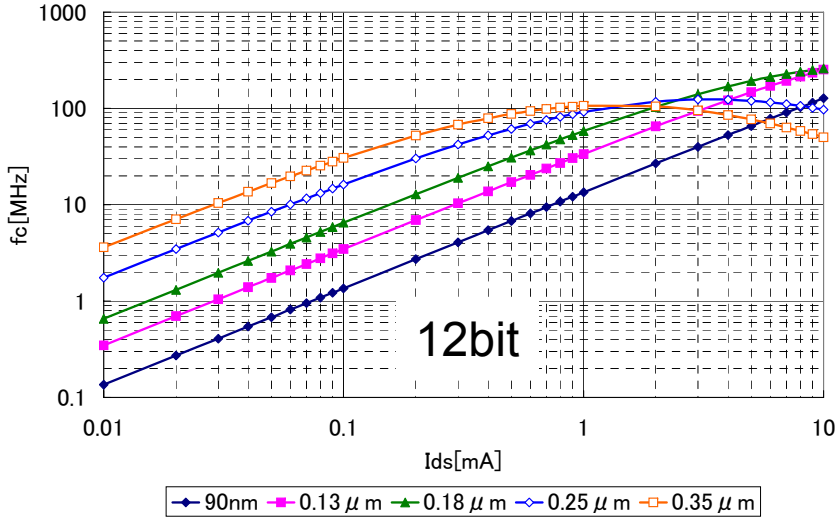
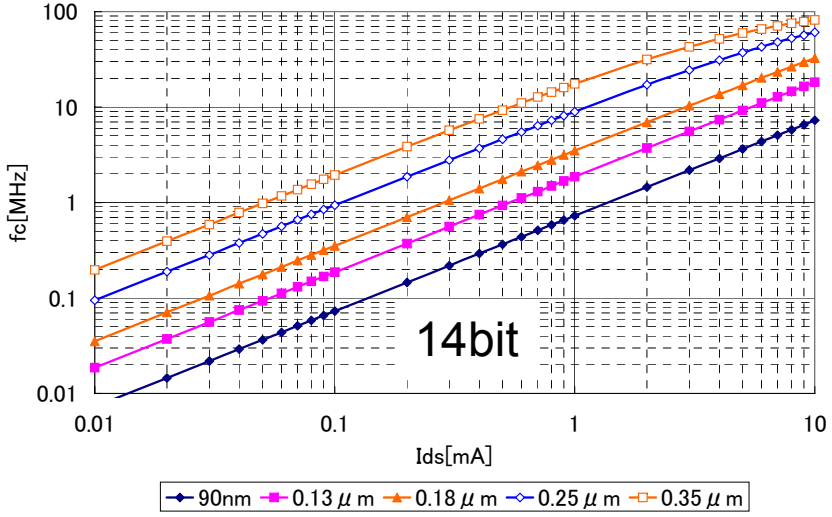
Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.









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Speed and power

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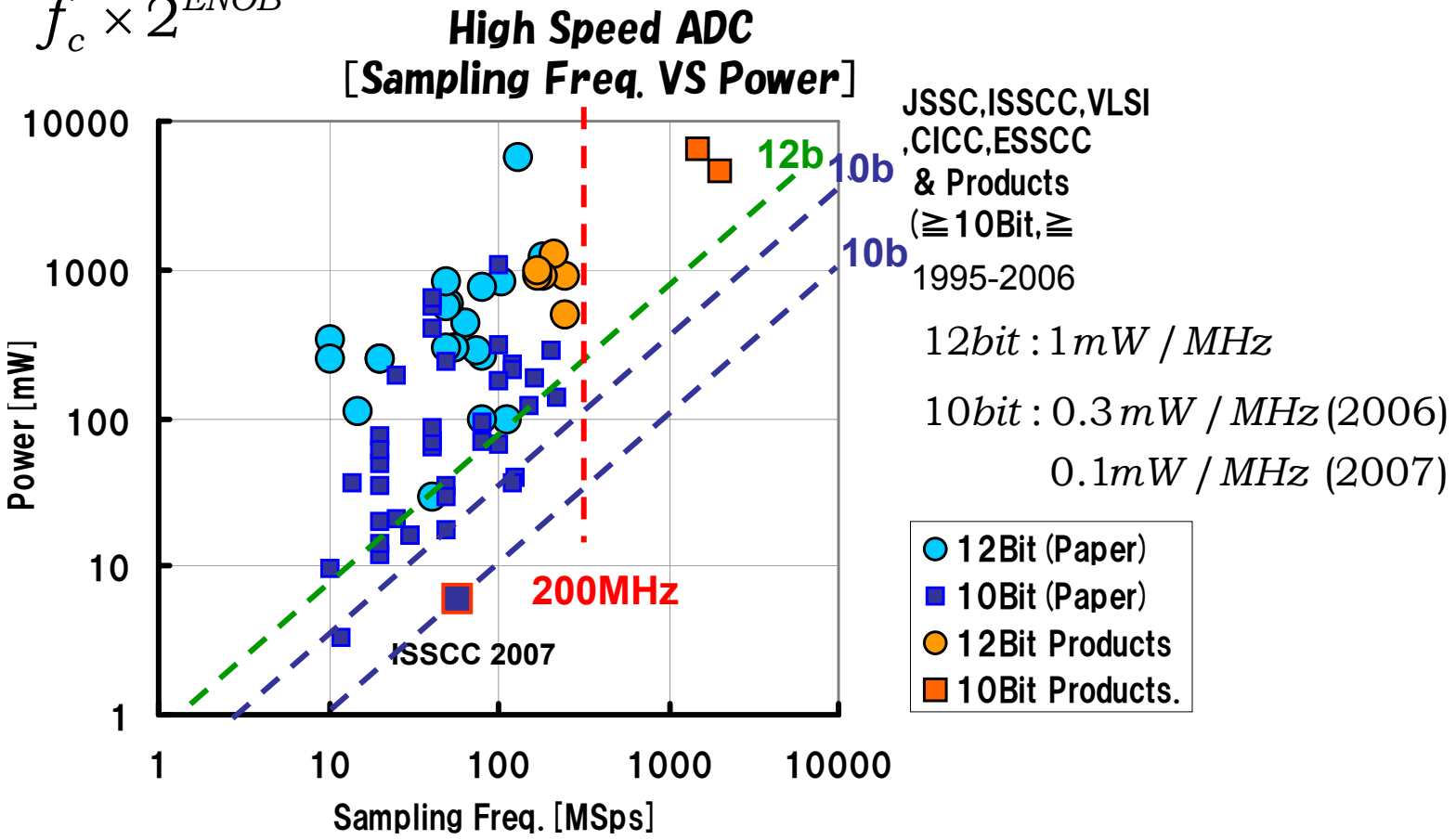
Conversion speed has saturated at 200 MHz
Lower mW/MHz is needed for low power operation.

$$FoM = \frac{P_d}{f_c \times 2^{ENOB}}$$

600 fJ -- 200fJ/Conv-steps



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Revolution of SA ADCs

(Low FoM ADC architecture)

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SA ADC

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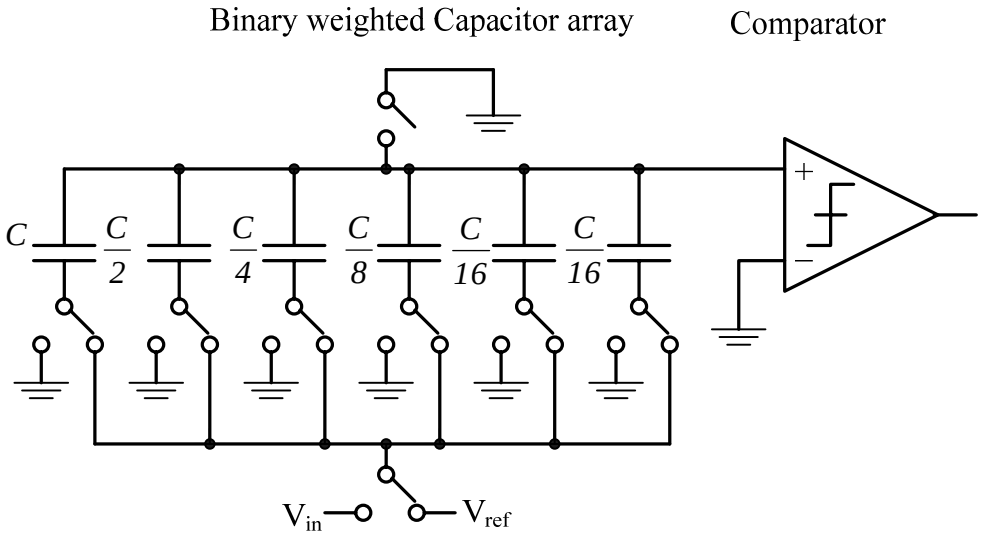
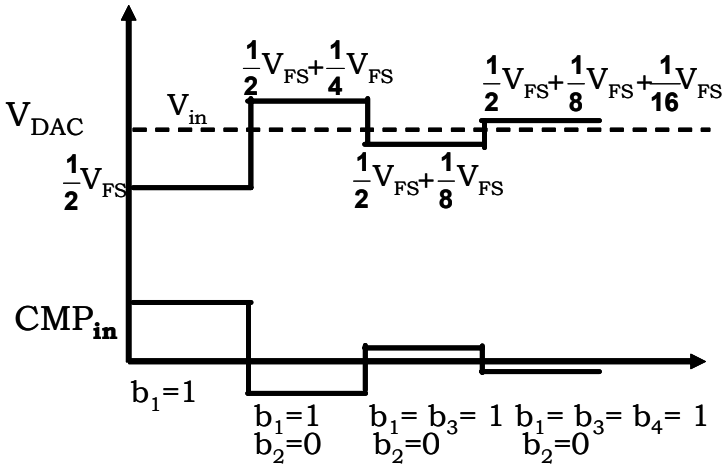
Successive Approximation ADC is free from OpAmp design issues and looks suitable for sub-100nm CMOS era.

Require only capacitors, switches, comparator, and logics.

No quiescent current → extremely low power



Binary search algorithm



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Performance overview of SA ADCs

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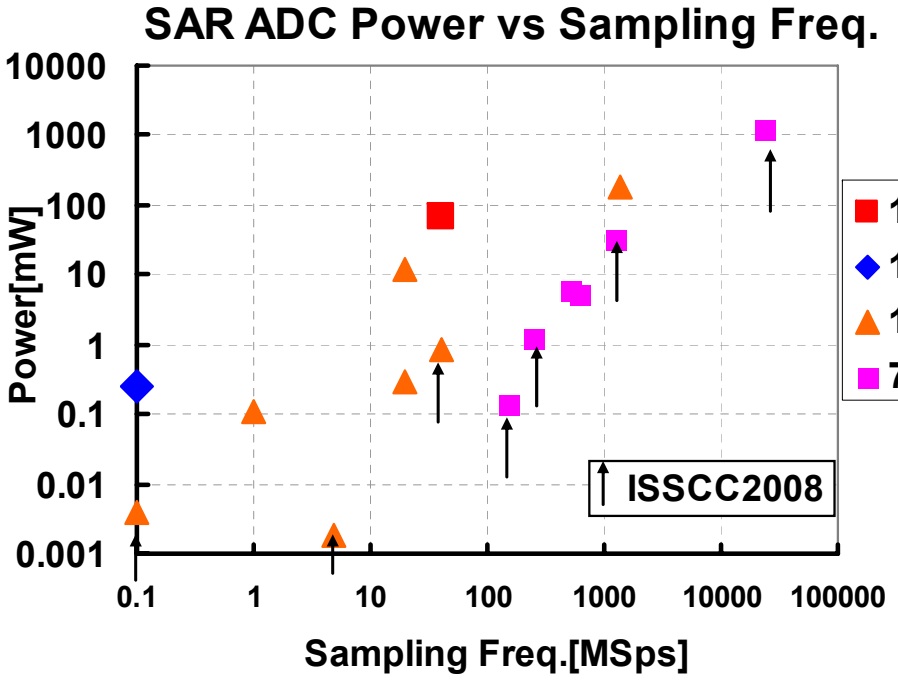
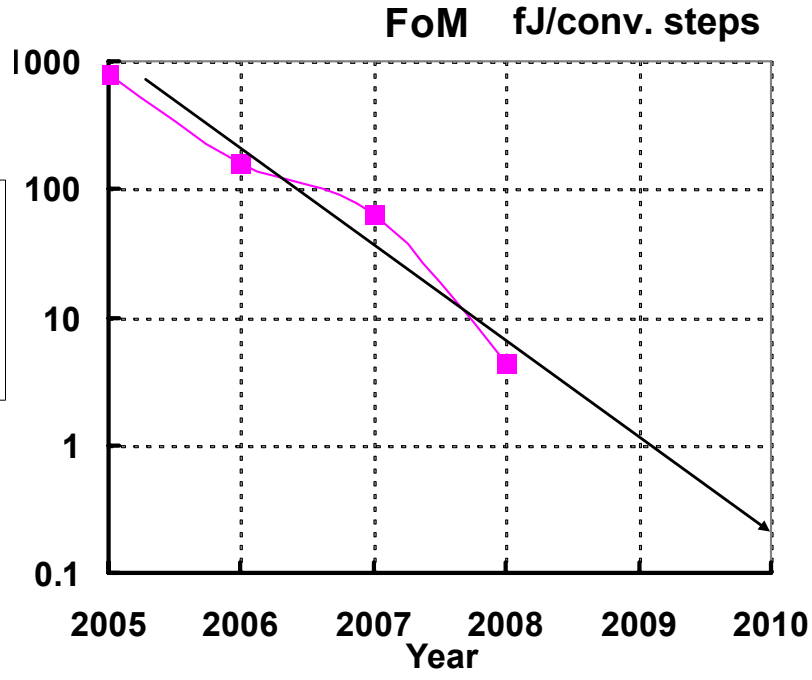
SA ADCs become dominant in every performance range.
In particular FoM has rapidly lowered.

1/200 during past three years.

Courtesy Y. Kuramochi





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Recent SA ADC

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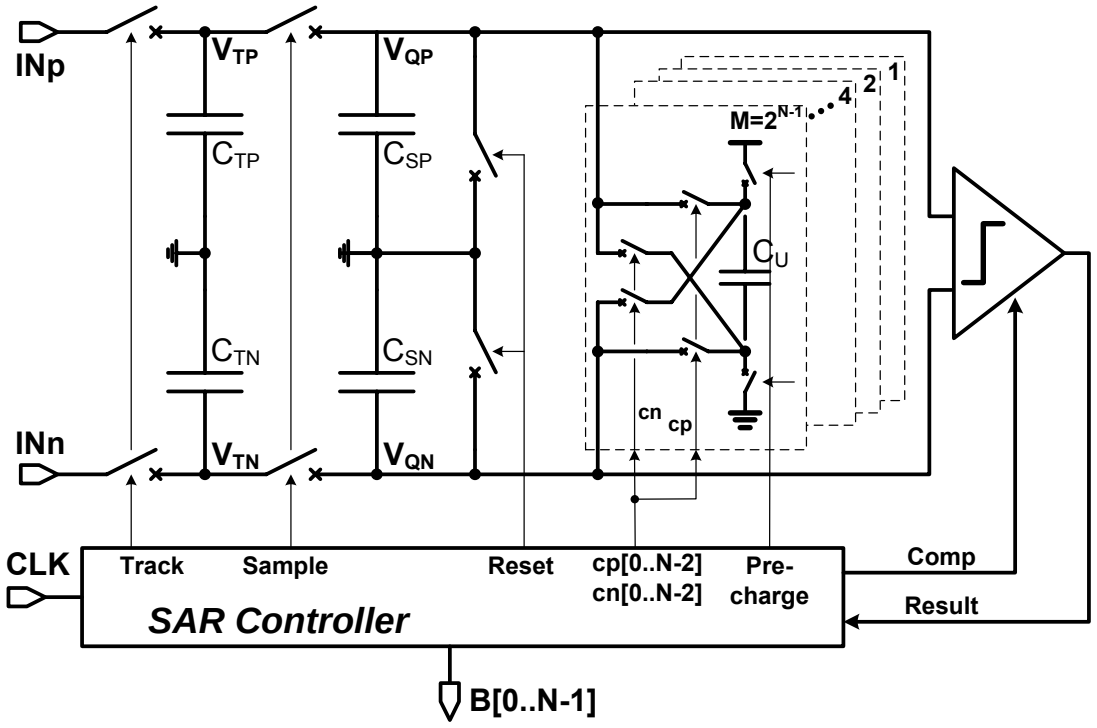
SAR ADC must be one of the good solution for scaled analog technology.
No OpAmp is needed.

No static power consumption.
Higher signal swing and small capacitance



$$Q_{REF} = \sum_i 2^i C_U \cdot V_{DD}$$

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

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Analog operation with capacitances

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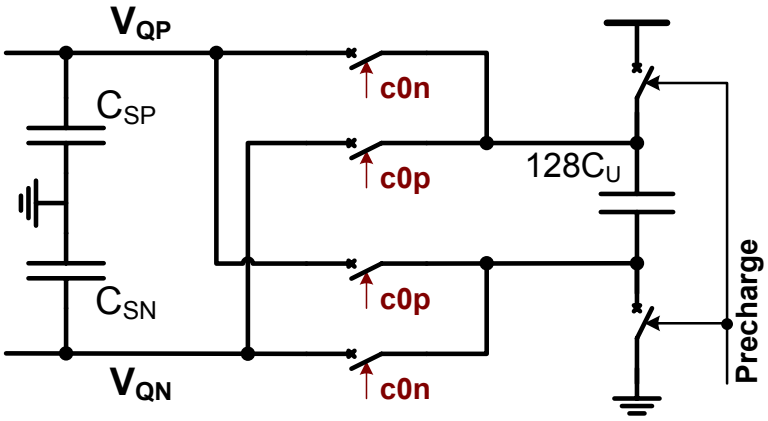
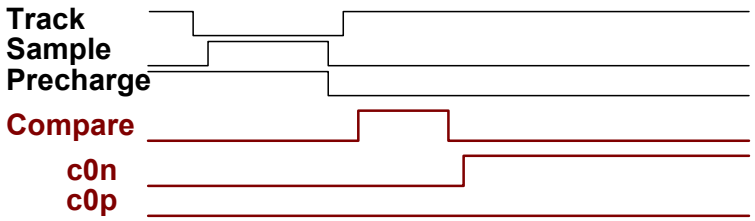
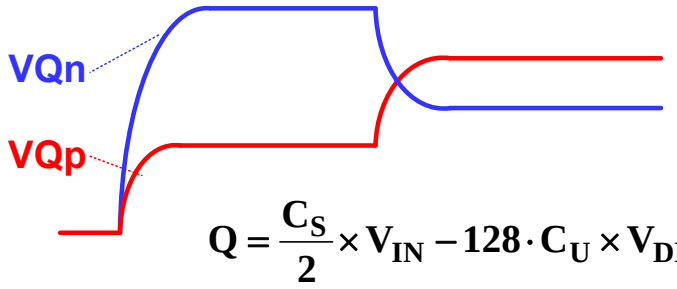
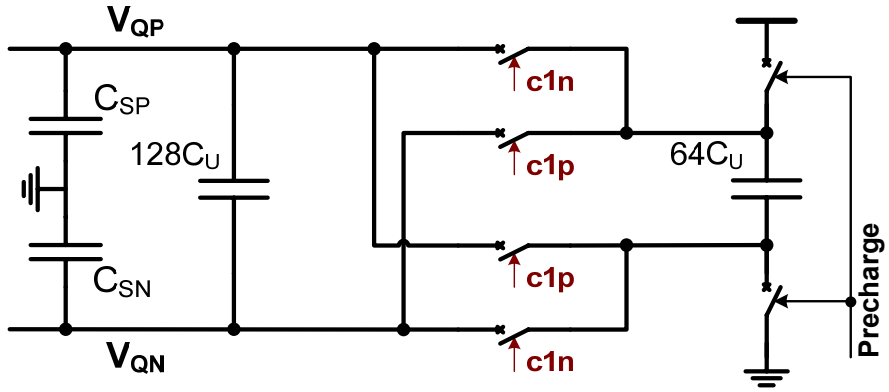
Capacitances can realize analog operation for SAR ADC.
No static current is required and higher signal swing can be used.

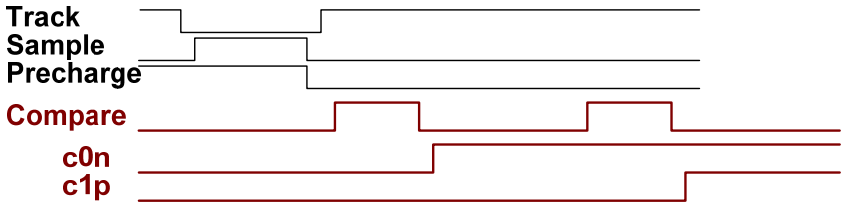


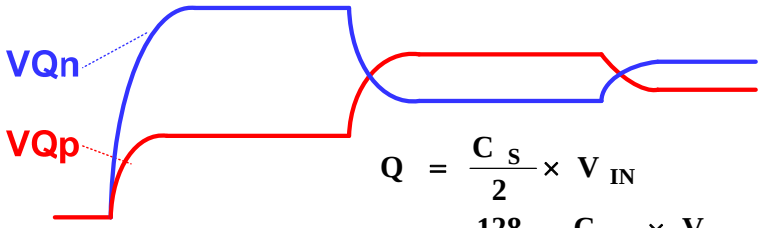




$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD}$$







$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD} + 64 \cdot C_U \times V_{DD} \pm \ldots$$

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Results

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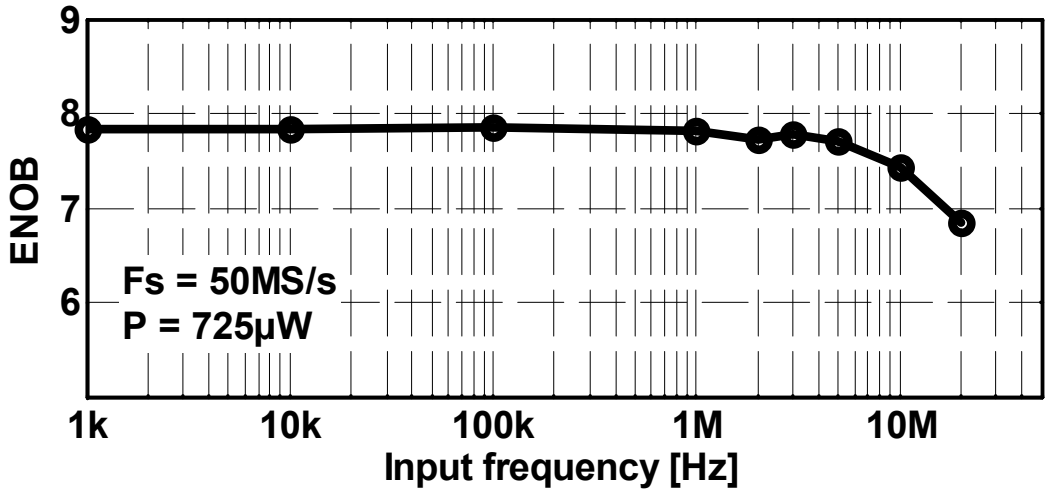
Amazing small FoM=65fJ/conv.-steps has been attained.



8bit, 0.3mW at 20MHz

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

ISSCC06 Paper #	Arch.	Fs [MS/s]	ENOB	P [mW]	FoM [fJ]	FoM includes		
						Ref.	Clock	Dec.
3.1	CTΔΣ	40	12	50	300	-	Yes	Yes
3.4	ΔΣ	4.4	12.6	13.8	500	-	No	No
12.1	PL	100	9.4	39	570	-	-	-
12.3	Subr.	50	10.4	30	440	-	-	-
12.4	PL−CBSC	7.9	8.7	2.5	760	-	-	-
12.5	SAR	0.1	10.5	0.025	170	No	No	-
12.7	PL	50	9.2	15	510	-	-	-
31.1	Flash	1250	3.7	2.5	160	-	-	-
31.5	SAR	300	5.3	2.65	220	No	Yes	-
This work	**CS−SAR**	**20**	**7.8**	**0.29**	**65**	**Yes**	**Yes**	-

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High resolution and high speed SA ADC

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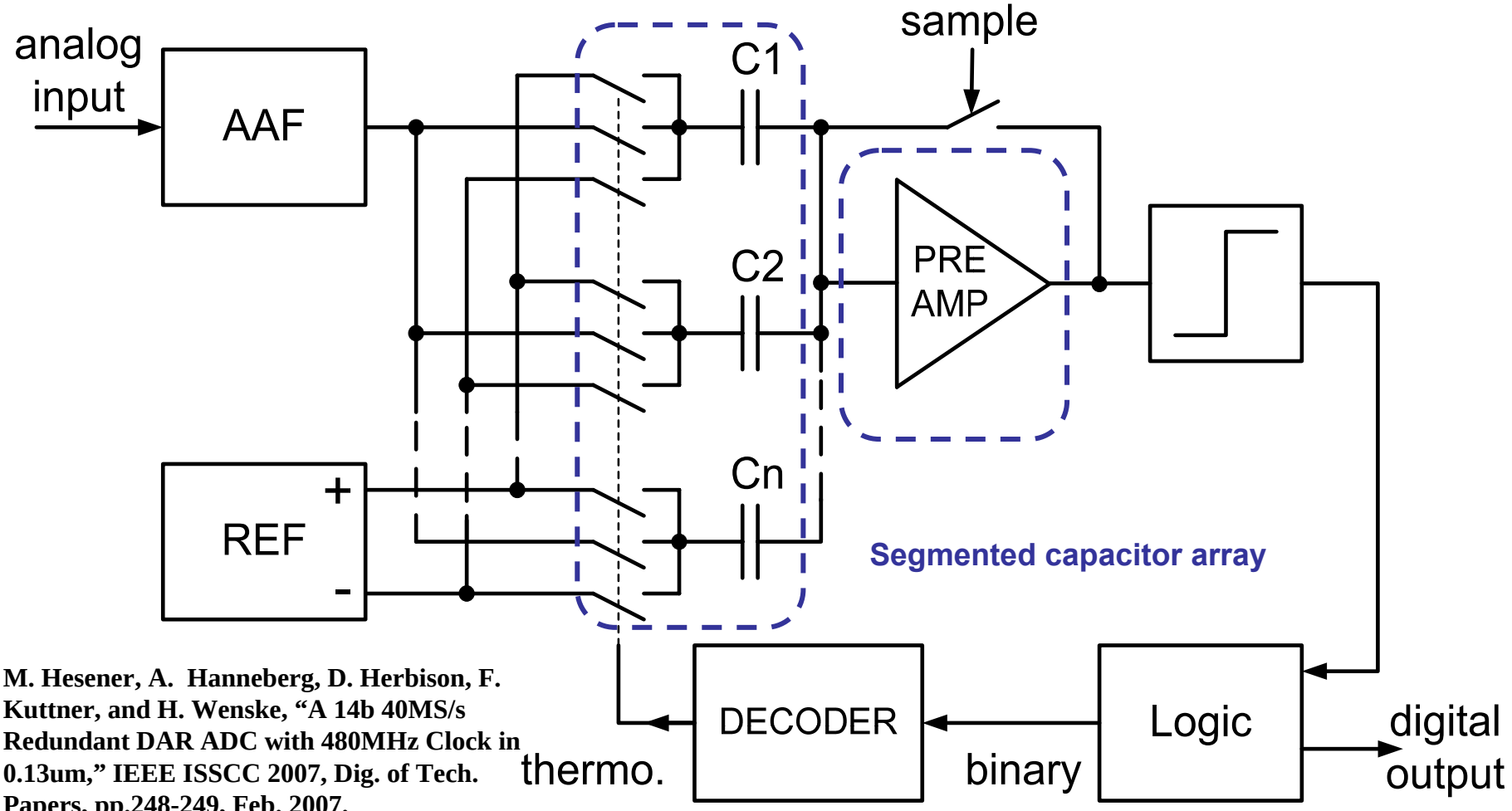
To increase the resolution, a pre-amplifier is located in front of a comparator



M. Hesener, A. Hanneberg, D. Herbison, F. Kuttner, and H. Wenske, "A 14b 40MS/s Redundant DAR ADC with 480MHz Clock in 0.13um," IEEE ISSCC 2007, Dig. of Tech. Papers, pp.248-249, Feb. 2007.

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Results

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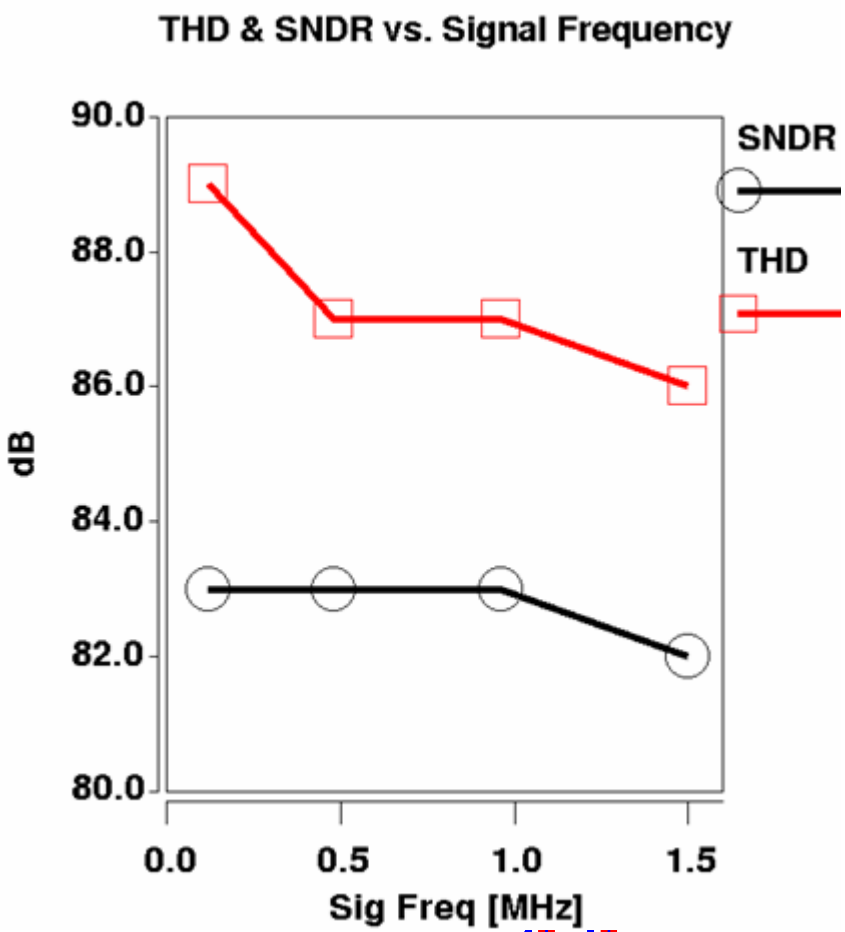
High conversion rate of 40MS/s and low power of 66mW have been attained

High ENOB of 13.5bit has been attained

High FoM=140fJ/conv-steps

0.13um CMOS

Supply voltage	1.5V
Input range	±0.9V diff.
Sample frequency	40MHz
Internal clock frequency	480MHz
Analog power	49mW
Digital power	17mW
Total power	**66mW**



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World lowest FoM ADC

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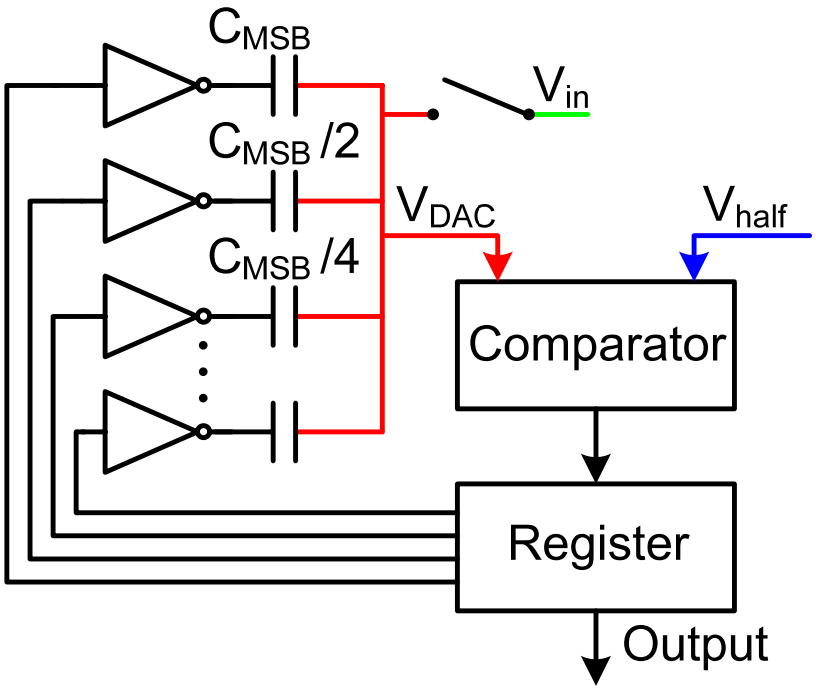
Extremely low FoM of 4.4fJ/conv-steps. SA ADC has been realized

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

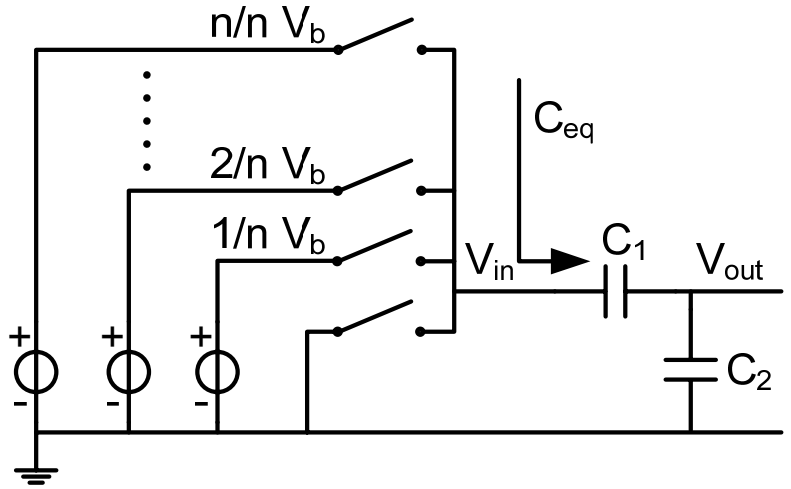
Multi-step charging can reduce energy more

$$E_{diss} = n \cdot \frac{1}{2} \cdot C_{eq} \cdot \left(\frac{V_b}{n}\right)^2 = \frac{1}{n \cdot 2} \cdot C_{eq} \cdot V_b^2$$

Simple SA architecture



Multi-step charging (Adiabatic charging)



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Summary of performance

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Extremely low FoM has been attained!!

	Average	Standard deviation
SNR (dB)	55.6	0.58
THD (dB)	-61.1	1.95
DNL (LSB)	0.49	0.06
INL (LSB)	2.24	0.18
SNDR (dB)	54.4	0.47
ENOB (bit)	8.75	0.08
$E_{conversion}$ (pJ/conversion)	1.9	
Figure Of Merit (fJ / conversion-step)	4.42	0.24

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Comparison with state-of-the-art ADCs

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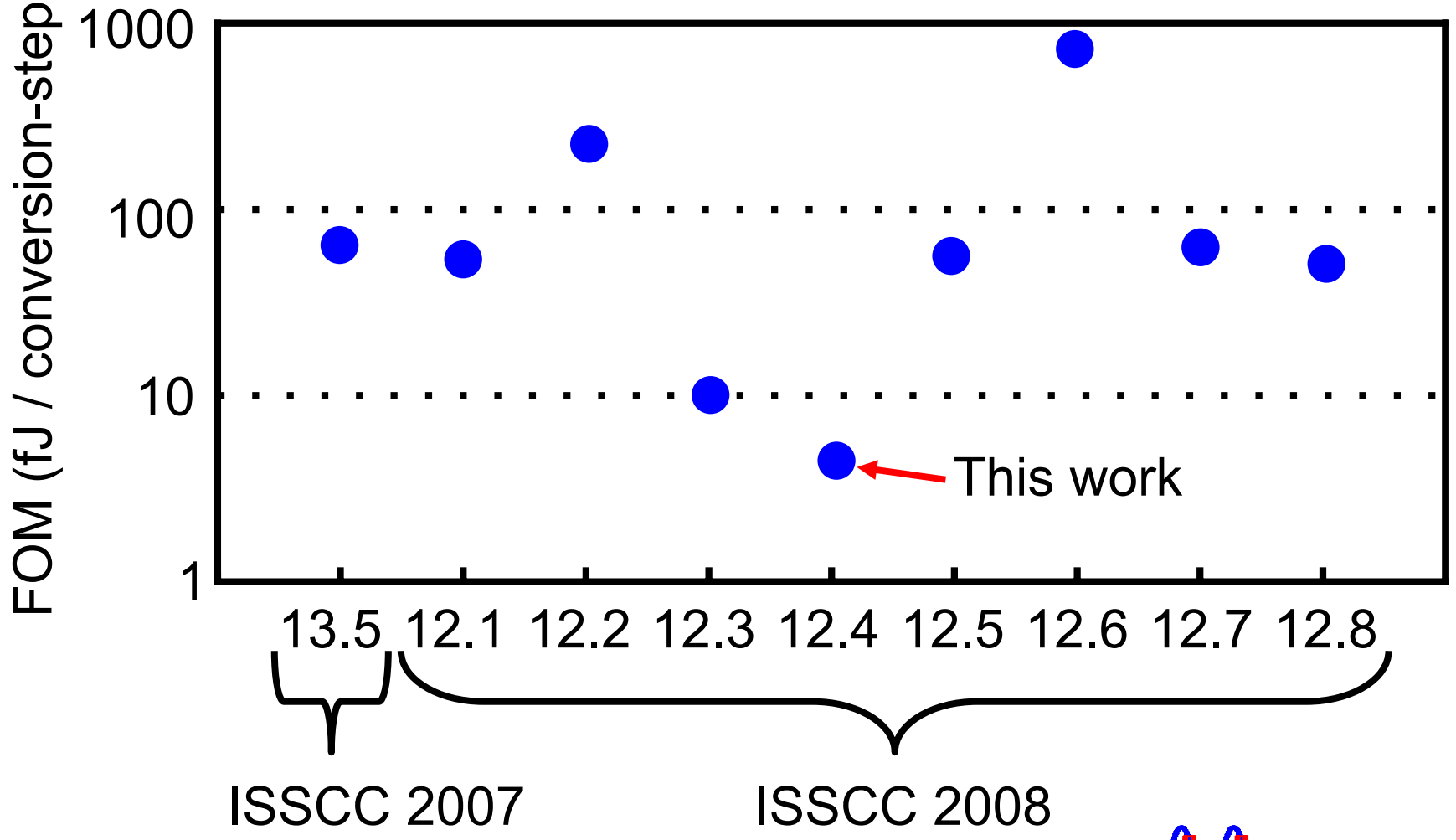
Low FoM <100fJ/conv.-steps ADCs become major.

4.4fJ/conv.-steps is the world lowest !!



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Massively parallel high speed SA ADC

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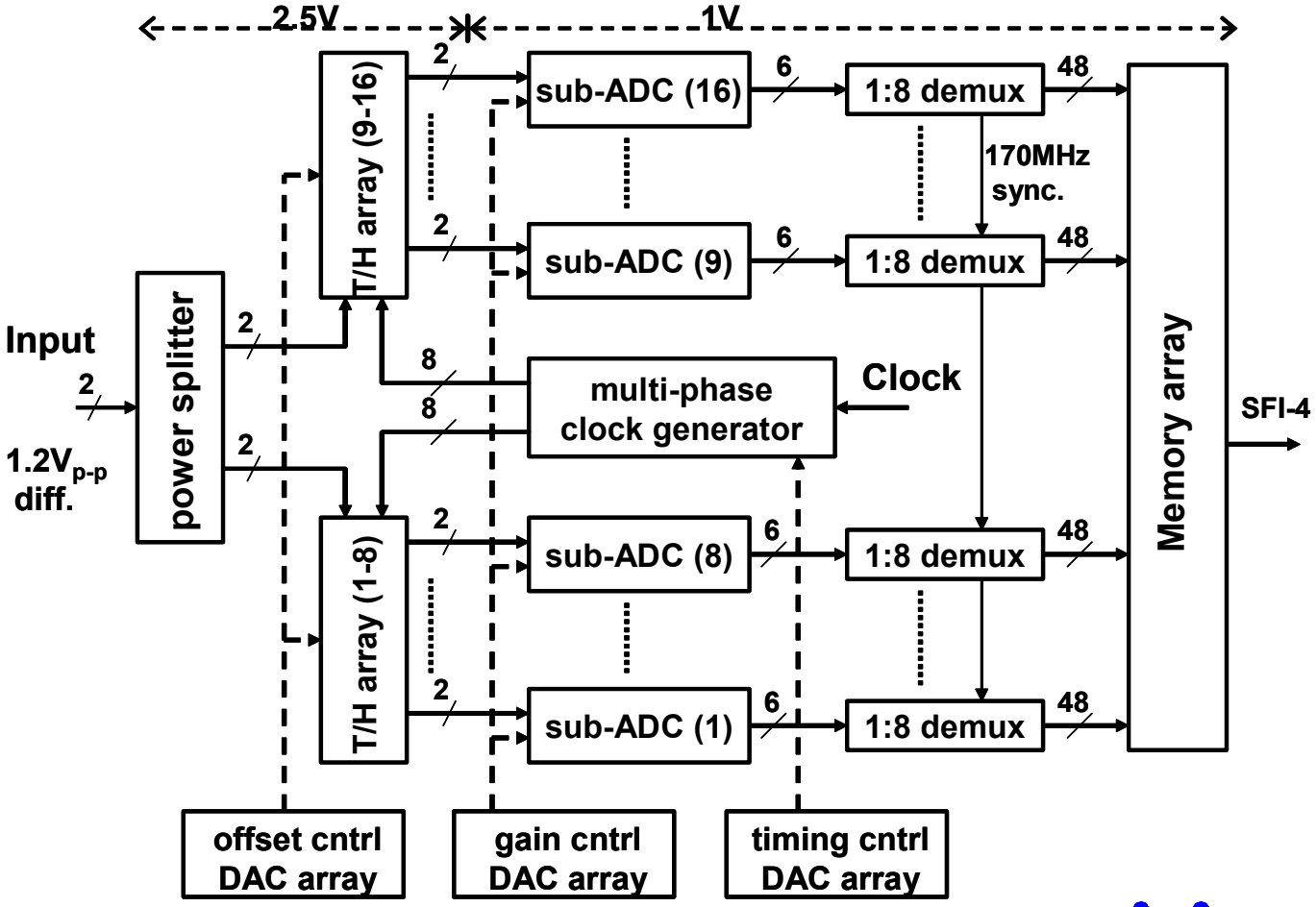
P. Schvan, et. al., "A 24GS/s 6b ADC in 90nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.544-545, Feb. 2008.

160 6b SA ADCs realize 24GS/s conversion

$$\#\ of\ ADCs = 16 \times 10 = 160$$

One ADC: 150MS/s



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Summary of performance and comparison

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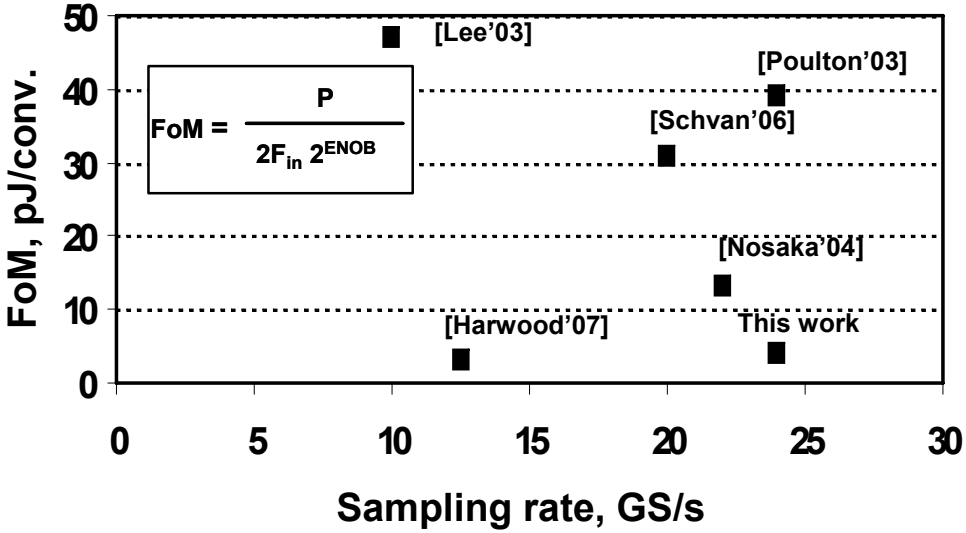
Packaged ADC performance

Resolution	6 bits
Conversion rate	0.1 - 24GS/s
Input range	$1.2V_{p\text{-}p}$ diff.
ENOB average cal / cal each freq	 4.2/4.8, F_{in}= 8GHz 3.5/4.1, F_{in}= 12GHz
SFDR	40dB @ 8GHz 35dB @ 12GHz
Power	1.2W @ 1V and 2.5V
ADC core	4 x 4 mm^2
Process	90nm CMOS

However FoM is about 3pJ/conv. (Large)



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Fight back of pipeline ADCs

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Optimization of OpAmp in Pipeline ADC

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90nm CMOS, near sub-threshold operation, and SC level-shift have realized 10bit 80MHz ADC with 0.8V operation and small power of 6.5mW

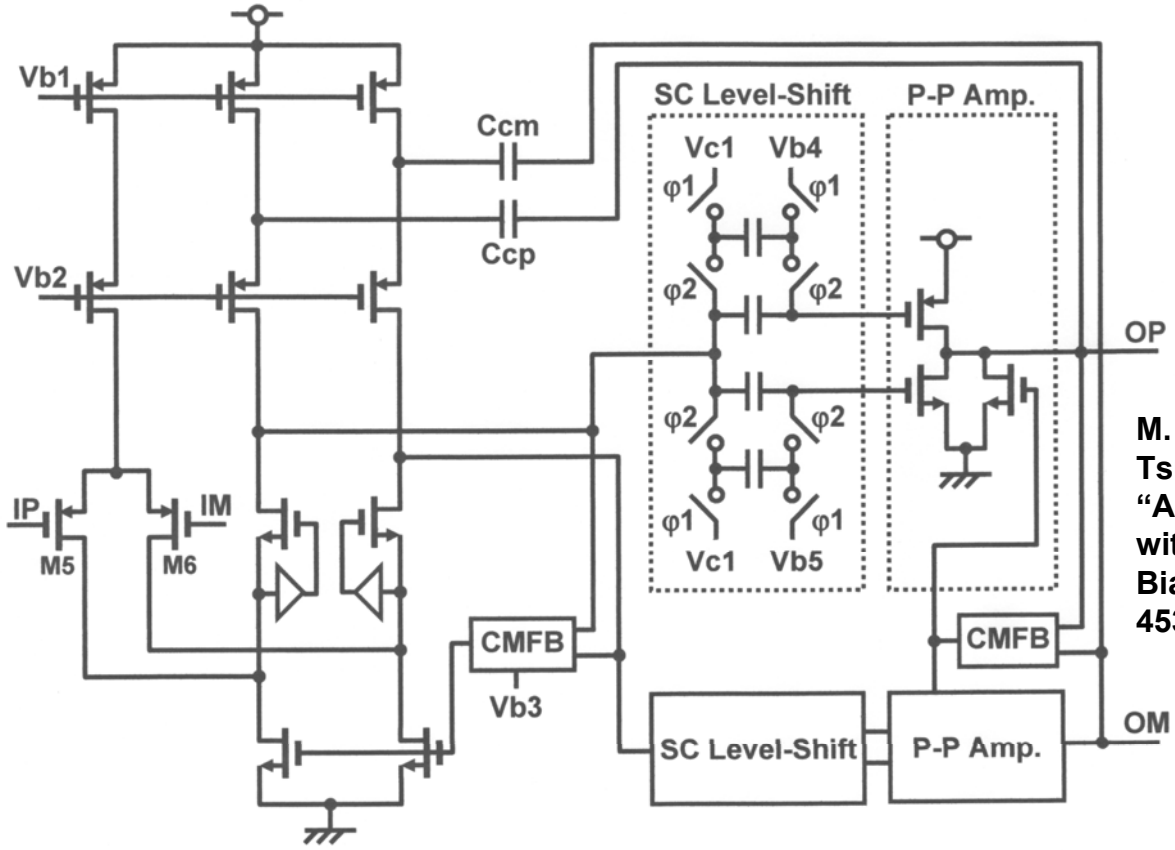

Figure 25.1.2: Schematic of two-stage amplifier.

FoM=200fJ/conv.-step

M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto
"A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing," ISSCC, Dig. Tech. paper, pp. 452-453, 2007.

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Results

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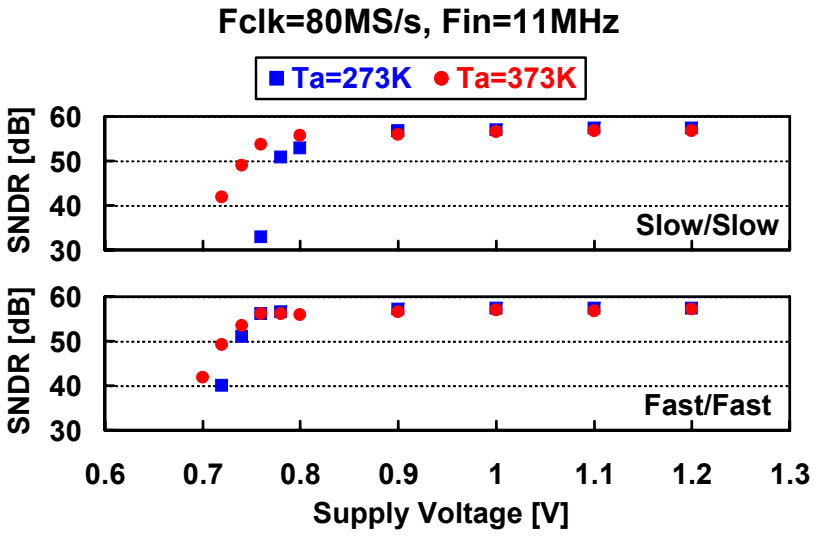
Excellent FoM has been attained in spite of pipeline ADC.

FoM=200fJ/conv.-step 0.08mW/MHz

Technology	1P10M 90nm CMOS with MIM Capacitors	
Resolution	10bit	
Conversion Rate	80MS/s	
Active Area	1.18mm x 0.54mm	
Input Range	1.2Vp-p Differential	
Supply Voltage	0.8V	1.2V
SNDR	55.0dB @2MHz 51.4dB @41MHz	56.9dB @2MHz 55.6dB @41MHz
Total Power Consumption	6.5mW	13.3mW
INL	< 1.0LSB	< 0.5LSB
DNL	< 0.8LSB	< 0.4LSB



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Process improvement of MOS transistor

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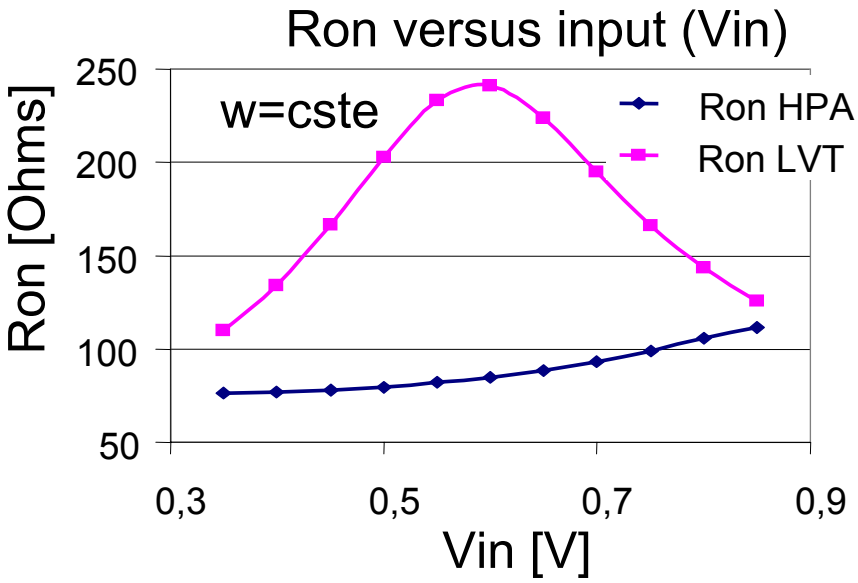
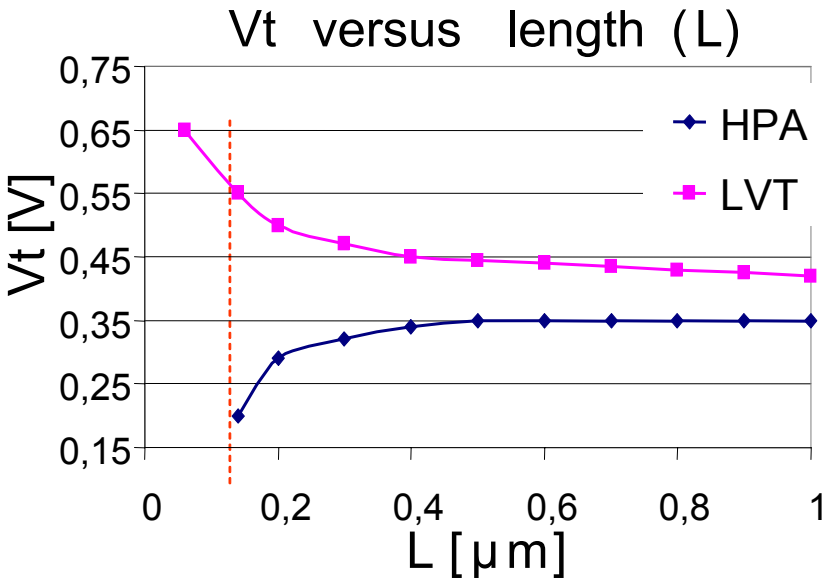
No pocket transistor with low threshold voltage transistor offers

low on-resistance for switches

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet, "A 1.2V 4.5mW 10b, 100MS/s Pipeline ADC in a 65nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.250-251, Feb. 2008.

Lmin (HPA)=0.14um





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Optimization of MOS transistor

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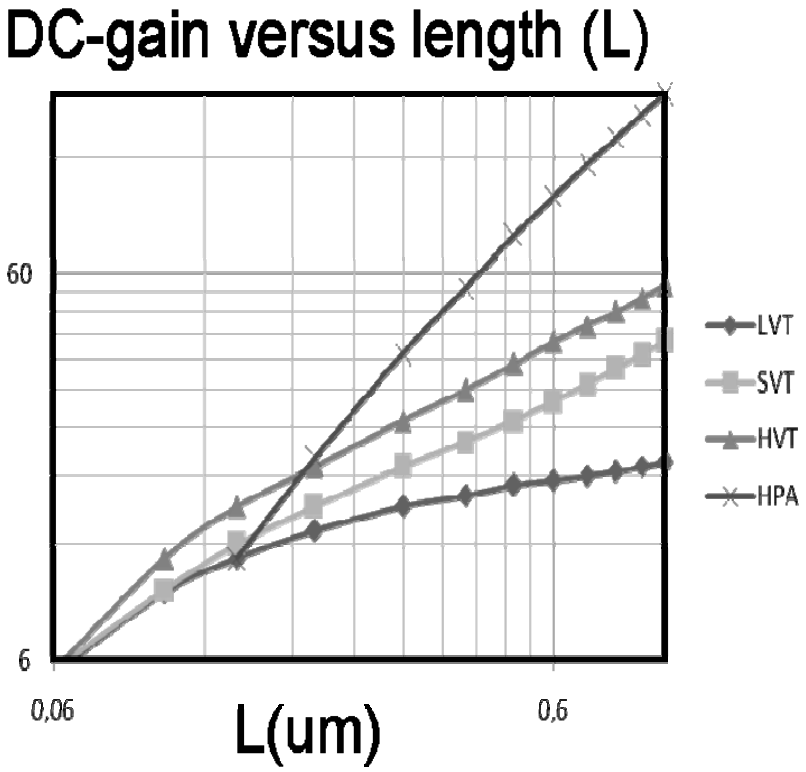
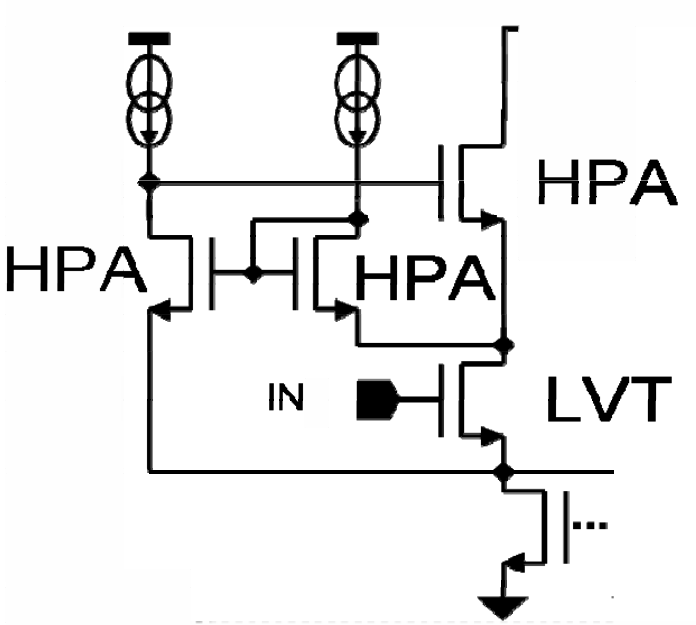
No-pocket MOS transistor can increase output resistance and results in increasing the DC gain.





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Summary of performance

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This pipeline ADC has attained excellent low FoM compared with SA ADC

Resolution	**10 bit**
Sampling speed	**100MS/s**
Input range	**1.0Vppd**
Power Consumption	**4.5mW**
SNDR	**59dB**
DNL	**+/-0.1 LSB**
INL	**+/-0.2 LSB**
Active area	**0.07mm^2**
Technology	**ST CMOS 65nm**

FoM= 62fJ/conv.-step

Tech (nm)	VDD (V)	Fs (MHz)	Power (mW)	SNDR (dB)	FOM (pj/step)	References
130	1.2	120	90	57.1	1.25	B.Hemes ISSCC-2004
90	1.2	12	3.3	52.6	0.76	R.Wang ISSCC-2005
90	1.2	100	35	56.9	0.6	G.Geelen ISSCC-2006
90	1.0	100	33	55.3	0.69	K.Honda JSSCC-2007
90	0.8	80	6.5	55	0.17	M.Yoshioka ISSCC-2007
65	1.2	100	4.5	59	0.062	This work

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Our original work

What determines FoM

OpAmp based design vs. comparator based design

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OpAmp based vs. comparator based

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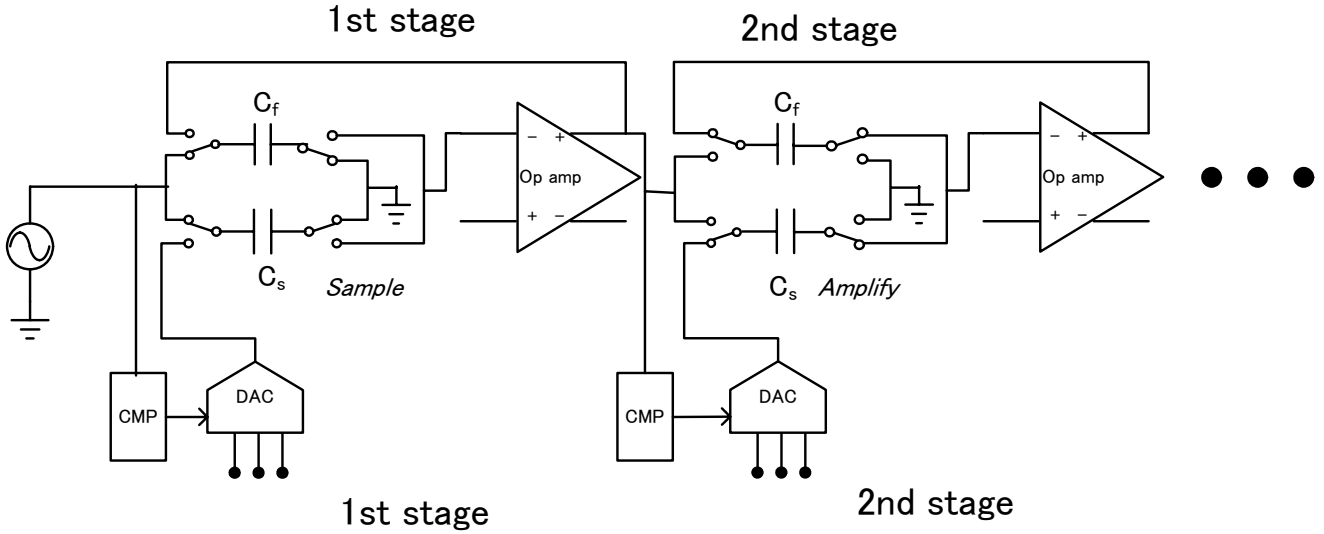
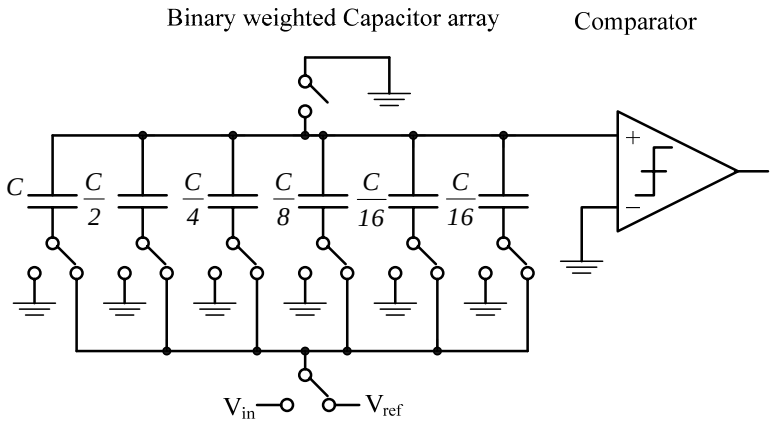
Pipelined ADC

Opamp base



SA ADC

Comparator base



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Noise of OpAmp

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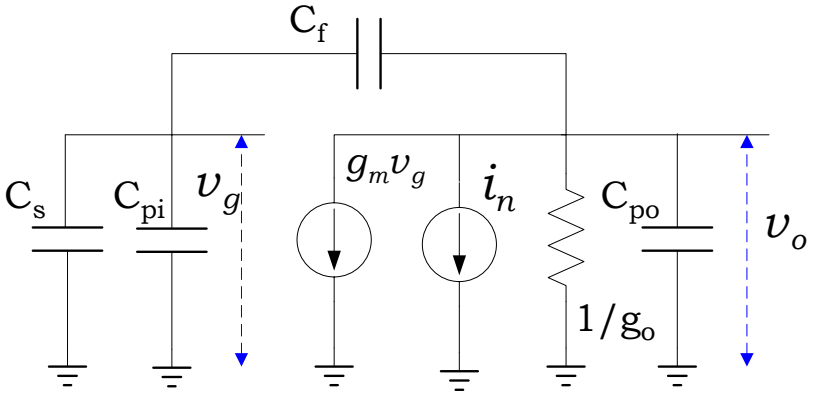
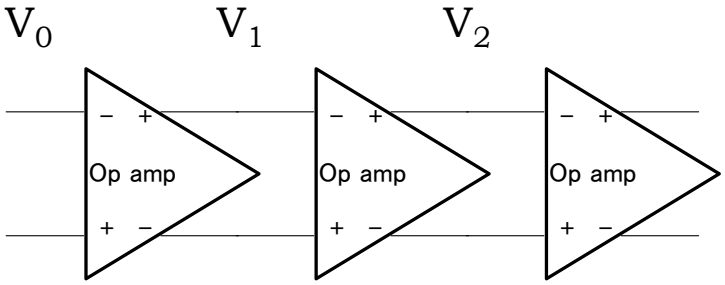
Amplification phase





$$v_{no}^2 = \int_0^\infty \frac{i_n^2}{(g_m\beta)^2 + (\omega C_L)^2} df = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f}$$

$$v_{no}^2 = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f} \qquad C_f = C_s = C_o$$

$$V_0: \quad v_{no}^2 \approx \frac{kT}{C}$$

$$V_1: \quad v_{n1}^2 = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C}$$

$$V_2: \quad v_{n2}^2 = 2 v_{n1}^2$$

$$\beta \rightarrow \beta \qquad C_L \rightarrow \frac{C_L}{2}$$

$$v_{ni}^2 = 2 \cdot v_{ni-1}^2$$

n=2: Cascode
n=3: Folded Cascode

$$v_{nt}^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1} \left(\frac{1}{2^2}\right)^i \cdot v_i^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1} \frac{2^i}{2^{2i}} \cdot v_1^2 \approx 2\frac{kT}{C_o} + \frac{\gamma n kT}{\beta C_L}$$

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FoM calculation

OpAmp consumes power, however operating frequency is just f_c and total power is only 2.5x of 1st OpAmp.

$$v_{nt}^2 = 2\frac{kT}{C_0} + \frac{\gamma nkT}{\beta C_L} \approx \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_0}$$

$$V_{qn}^2 = \frac{1}{3}\left(\frac{q}{2}\right)^2 = \frac{1}{3}\left(\frac{V_{dd} - 2V_{eff}}{2^N}\right)^2 \quad if \quad V_{nt}^2 = V_{qn}^2 \quad \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_o} < V_{qn}^2$$

$$C_0 > \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{V_{qn}^2}$$

$$f_{close} > \frac{Nf_c}{3} \quad \therefore \frac{g_m \beta}{2\pi C_L} > \frac{Nf_c}{3} \therefore g_m > Nf_c \frac{2\pi}{3\beta} C_o \quad g_m \approx \frac{2I_{ds}}{V_{eff}}, \quad I_{ds} > Nf_c \frac{2\pi}{3\beta}\frac{V_{eff}}{2} C_o$$

$$P_d \approx 2.5 \times (2 \times 2 \times I_{ds} \times V_{dd}) = 10 I_{ds} V_{dd}$$

$$FoM = \frac{P_d}{f_c \times 2^{N-0.5}}$$

Estimated FoM for pipeline ADCs

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We are reaching the theoretical limit of FoM

$V_{dd} = 1.0(V)$
$V_{eff} = 0.15(V)$
$kT = 4.1 \times 10^{-21}$
$\gamma = 2$
$n = 2$
$\beta = \frac{1}{3}$
$f_c = 100MHz$

Analog portion only

Resolution	10	12	14
C_o(pF)	0.37	6.0	95
I_{dd}(mA)	1.75	33.6	628
P_d (mW)	1.75	33.6	628
FoM(fJ)	24	116	542

Recent ADC

$V_{dd} = 1.2(V)$
$V_{pp} = 1.0V$
$f_c = 100MHz$
$C_o = 0.4pF$
$P_d = 4.5mW$
$SNDR = 59dB$
$FoM = 62fJ$

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet, "A 1.2V 4.5mW 10b, 100MS/s Pipeline ADC in a 65nm CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.250-251, Feb. 2008.

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SA ADC

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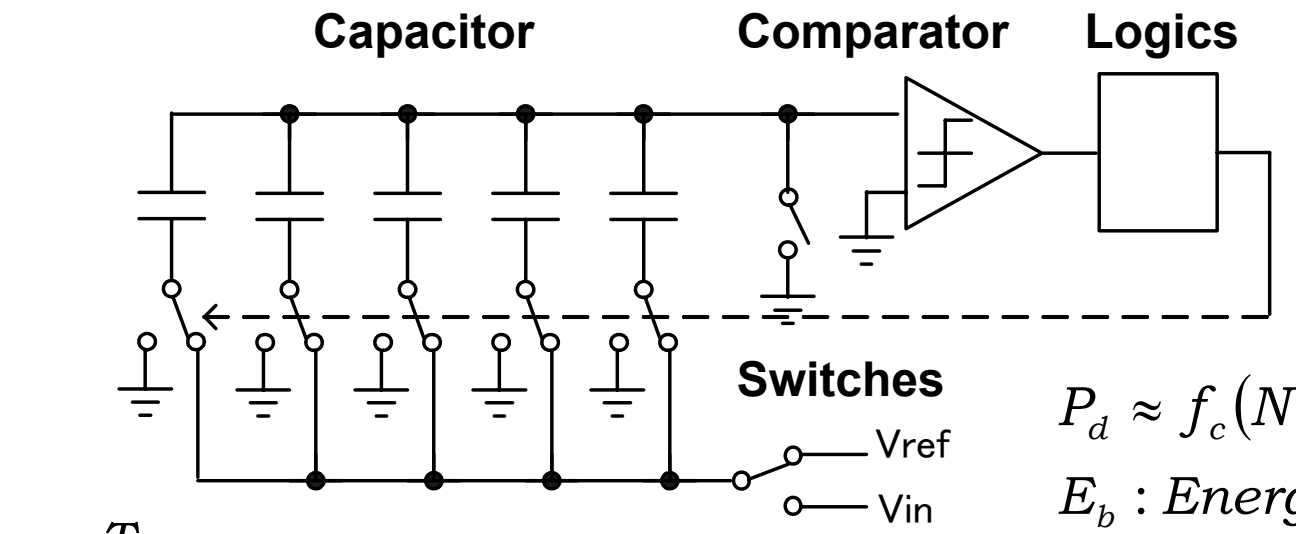
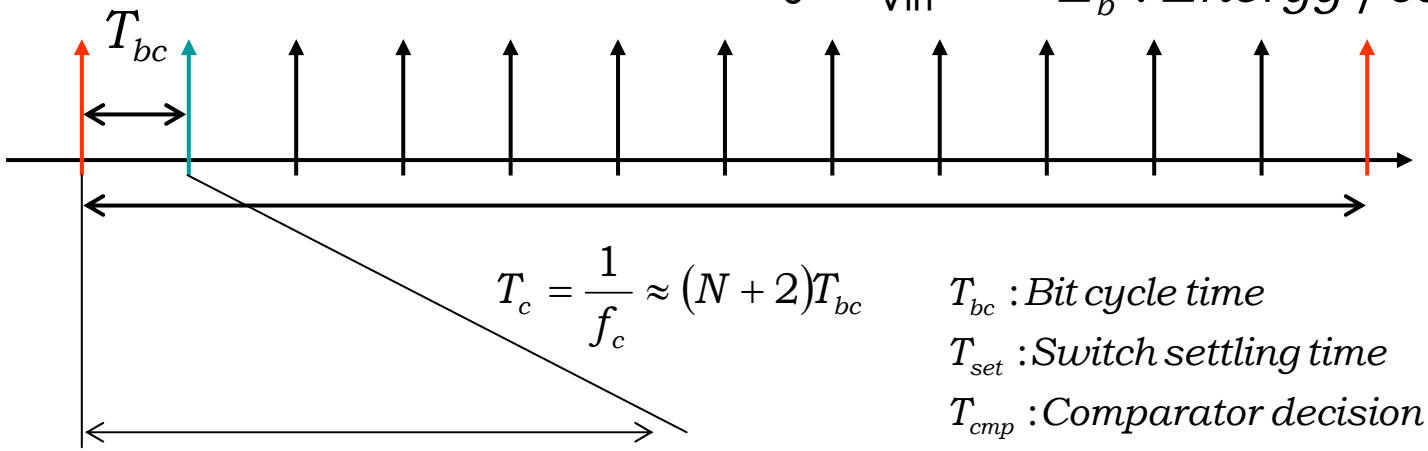
SA ADC needs high speed switches, comparators, and logics.



$$P_d \approx f_c(N+2)E_b$$

$$E_b : Energy / conv$$



$$T_c = \frac{1}{f_c} \approx (N+2)T_{bc}$$

$$T_{bc} = T_{set} + T_{cmp} + T_{dig}$$

T_{bc} : *Bit cycle time*

T_{set} : *Switch settling time*

T_{cmp} : *Comparator decision time*

T_{dig} : *Logic delay time*

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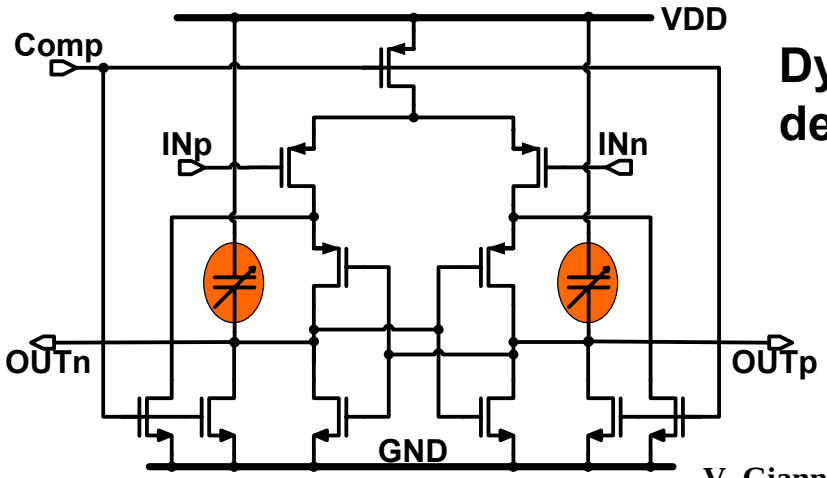
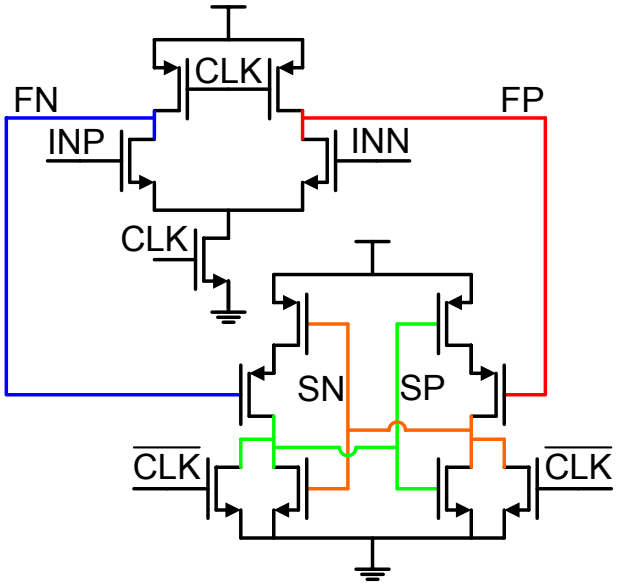
Comparators

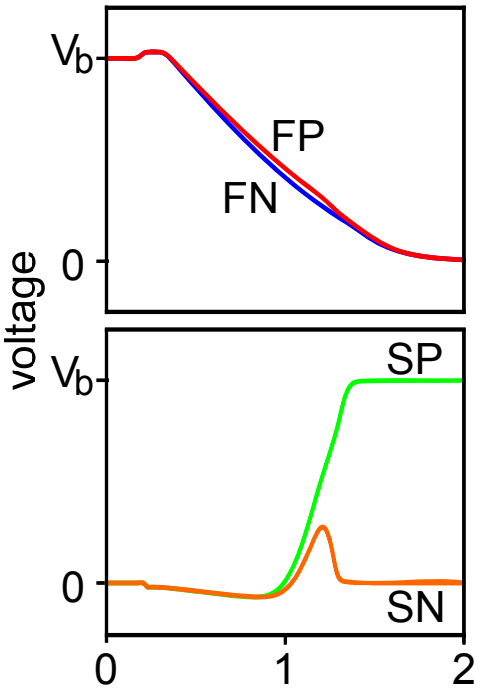
Dynamic comparators are widely used for not only SA ADCs but also Flash ADCs





Dynamic comparators use the fast voltage fall depended on input voltage difference

Fast voltage fall



V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Issue of comparator for SA ADCs

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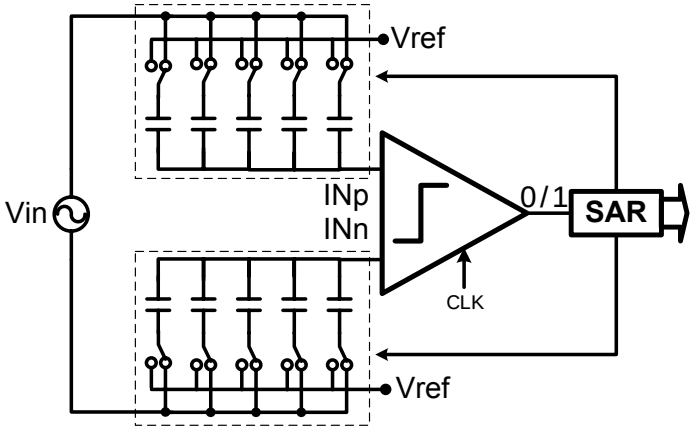
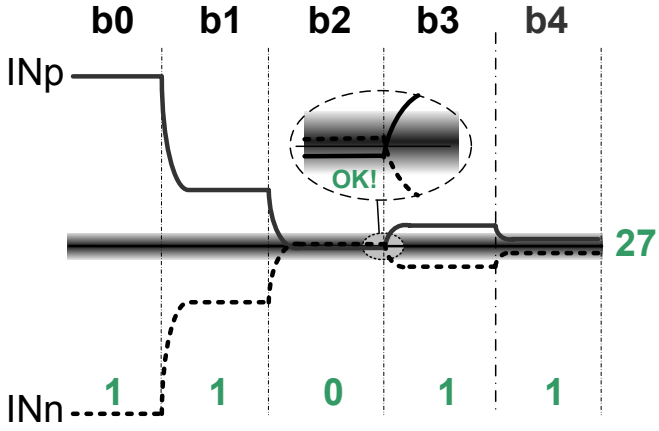
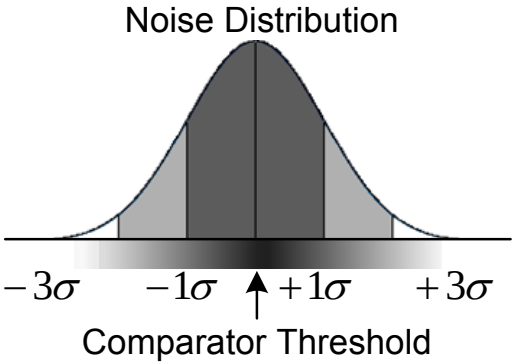
A comparator has noise and this results in conversion error.

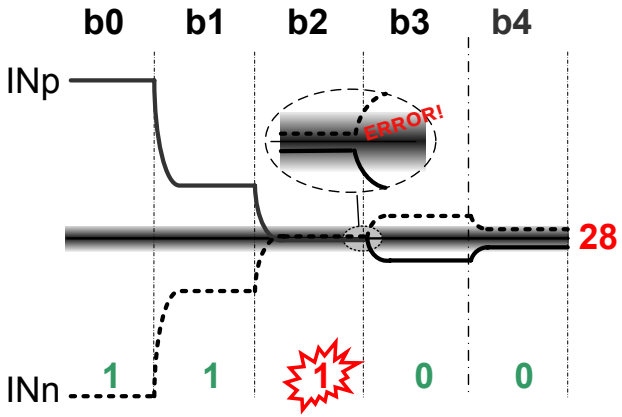
V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

5b Charge Redistribution (CR) SAR ADC









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Comparator noise and ENOB

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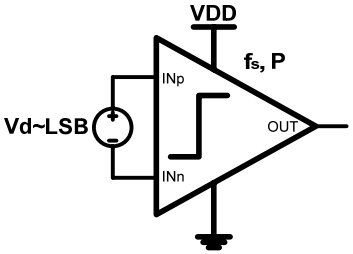
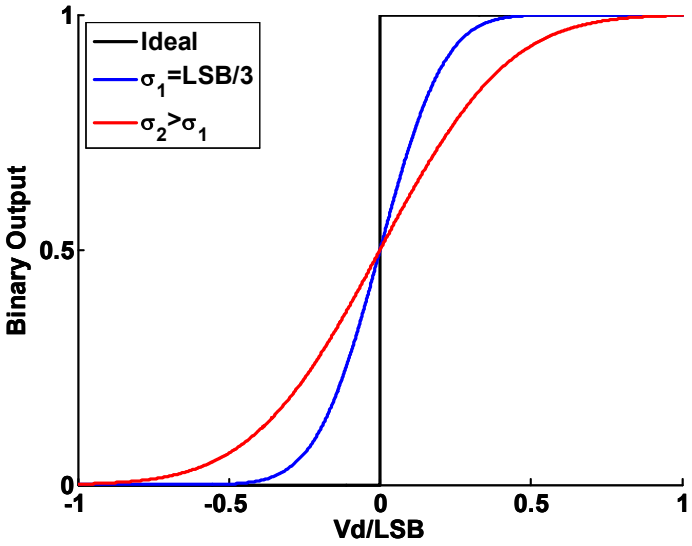
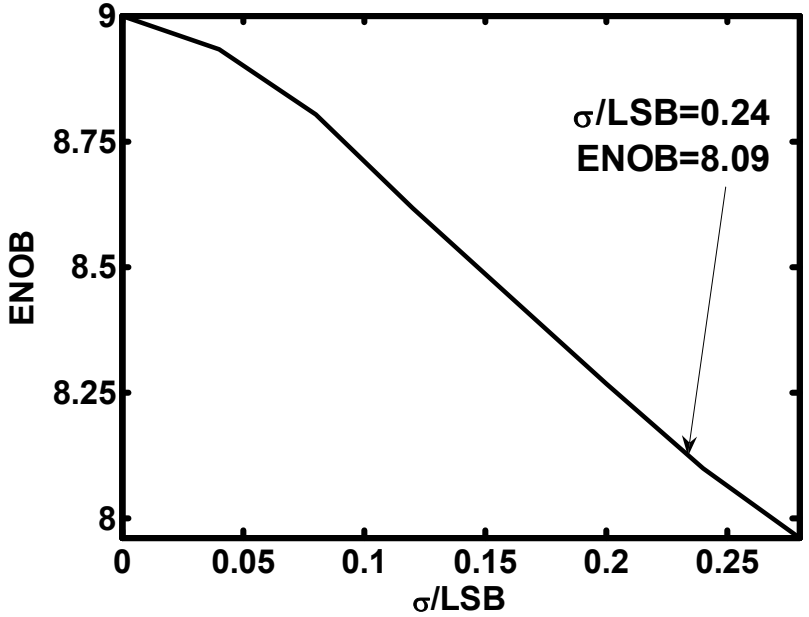
Low comparator noise is required for SA ADC



$$\sigma_V < 0.25LSB : -1bit\,\deg rade$$

$$\sigma_V < 0.15LSB : -0.5bit\,\deg rade$$





V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

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Expected FoMs for comparators

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FoM due to comparator is not negligibly small. Operating frequency is (N+2)f_c and power increases with N. Recent SA ADCs are reaching the limit.

$$p_d = 2(N+2) f_c C_L V_{dd}^2$$

$$FoM = \frac{p_d}{f_c \times 2^{N-0.5}}$$

$$C_L > 4 \times 10^{-20} \times 2^{2N}$$

f_c=100MS/s

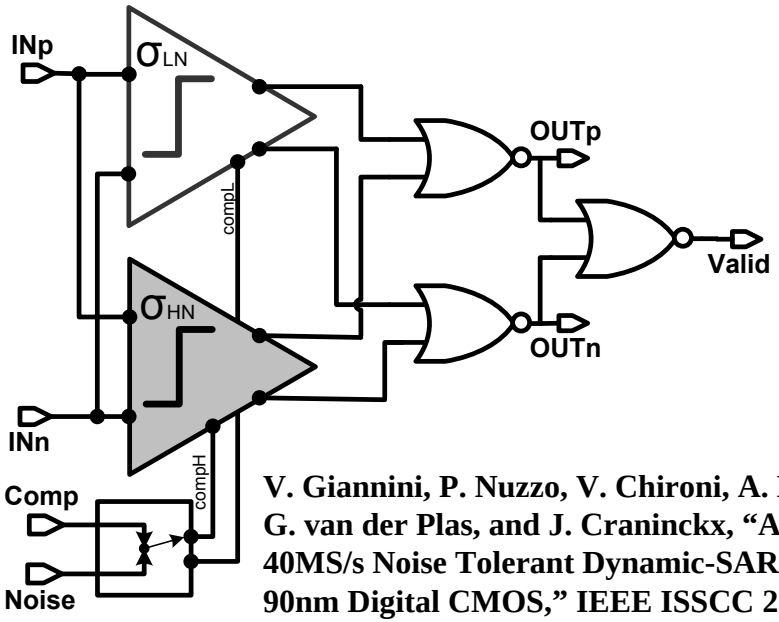
$$\gamma = 1, V_{dd} = 1.0V, V_{eff} = 0.2V$$

Resolution	10	12	14
C_L(fF)	42	670	11000
P_d(mW)	0.1	1.9	34
FoM(fJ)	1.4	6.5	30

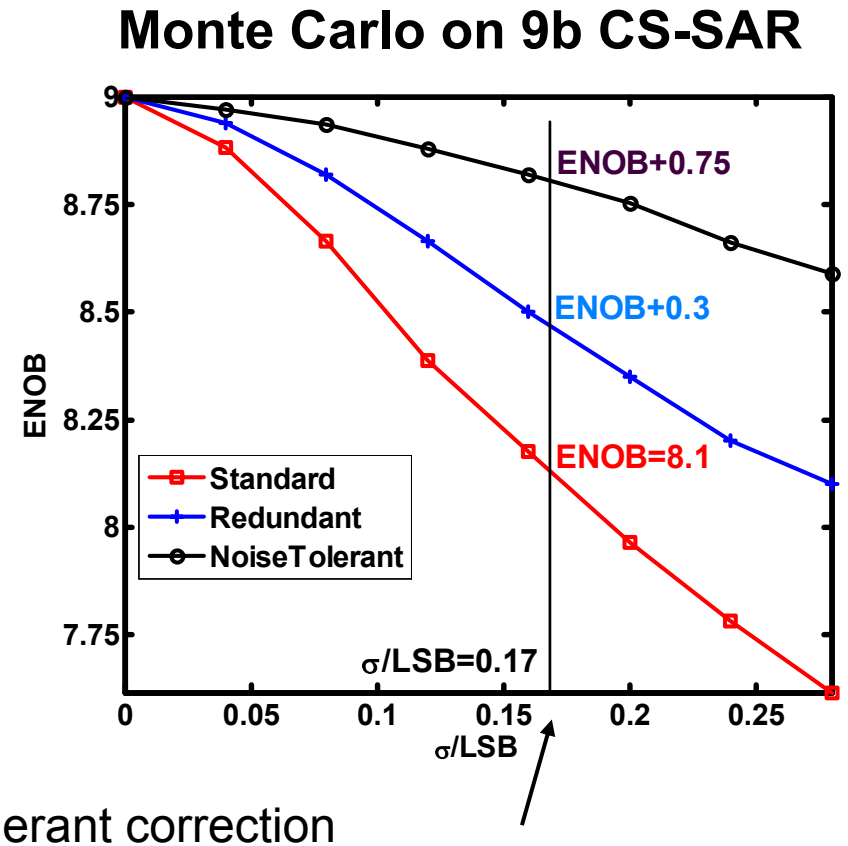
M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Redundant architecture

Combination of Large and small comparators and one redundant conversion increase ADC performance without serious FoM degradation.



V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.



- Comparators are sized so that

  σ HN ~1/6 LSB and σ LN ~1/12 LSB

- Good ENOB improvement with Noise Tolerant correction

Technology trend of ADCs

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SA ADCs become major, but….

Architecture	Flash	Two-step parallel	Pipeline	SA
Period	78---88---	88 --- 95--	95-- 1x--	06--
Technology	Bipolar/CMOS	Bi-CMOS, CMOS	CMOS	CMOS
Parallel/Serial	Parallel	Two-step, Semi-parallel	Serial (Pipeline)	Serial
Base	Comparator	Comparator	Amplifier	Comparator
Gain	No	No (Yes Interpolation)	Yes	No
Sampling	No	Yes	Yes	Yes
Accuracy	Transistor mismatch	Comparator mismatch Comparator noise Settling	Capacitor mismatch Amplifier gain OpAmp noise Settling	Capacitor mismatch Comparator noise
Speed	Device fT	Reference+Switch Comparator+Logic	OpAmp GBW Switch	Comparator+Logic Switch
Design technique	Interpolation Averaging Folding Dynamic comparator	Redundancy Interpolation Averaging Gain boost Dynamic comparator	Redundancy (1.5b) Gain boost OpAmp sharing Calibration	Serial Capacitor Dynamic comparator Interleaving Calibration

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Summary

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- **Pipelined ADCs, current major ADC architecture are now facing serious issues;**
  - **Low OpAmp gain**
  - **Low voltage operation→ larger capacitance**
  - **Scaled device is not suitable for higher resolution**

- **SA ADCs becomes attractive and looks suitable for scaled CMOS**
  - **Extremely Low FoM**
  - **Simple; needs only capacitors, switches, comparators, and logics.**
  - **Free from OpAmp issues**

- **Pipelined ADCs have fight backed**
  - **Same FoM as SA ADC, owing to process improvement**

- **What determines FoM and which is better.**
  - **Pipeline: OpAmp SA ADC: Comparator**
  - **SA is better in FoM, however the difference is not large.**
  - **Attention to the sensitivity of comparator for SA ADC design**