# High speed ADCs: History and future

## along with my life

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NTU A. Matsuzawa

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*Pursuing Excellence*

- **History of high speed ADCs along with my life**

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**Matsuzawa & Okada Lab.**

# History of high speed ADCs along with my life

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# Start to develop ADCs

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I joined Matsushita electric in 1978 after graduate from MS of Tohoku Univ.
In 1979, I started to develop video-rate ADCs in Central research Lab.

In 1979, Panasonic released the monumental VTR that realized world first long
play (2H → 6H) recording and became world top video supplier.

**10B$/year !!**

This product must be the treasure of analog technology .

Panasonic
=Matsushita Electric



1979, in front of Central research Lab.



Panasonic VHS Video NV-6000, 1979

Matsuzawa
& Okada Lab.

**At that time,**
**Panasonic already started the development of digital video & TV systems.**

**Network, Communication**
**Storage media systems**

| Analog Processing | Data Converter | Communication processing | Data compression |
|---|---|---|---|

**Analog technology**
- ·RF
- ·Optical I/F
- ·Cable drive
- ·Signal Generation
- ·A/D Converter
- ·D/A Converter

**Digital technology**
- ·Mod/ Demod
- ·Channel select
- ·Error correction
- ·Protocol
- ·Encryption
- ·MPEG2, 4
- ·DSP
- ·Codec

# Video ADC board at 1980

**A video rate ADC is the serious bottle neck for the digital consumer products.**

**My mission was to develop ADCs of which cost and power are low enough for consumer use.**

**10bit 14.3MHz ADC $10,000, Pd=20W !!**
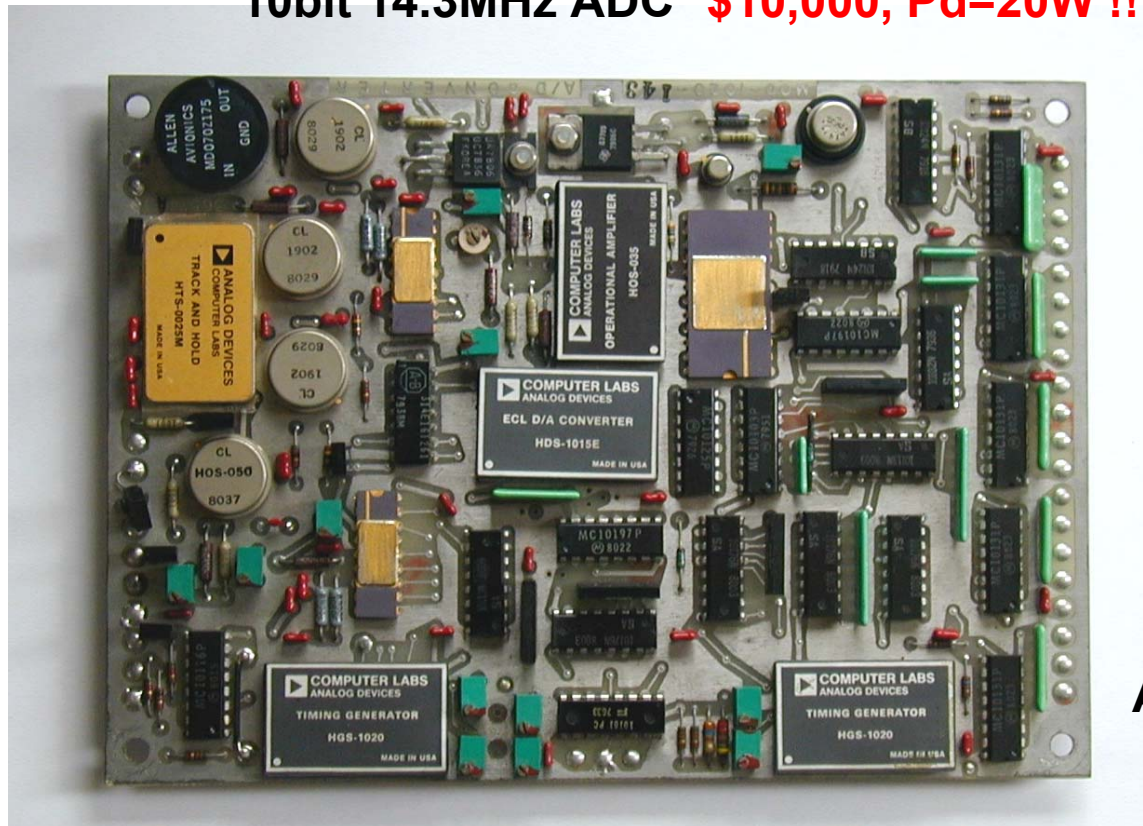


**Analog Devices Inc.**

**I developed many ADCs to realize new digital consumer products**
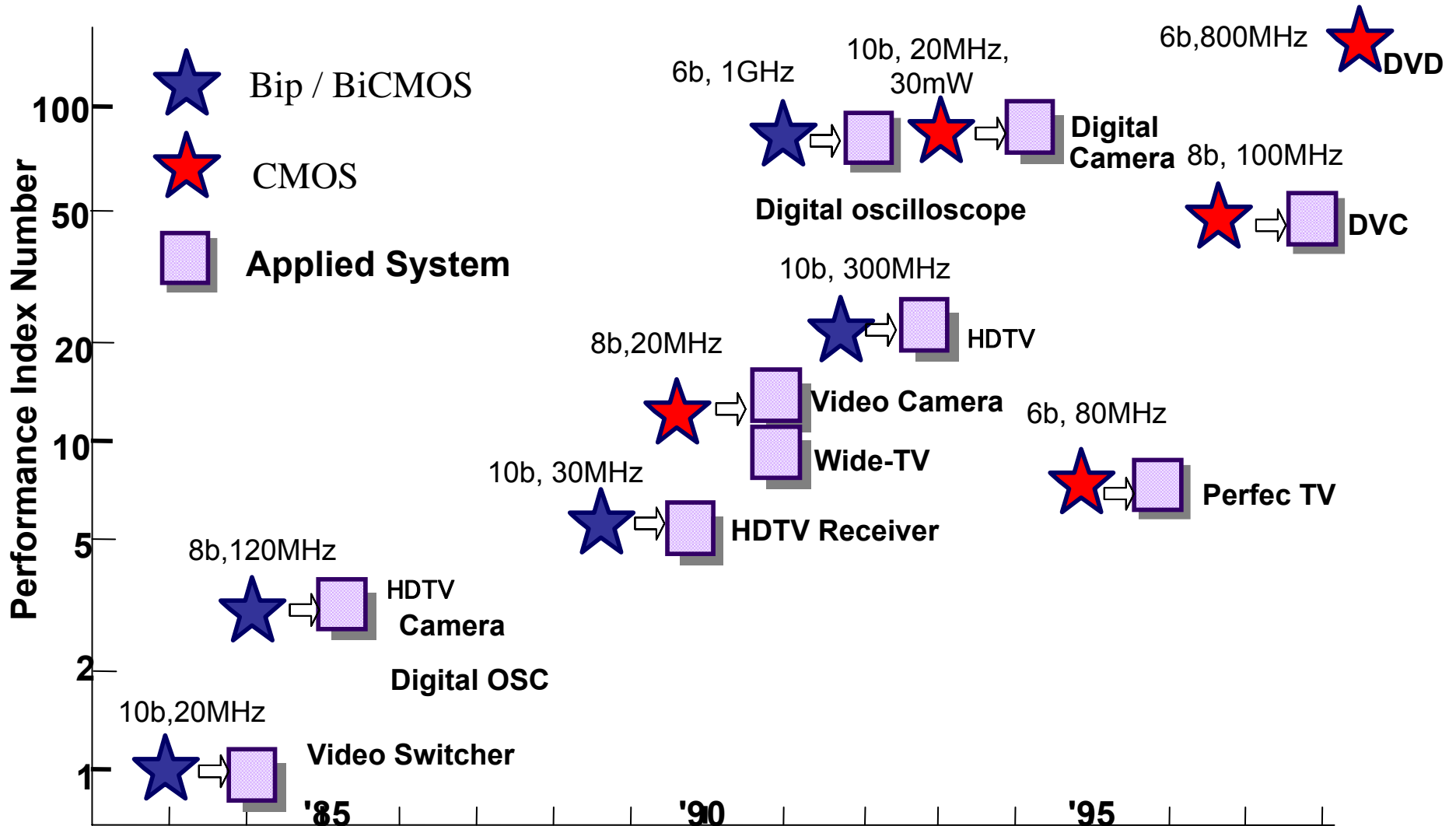
# Japan first video-rate 8b ADC

**I succeeded to develop Japan first video-rate 8b ADC, in spite of my first work.**



**My first IC design      At 1981**

**Bipolar (3um)**
**8b, 30MS/s, 0.7W**
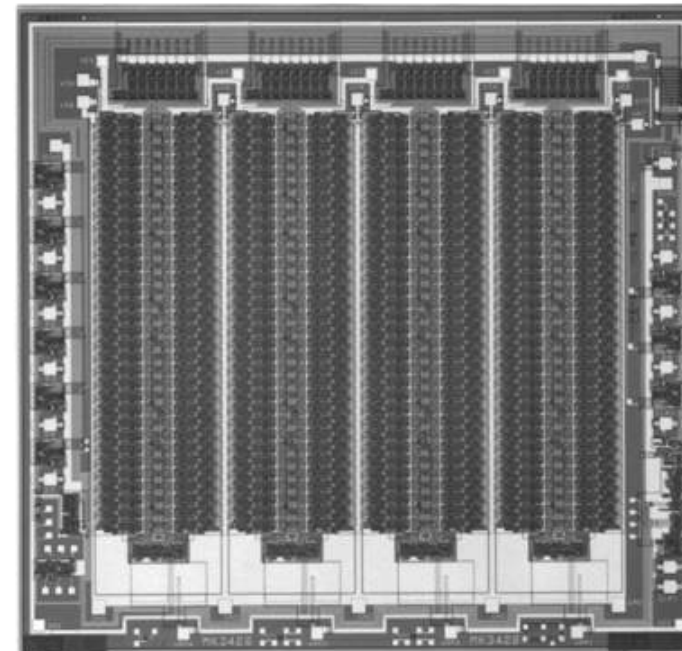
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# World first monolithic Video-rate 10b ADC

**Only way to realize 10b video-rate ADC was to use high precision bipolar and array of comparators → Flash ADC**

Bipolar (3um)
10b, 20MS/s, 2W
$ 800

**This ADC contributed to**   T. Takemoto and A. Matsuzawa, JSC, pp.1133-1138, 1982.

**Realization of world first HDTV world first digital TV studio**

IR100 Award

日経エレクトロニクス
NIKKEI ELECTRONICS
プログラム自動生成ツールの動向
電磁妨害の少ないプリント基板設計
高速ディスク・コントローラLSi

民生用のバイポーラICを最小寸法3μmで製造する
バイポーラ・プロセス技術

V_DD  $v_{in}$  Φ

R/2
R
R
R
R
R
R
R
R/2

Comparator

Encoder

Digital out

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**Matsuzawa & Okada Lab.**
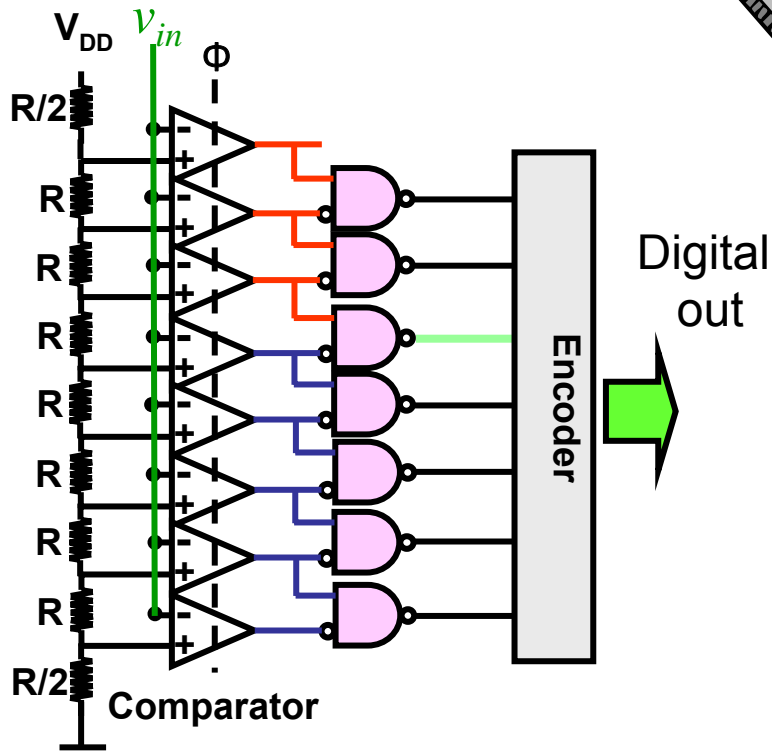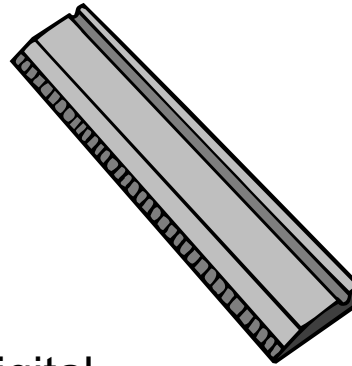
# Issue of flash ADC

**Rapid increase of power dissipation** $P_d, Area \propto 2^N$

**Tough requirement for mismatch, 0.1mV → Low yield**
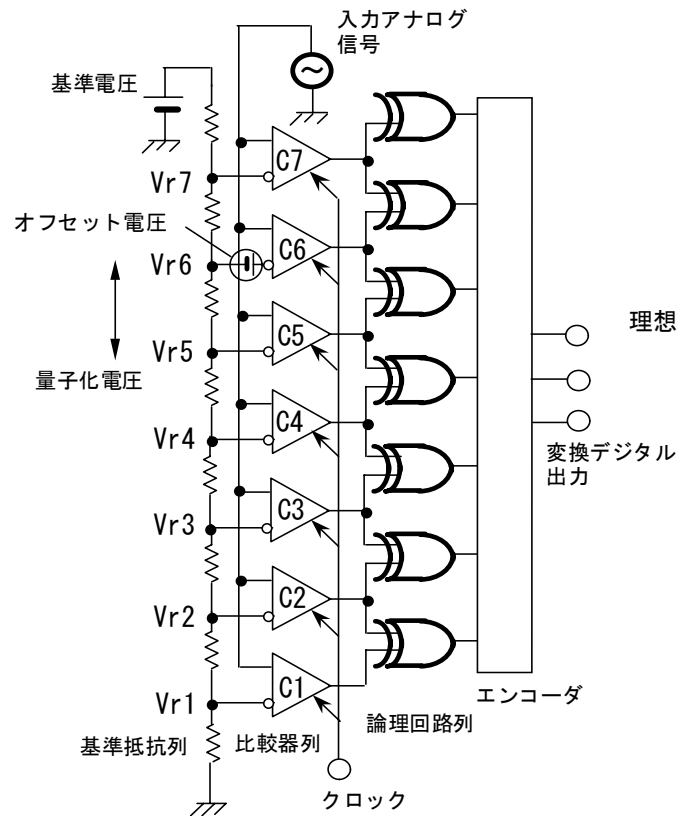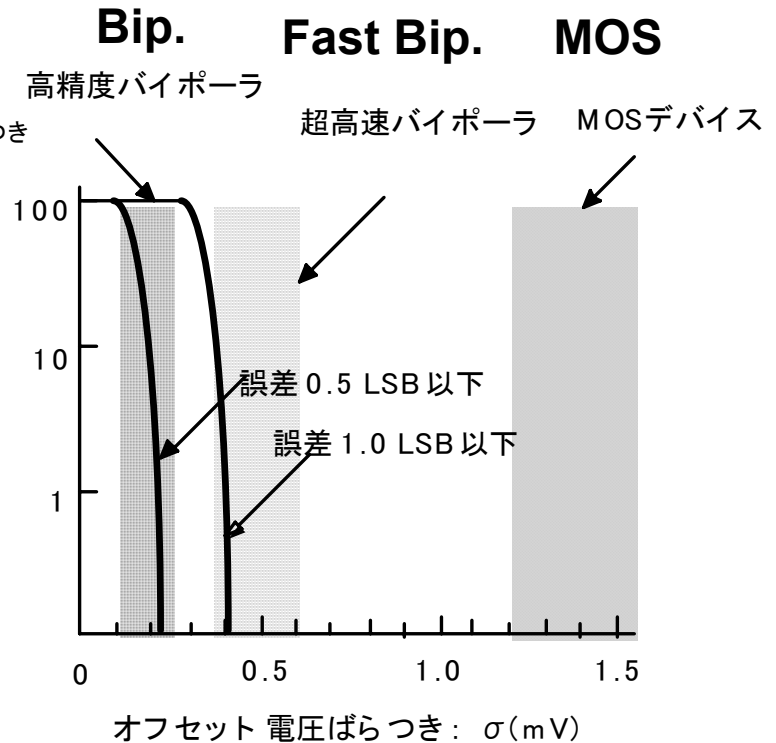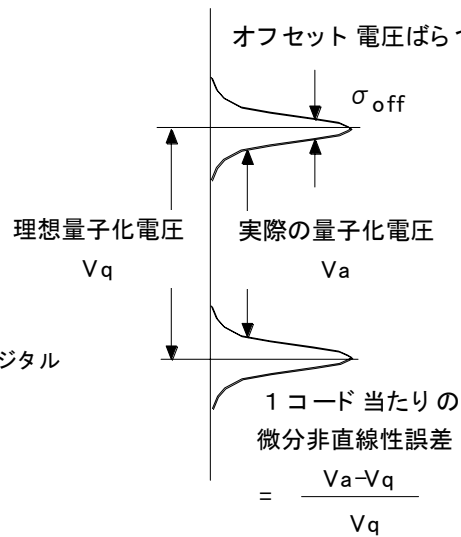
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**We developed ADC suitable for commercial HDTV receivers.**

**Two step parallel with interpolation**

A.   Matsuzawa ISSCC 1990.
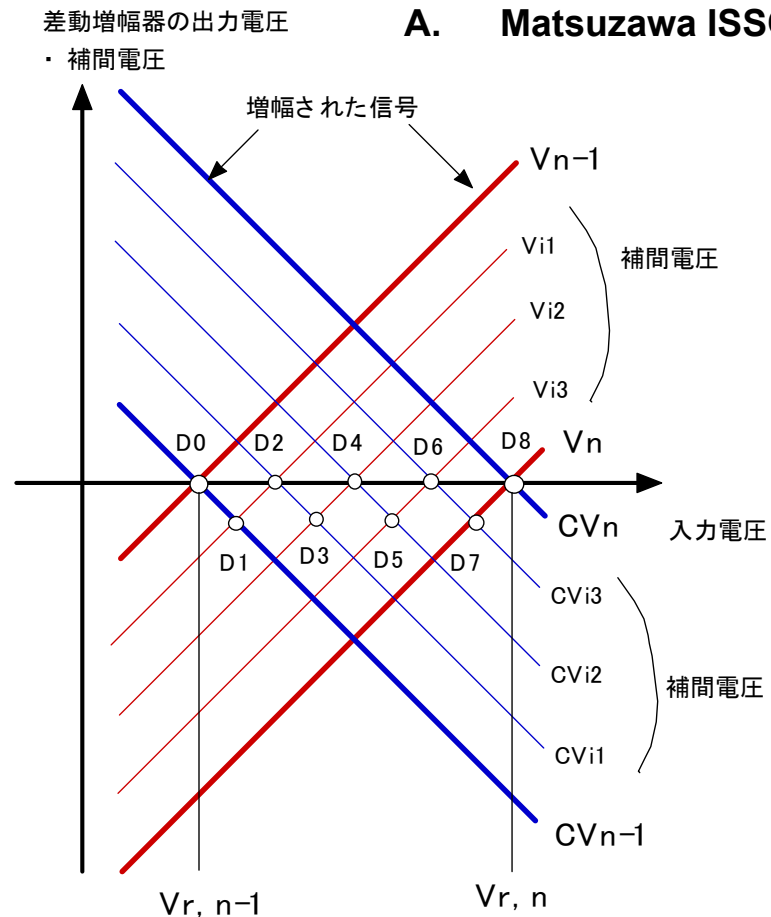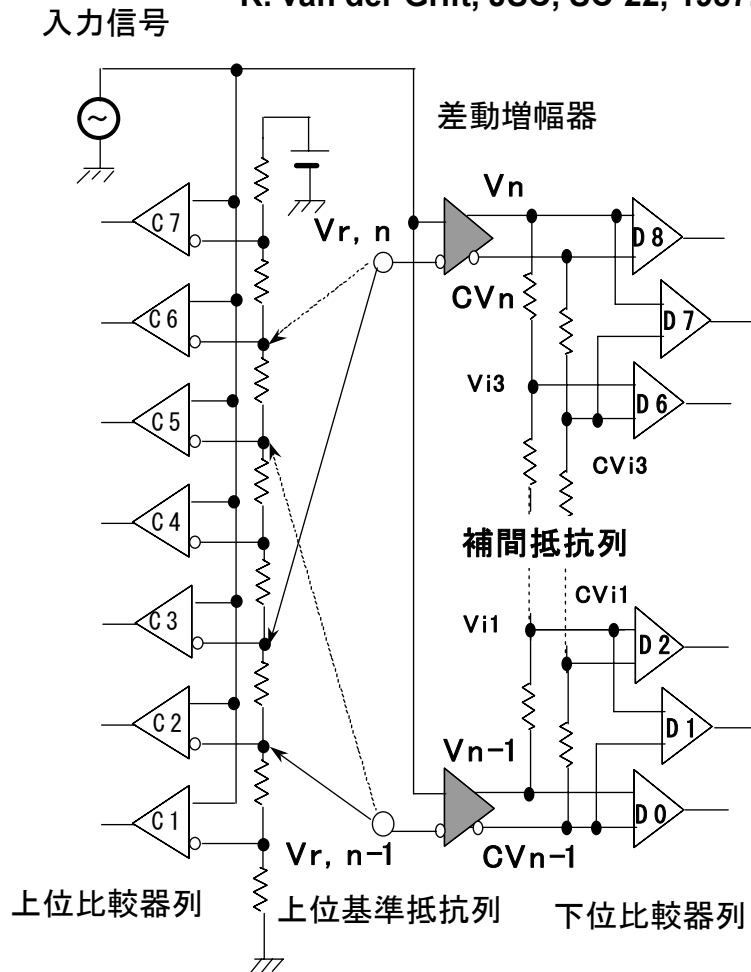
**Bi-CMOS**
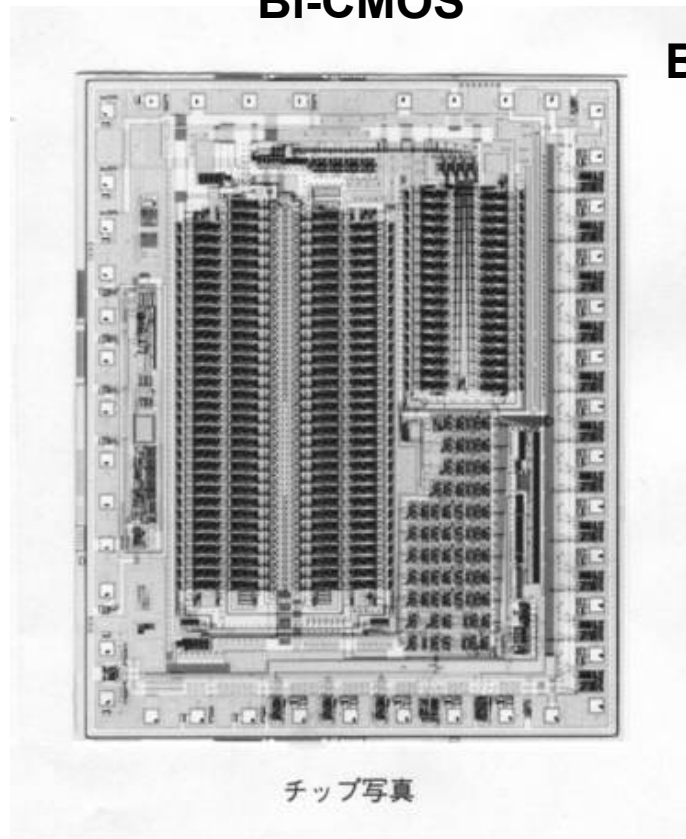
**Board for world first commercial HDTV receiver**



チップ写真



AN8130K

NTU A. Matsuzawa

Matsuzawa
& Okada Lab.

## Compare interpolated amplified signals by resistor ladder

### Philips group is another inventor

R. van der Grift, JSC, SC-22, 1987.

### Remarkable invention award in 1994

A. Matsuzawa ISSCC 1990.

入力信号

差動増幅器

$V_n$

$V_r, n$

C7

D8

$CV_n$

C6

D7

$V_{i3}$

D6

C5

$CV_{i3}$

補間抵抗列

C4

$V_{i1}$

$CV_{i1}$

C3

D2

$V_{n-1}$

C2

D1

D0

C1

$V_r, n-1$

$CV_{n-1}$

上位比較器列　　　上位基準抵抗列　　　下位比較器列

差動増幅器の出力電圧
・補間電圧

増幅された信号

$V_{n-1}$

$V_{i1}$

補間電圧

$V_{i2}$

$V_{i3}$

D0 D2 D4 D6 D8 $V_n$

$CV_n$ 入力電圧

D1 D3 D5 D7

$CV_{i3}$

$CV_{i2}$

補間電圧

$CV_{i1}$

$CV_{n-1}$

$V_r, n-1$ $V_r, n$

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# Effect of the interpolation method

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**Equivalent $V_q$ is G times larger → relax mismatch**

**Effect of offset of amplifier to DNL can be reduced by m: # of interpolation**

**High production yield**

$$\sigma_{off}^2 = \left(\frac{\sigma_{diff}}{m}\right)^2 + \left(\frac{\sigma_{comp}}{G}\right)^2$$
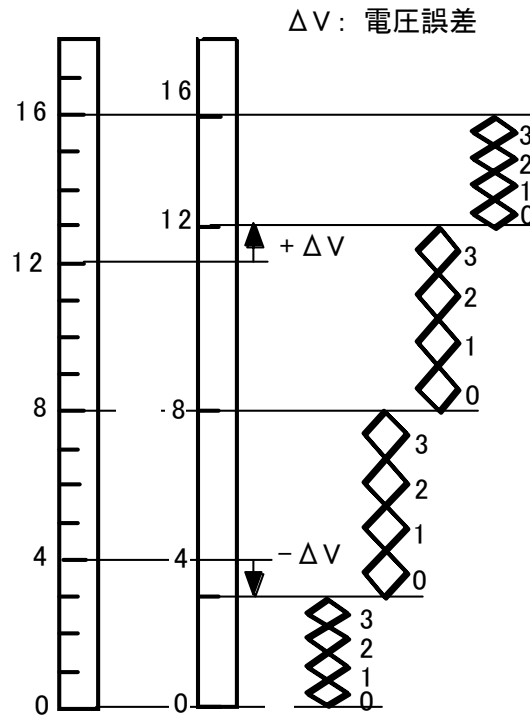
ΔV：電圧誤差

**Smooth conversion
Even if large offset** も

理想直線

入力電圧

（a）A／D変換動作                                （b）A／D変換特性

2008.04.24                              NTU A. Matsuzawa
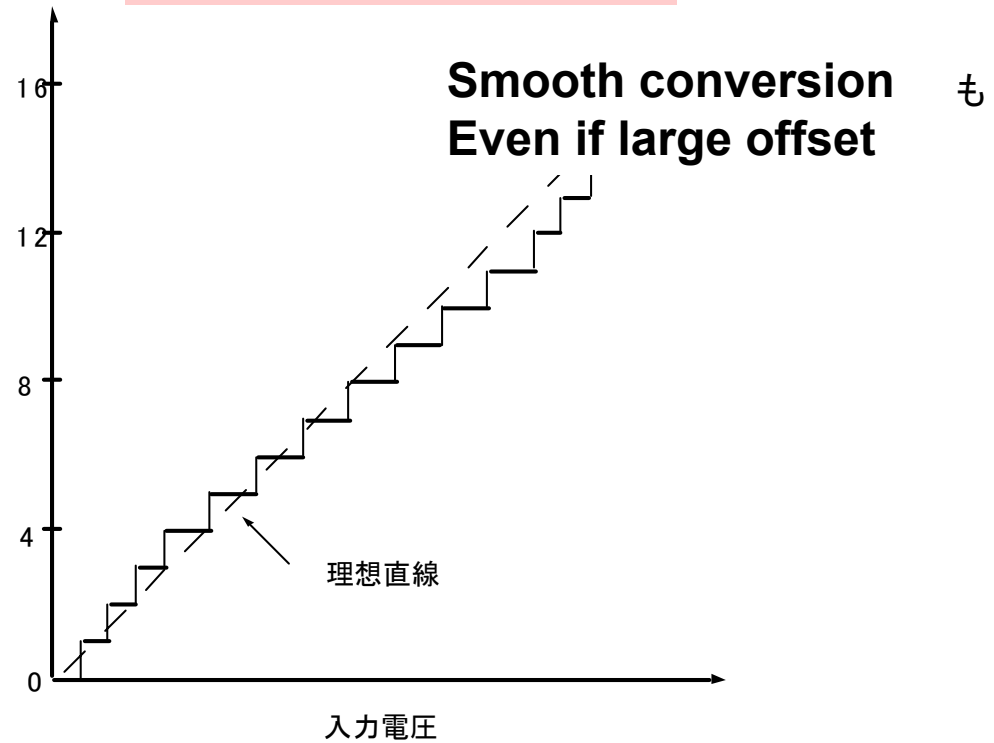
Matsuzawa
& Okada Lab.

# Ultra-high speed ADCs
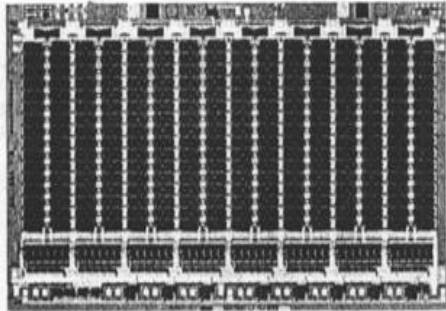
**Ultra-high speed ADCs have been developed.**

**8b, 120MHz, (1984）**   M. Inoue and A. Matsuzawa, ISSCC 1984
                                      JSC. SC-19, 1984

**World fastest 8b ADC**

**Contributed to the realization of HDTV camera and Digital oscilloscope**
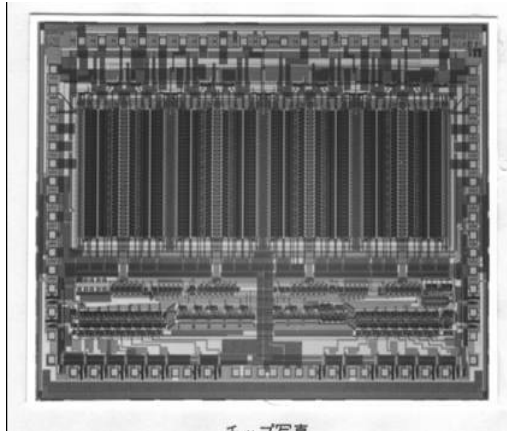
**8b, 600MHz ADC (1991）**

**World fastest 8b ADC**   A. Matsuzawa, VLSI symposia 1991
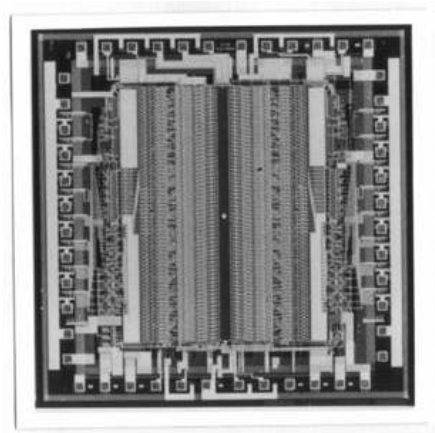
A. Matsuzawa, ISSCC 1991

**6b, 1GHz ADC (1991）**

**World fastest in production
(Dual Parallel method）**

**Contributed to Digital oscilloscope**

2008.04.24                NTU A. Matsuzawa

# Digital Oscilloscope

**Ultra-high speed ADCs realized Digital Oscilloscopes.**

**Yokogawa Electric   8b 1GHz (1994）**
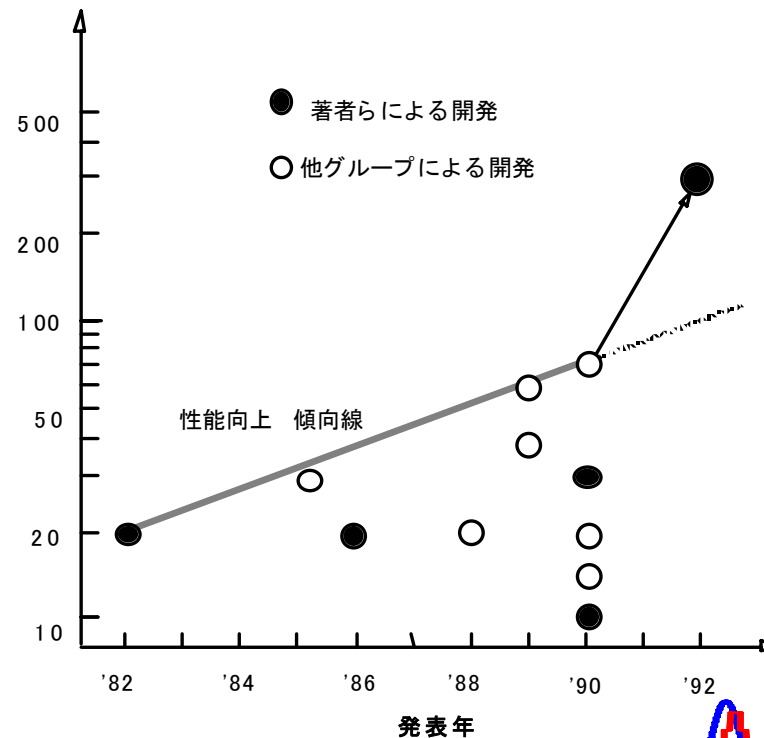
**Panasonic：10b 100MHz OSC (1986年）**



VP-5760A ¥1,490,000(税別)

# Ultra fast 10b 300MHz ADC

**World fastest 10b ADC contributed to high speed optical communication for HDTV signals.**



1.2um Bipolar
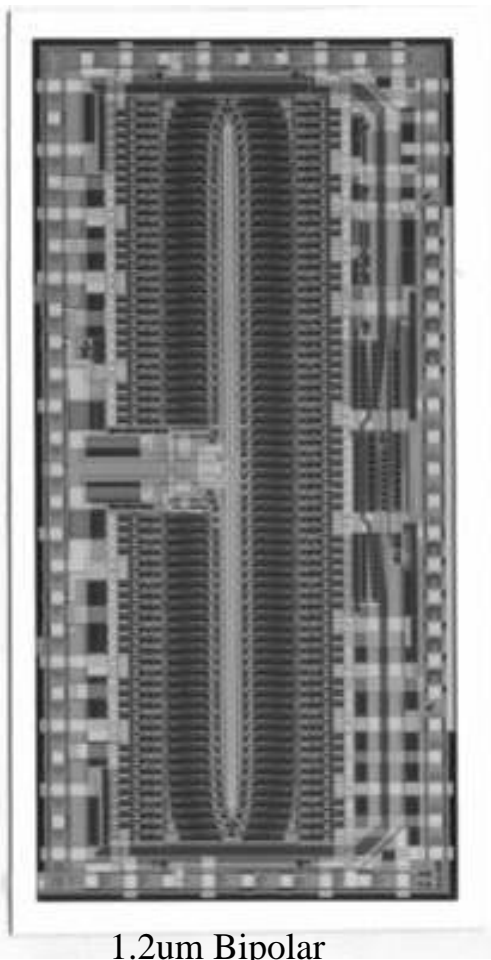
**Bipolar 10b 300MHz, 4W**
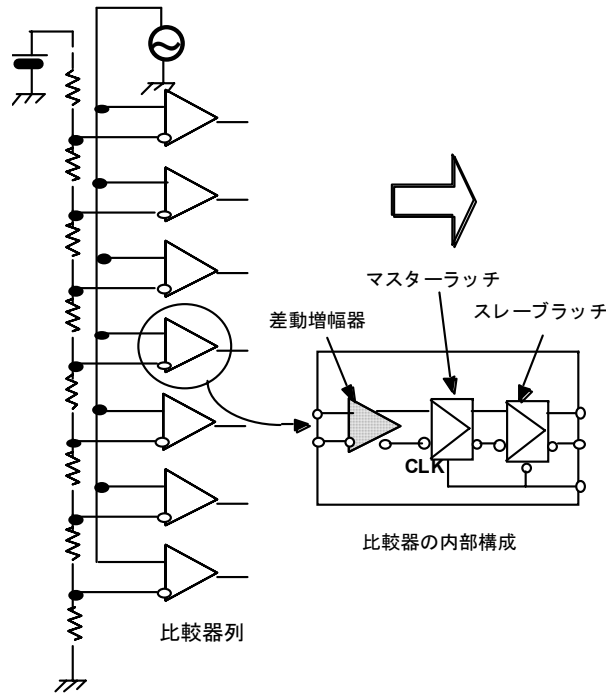
**H. Kimura and A. Matsuzawa, VLSI Symposia '92
JSC, SC-28, 1993.**



● 著者らによる開発

○ 他グループによる開発

性能向上　傾向線

発表年

2008.04.24　　　　　　　　　　　NTU A. Matsuzawa

**Matsuzawa
& Okada Lab.**

**Relax mismatch → use of high speed transistors**

**High speed and high accuracy flash ADCs**

**Parallel**

**Interpolated parallel**
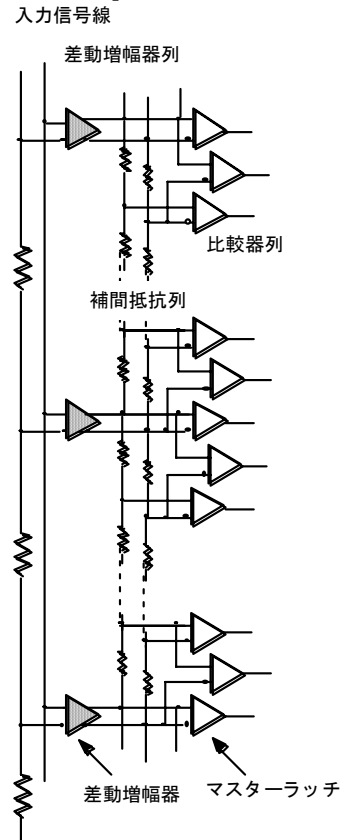
**Amplified signal is applied**

入力信号線

差動増幅器列

比較器列

マスターラッチ

スレーブラッチ

差動増幅器

CLK

比較器の内部構成

補間抵抗列

比較器列

差動増幅器    マスターラッチ

従来の並列型A/D変換器

高速バイポーラトランジスタ
のオフセット領域

誤差0.5LSB以下
の精度の達成確率

補間型A/D変換器

100

10

1

0.1

0        0.5        1.0        1.5

オフセット電圧ばらつき σ(mV)

並列型A/D変換方式

補間並列型A/D変換方式

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**Matsuzawa
& Okada Lab.**
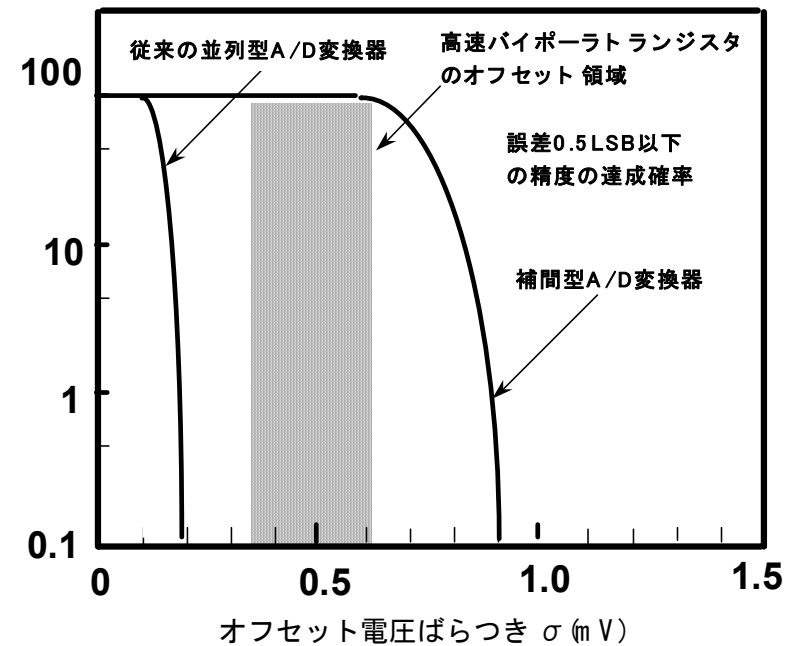
# R&D 100 Award in 1994

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**Breakthrough in ultra fast signal processing**

**In Chicago**

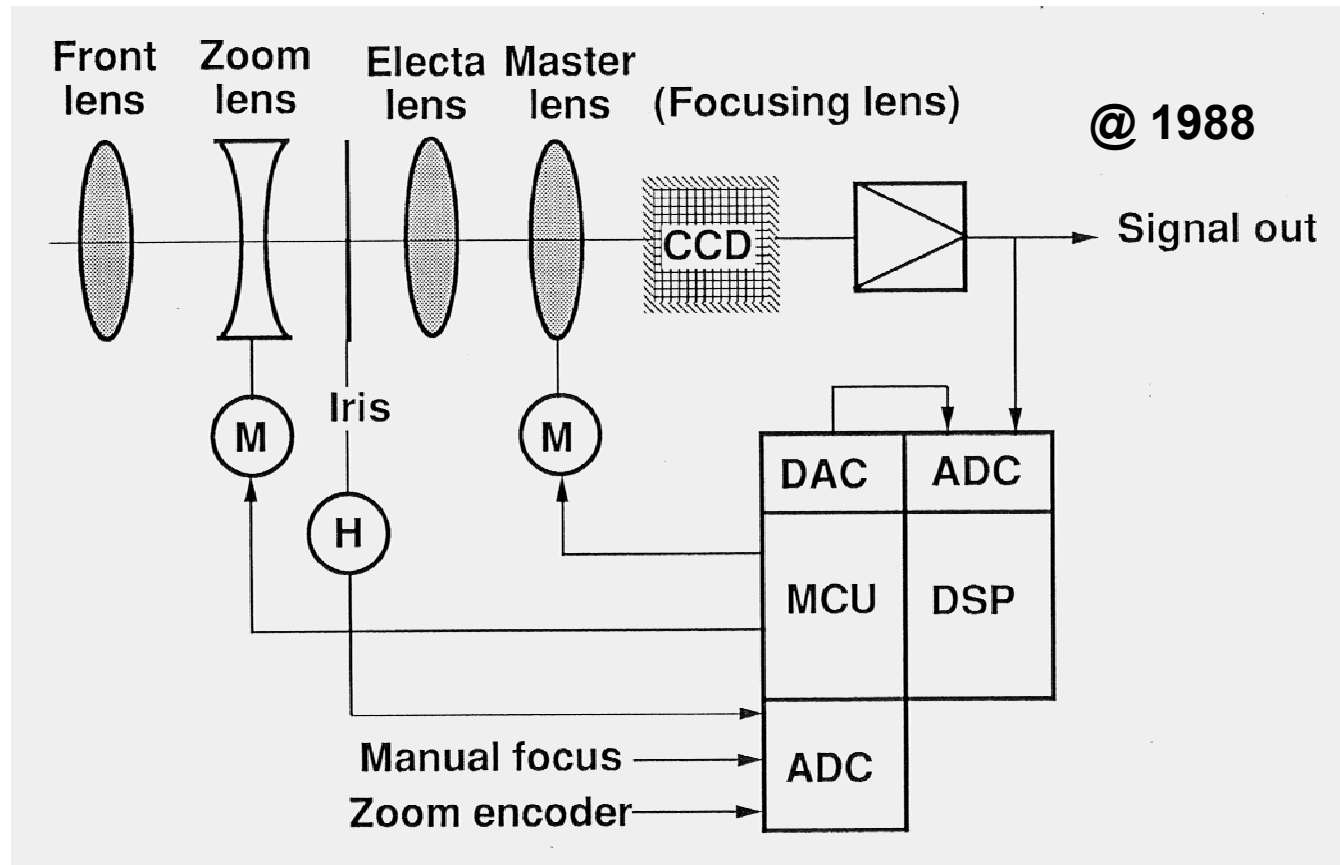**Matsuzawa & Okada Lab.**
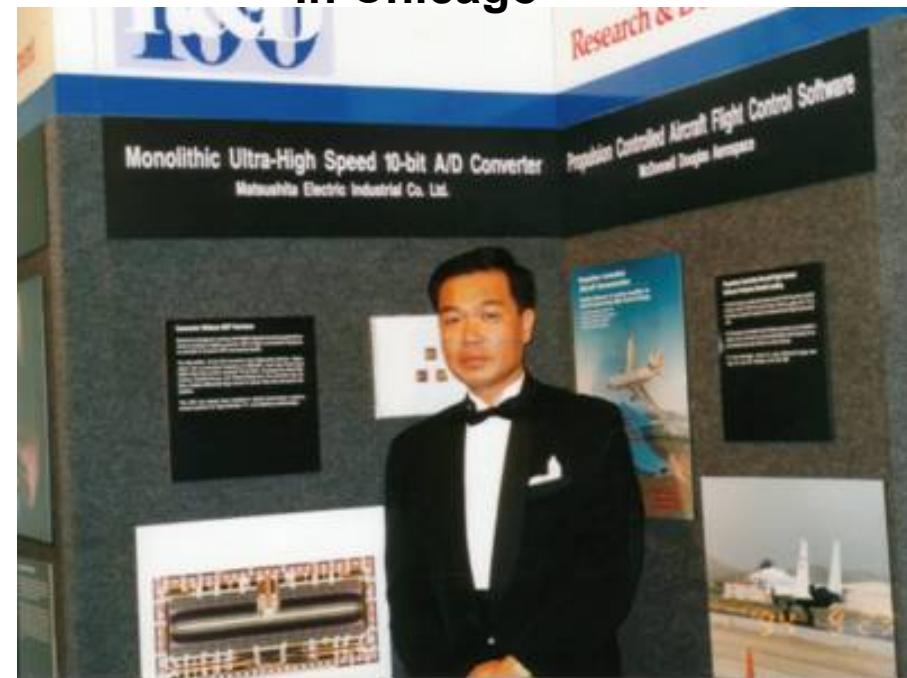
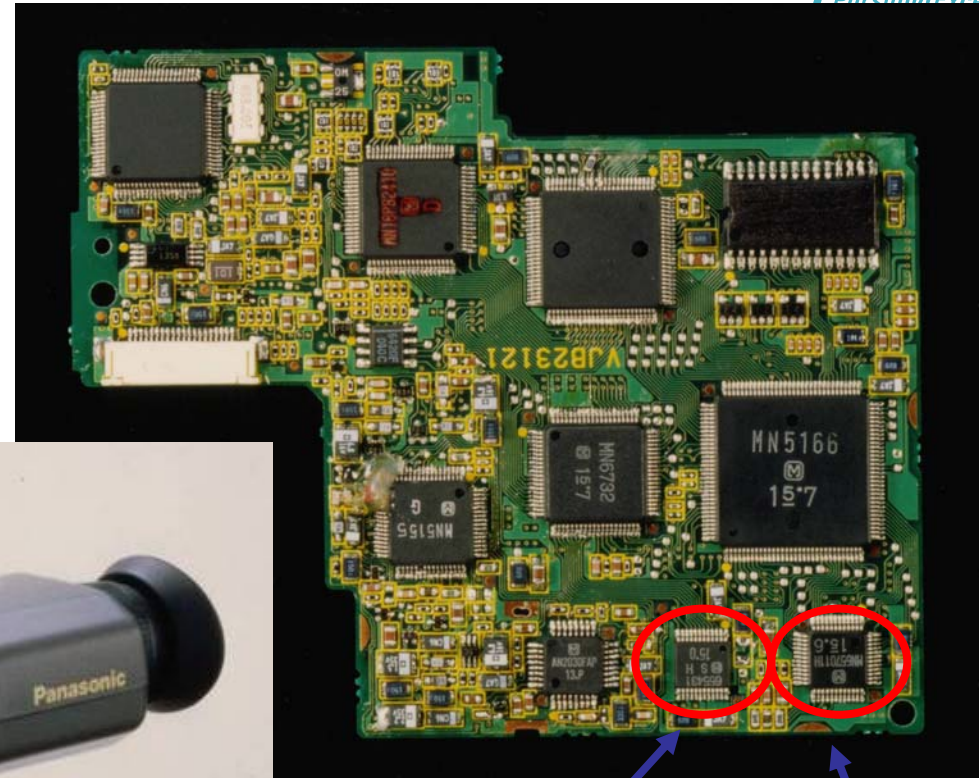**Digital camera system required ultra-low power ADCs**

**At that time, ADC consumed several 100 mW !!**

# Development of low power CMOS ADC and DAC

**Digital handy VCR needs CMOS ADCs and DACs**

1991



CMOS 8b ADC

CMOS 8b 3ch DAC

**Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.**

**1993 Model: Portable VCR with digital image stabilizing**

A. Matsuzawa, "Low-Voltage and Low-Power Circuit Design for mixed Analog/Digital Systems in Portable Equipment," IEEE Journal of Solid-State Circuits, Vol.29, No.4, pp.470-480, 1994.
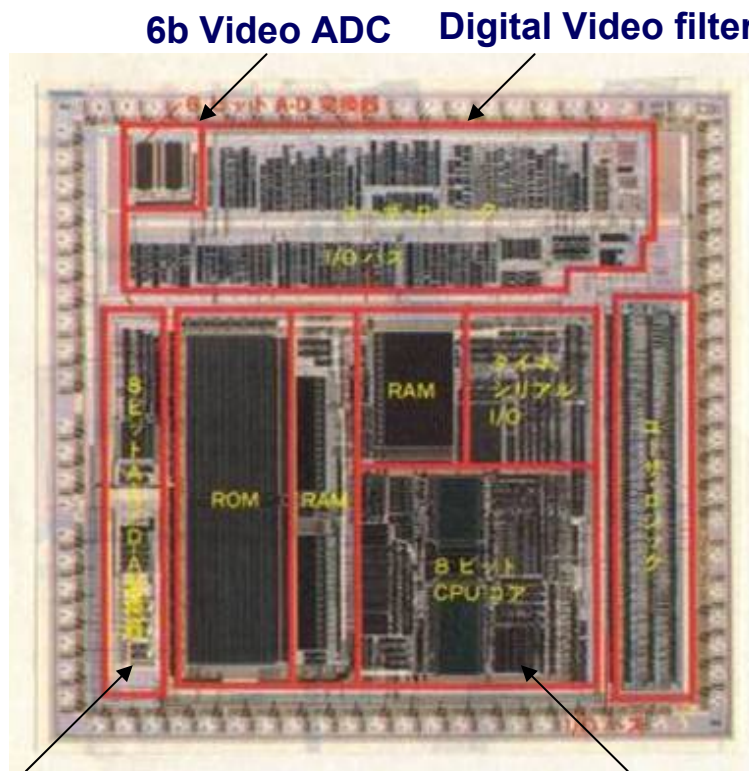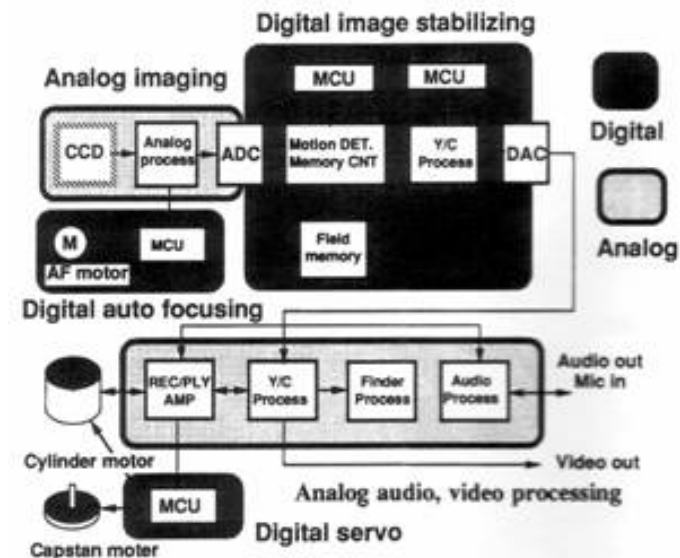
6b Video ADC    Digital Video filter



**System block diagram**
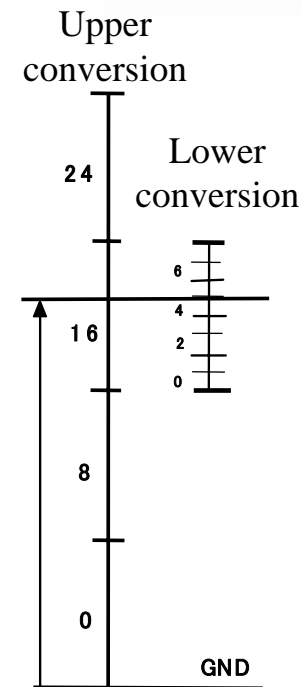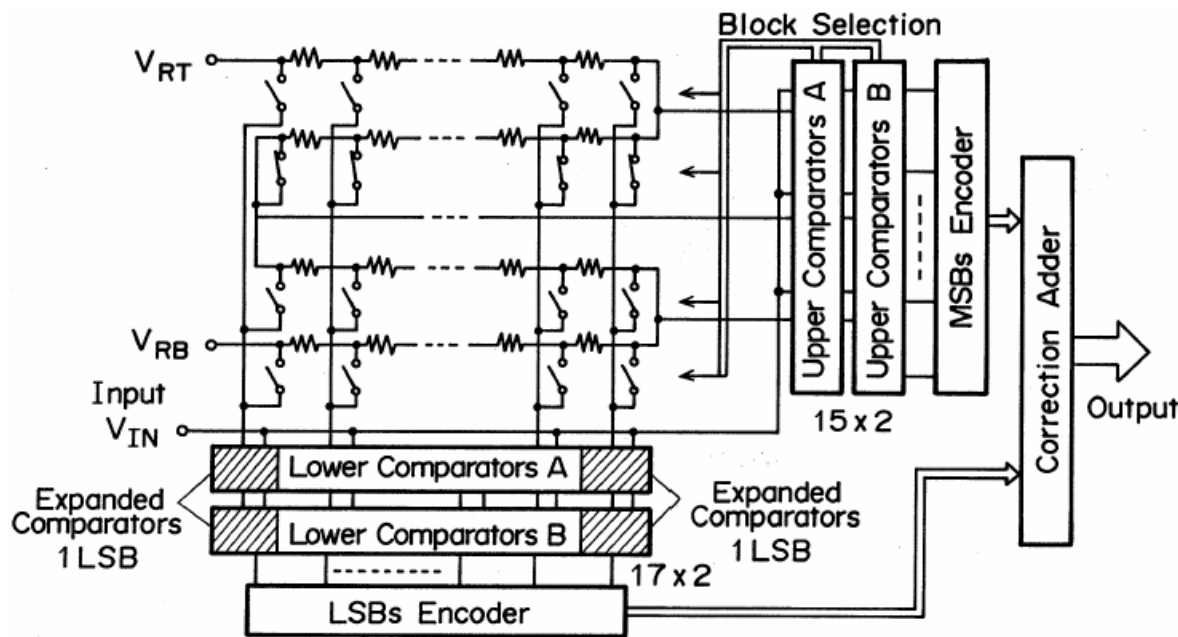


8b low speed ADC;DAC          8b CPU

Matsuzawa
& Okada Lab.

**Multi-step conversion can reduce the # of comparators.**
**As a result, small power and area.**
**However, it needs high precision comparators.**

$$10bits: \ Flash; \ 2^N - 1 = 1023$$

$$two \ step; \ 2\left(2^{\frac{N}{2}} - 1\right) = 62$$   **N. Fukushima, ISSCC 1989**

**Slide gauge**



Input voltage

**Matsuzawa & Okada Lab.**

# Chopper inverter comparator

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**CMOS has very large mismatch voltage and couldn't be used in ADC.**

**Offset cancel and signal sampling with simple circuit**

**This invention opened the door of CMOS ADCs**

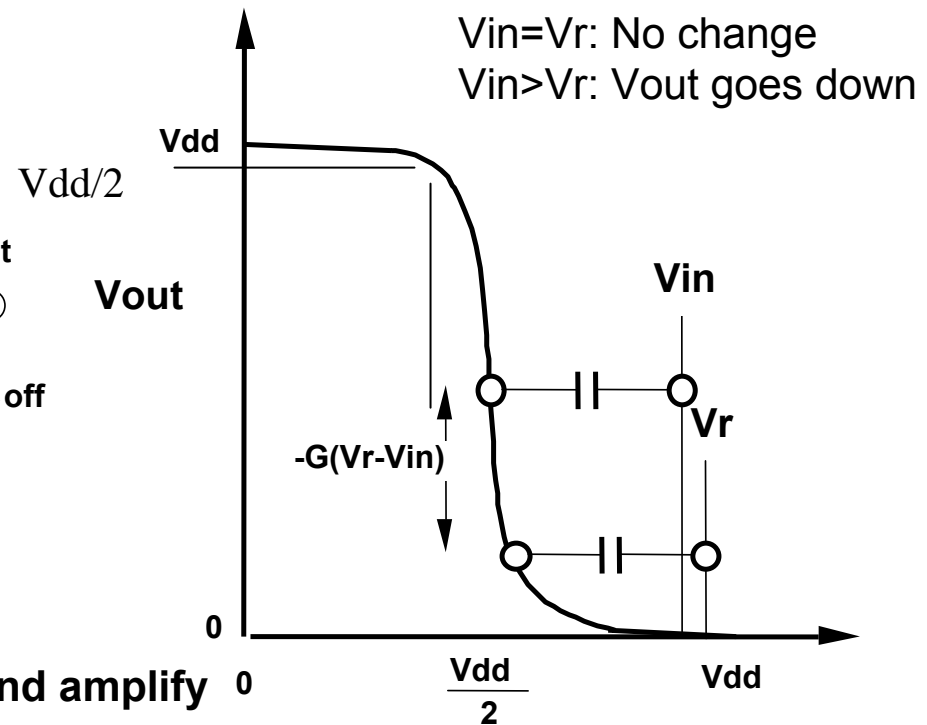Pros: Simple, low power, small area, low voltage, and sample and hold action
Cons: large absolute offset, suffer the power supply noise, sensitive to $V_{dd}$.

**A. Dingwall, JSC, SC-14, 1979**

Vdd

S1 on → off
Vg
Vin
C
Vout
Vr
S2
S3
off → on
on → off
GND

Vin=Vr: No change
Vin>Vr: Vout goes down

Vdd

$Vdd/2$

Vout

$-G(Vr-Vin)$

Vin

Vr

0

0   $\dfrac{Vdd}{2}$   Vdd

Vg

**S1, S2:ON, S3:OFF; Signal sampling**
**S1, S2:OFF, S3:ONN; Offset cancel and amplify**

Matsuzawa & Okada Lab.

# Two step parallel ADC

**A two step parallel ADC needs signal sampling function.
CMOS can realize it.**

**N. Fukushima, ISSCC 1989**



上位コンパレータ

For upper conversion

インバータ1c  インバータ2c
インバータ1f  インバータ2f

下位コンパレータ
For lower conversion
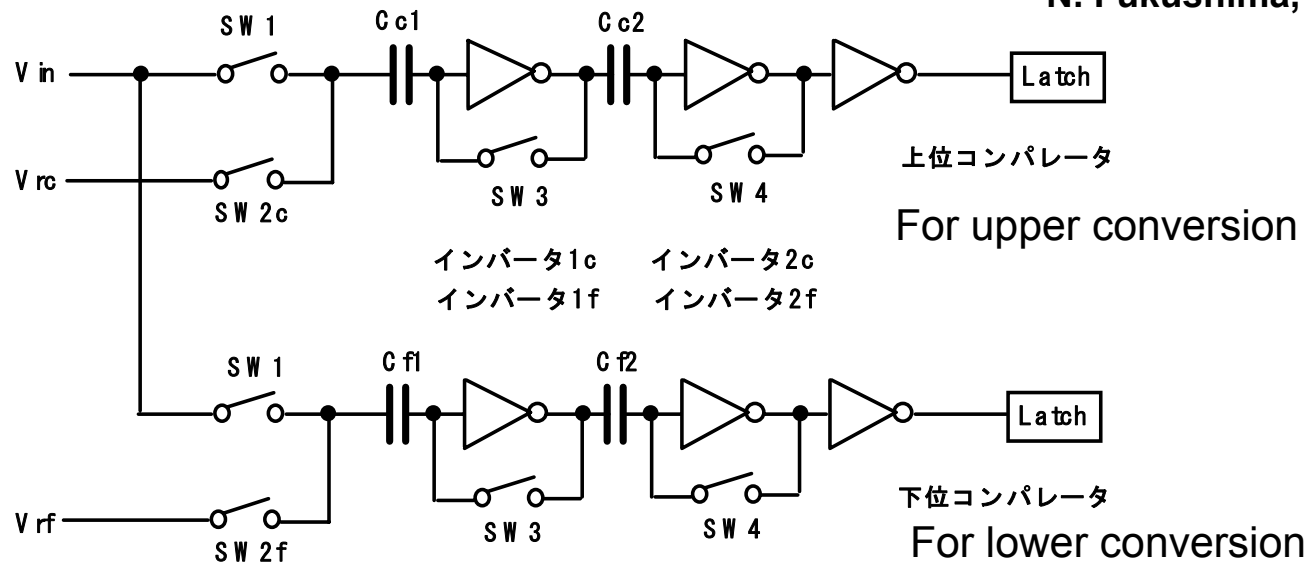
Realizing simultaneous signal sampling
2 channel lower conversion units realize two times higher operation
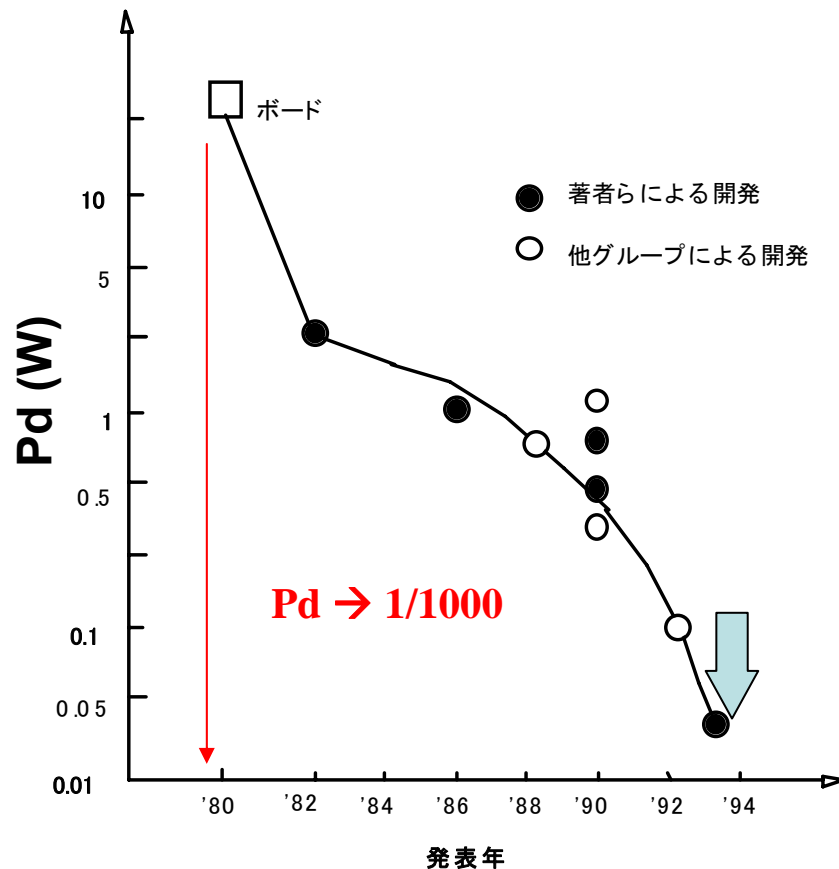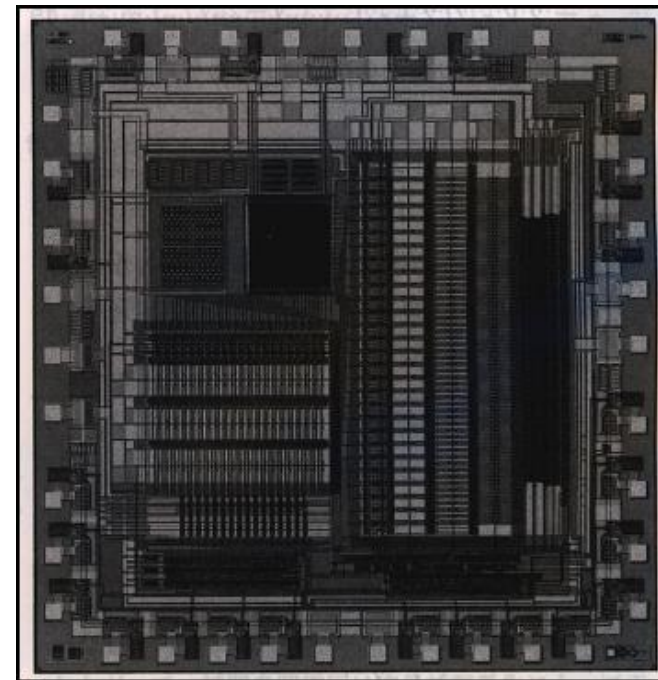Overlap scheme relaxes needed offset voltage for comparators

**To realize the digital handy video camera, Ultra low power ADC was needed.**

**We could develop world lowest power video-rate 10b, CMOS ADC.**

**CMOS 10b, 20MS/s, 30mW**
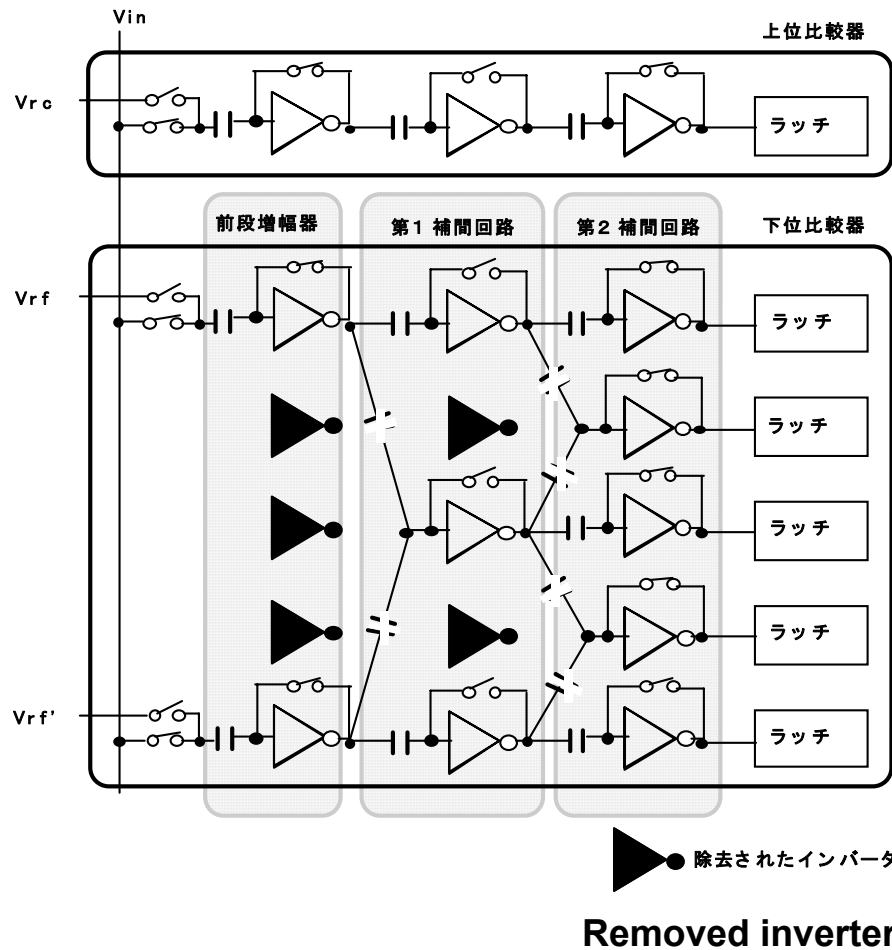
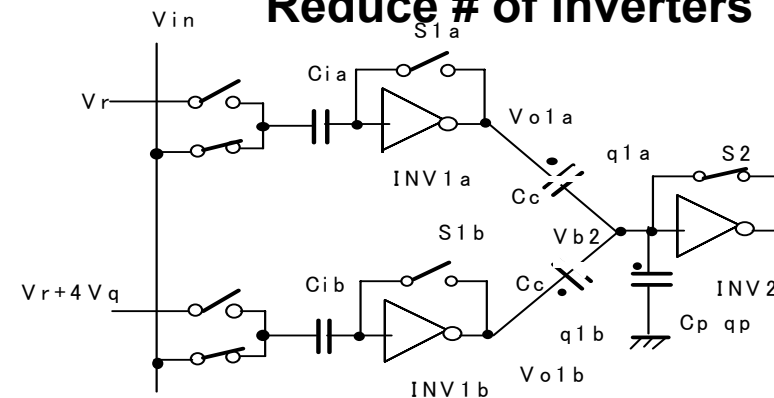**K. Kusumoto, A. Matsuzawa**
**ISSCC '93, JSC 1993.**

@0.8umCMOS ADC

**Simple circuits; switch, capacitors, and inverters**

**Amplify, offset cancel, interpolation, sampling**



**Removed inverter**

**Relax mismatch**
**Reduce # of inverters**



回路状態1,INV1a,INV1b:増幅状態,INV2:バイアス状態
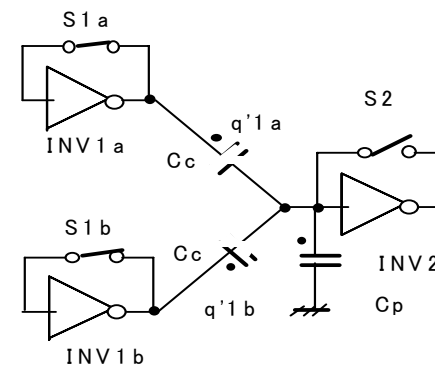


回路状態2,INV1a,INV1b:バイアス状態,INV2:増幅状態

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# Interpolation method

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**Interpolation can generate accurate intermediate references which are between two references. Thus step sizes are almost equal, even though mismatch voltages are large.**
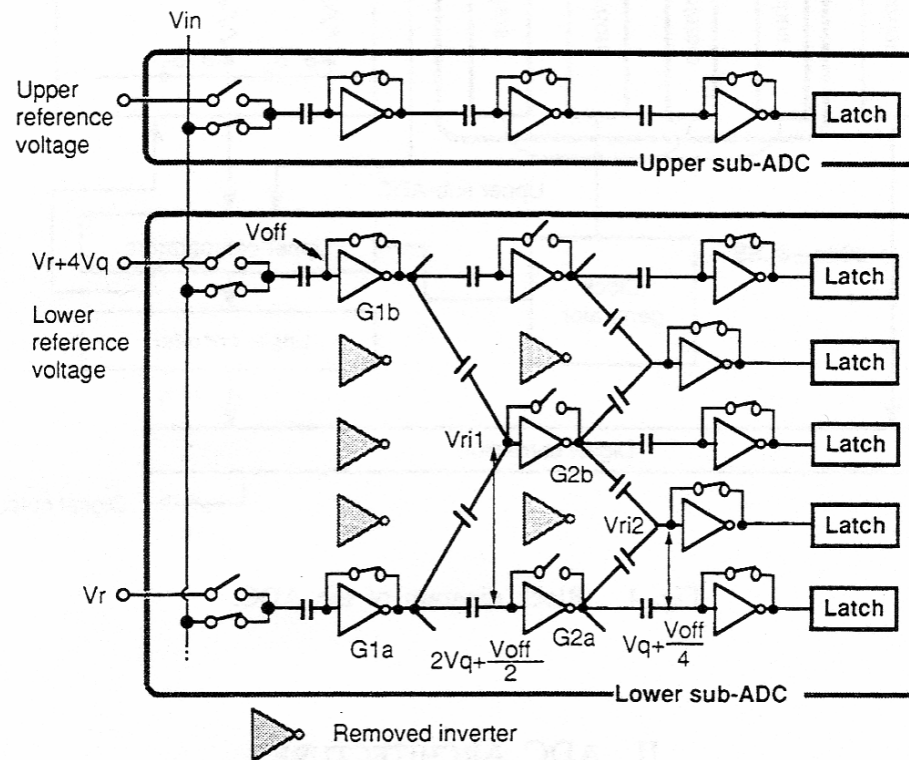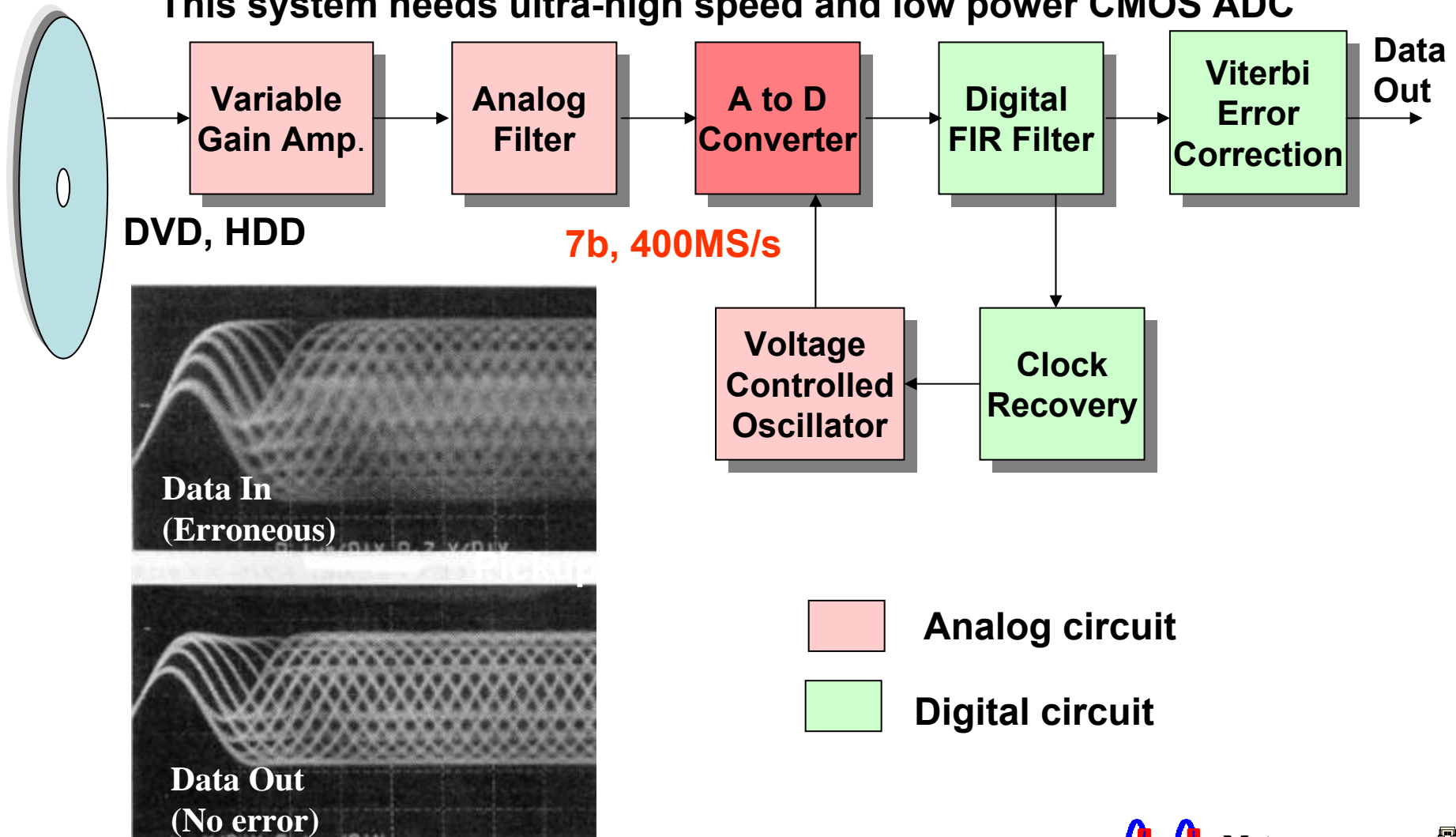


K. Kusumoto and A. Matsuzawa
JSC, pp. 1200-1206, 1993.

NTU A. Matsuzawa

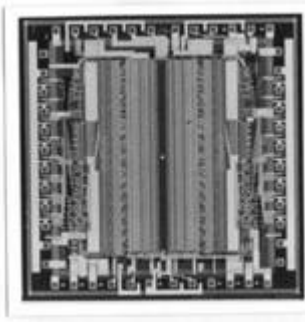Matsuzawa
& Okada Lab.
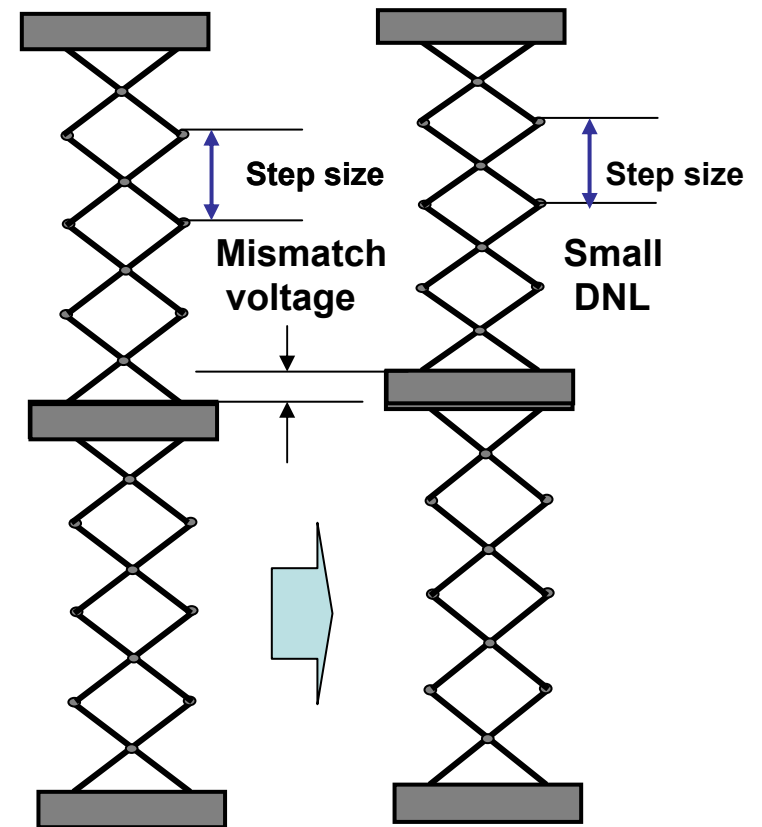
# Mixed signal tech. ; Digital read channel

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**Digital storage also needs high speed mixed signal technologies.**

**This system needs ultra-high speed and low power CMOS ADC**

DVD, HDD

Variable Gain Amp. → Analog Filter → A to D Converter → Digital FIR Filter → Viterbi Error Correction → Data Out

**7b, 400MS/s**

Voltage Controlled Oscillator ← Clock Recovery

Data In (Erroneous)

Data Out (No error)

Analog circuit

Digital circuit

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**Matsuzawa & Okada Lab.**

**High speed ADCs have reduced power and area down to be embedded.**

### World fastest 6b ADC

6b, 1GHz ADC
2W,
1.5um Bipolar

A. Matsuzawa, SSCC 1991

### World fastest CMOS ADC

K. Sushihara and A. Matsuzawa, ISSCC 2000.
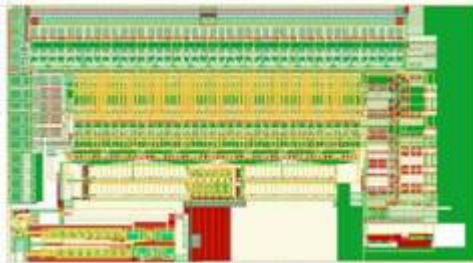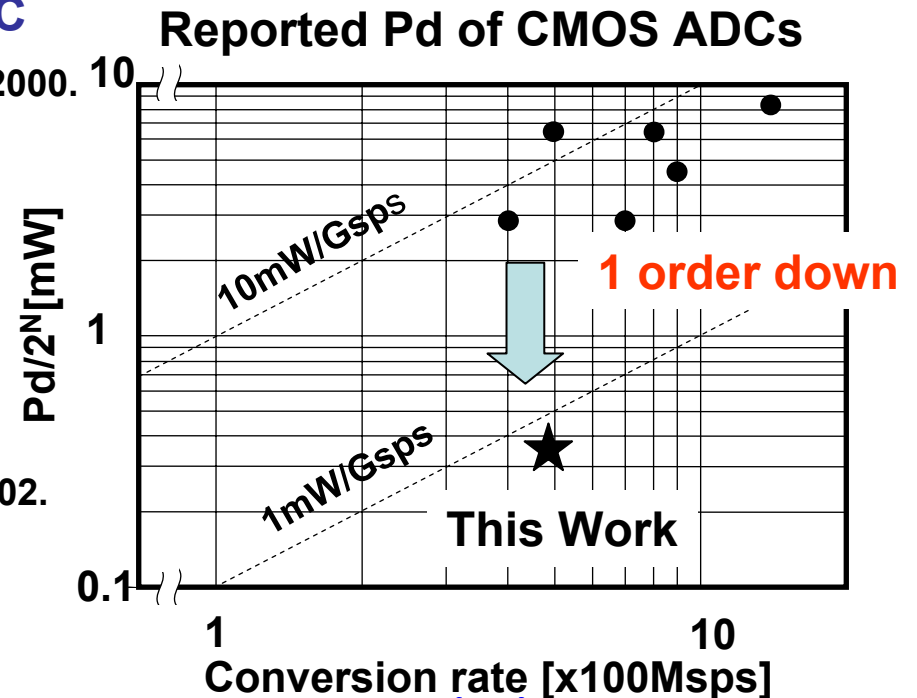
6b, 800MHz ADC
400mW, 2mm²
0.25umCMOS

### World lowest Pd HS ADC

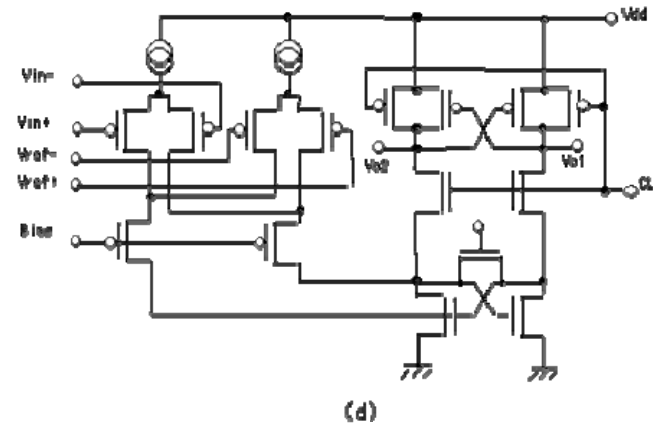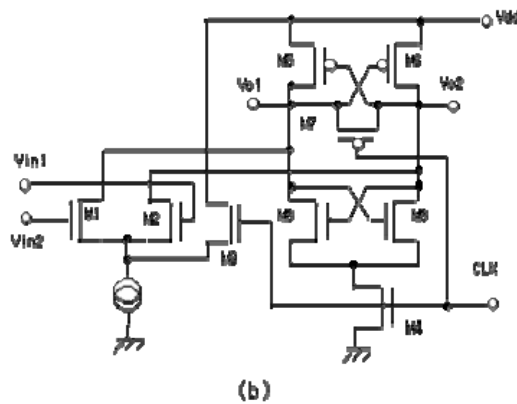K. Sushihara and A. Matsuzawa, ISSCC 2002.

7b, 400MHz ADC
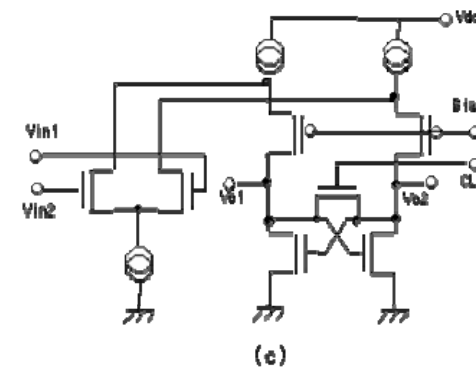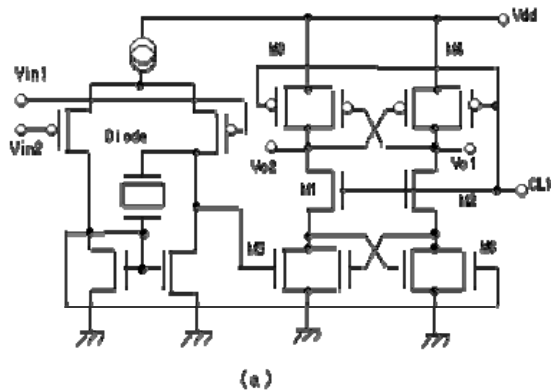**50mW, 0.3mm²**
0.18umCMOS

**Reported Pd of CMOS ADCs**



10mW/Gsps

1mW/Gsps

$Pd/2^N$[mW]

**1 order down**

★

**This Work**

0.1

1 ... 10

**Conversion rate [x100Msps]**

Matsuzawa & Okada Lab.

# CMOS comparators

**There are many types of comparator circuits,
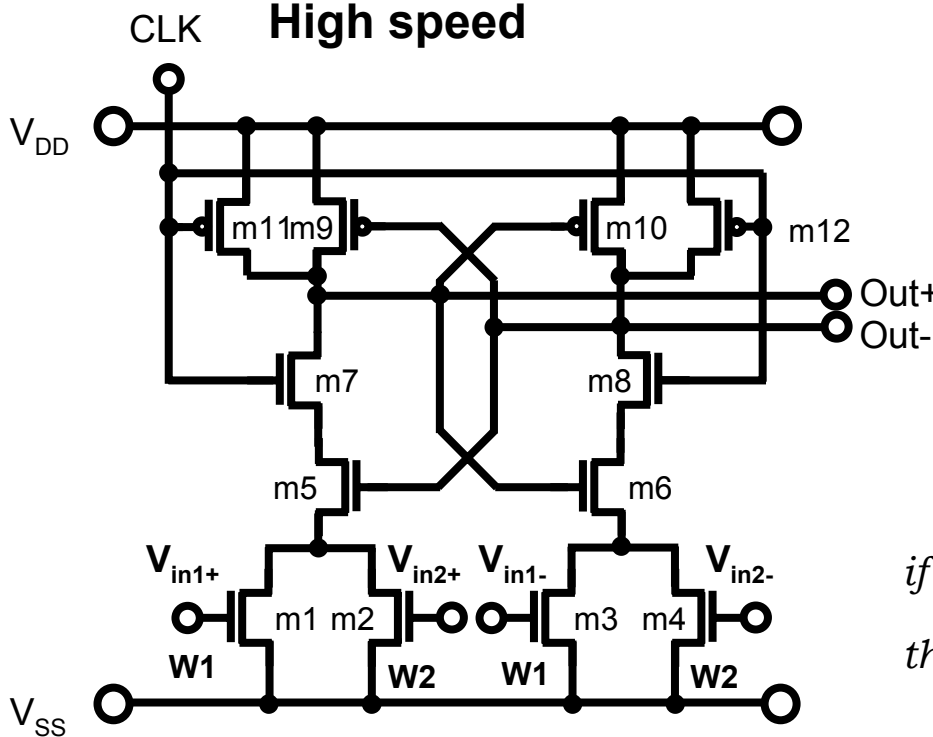However all need static current.**

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**A CMOS comparator is low power because of no need of static current.**

**No static current**
**Differential comparison**
**Interpolation action**
**High speed**

T.B.Cho., et al., J.S.C., Vol.30,
No.30, pp.166-172, Mar. 1995.

**Interpolation action**

$$G_1 = K_p \left[ \frac{W_1}{L} \left( V_{in1+} - V_{th} \right) + \frac{W_2}{L} \left( V_{in2+} + -V_{th} \right) \right]$$

$$G_2 = K_p \left[ \frac{W_1}{L} \left( V_{in1-} - V_{th} \right) + \frac{W_2}{L} \left( V_{in2-} + -V_{th} \right) \right]$$

$$if \ W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m}$$

$$then, \ (m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-}$$

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& Okada Lab.

**No static current and can realize interpolation without current consume, resistive interpolation.**



Output of Pre-amplifiers

$$\frac{(m-n)V_{n-1} + nV_n}{m}$$

$$\frac{(m-n)CV_{n-1} + nCV_n}{m}$$

CVn      Vn-1

CVn-1

Vn

Vrn-1        Vrn

Comparator Latches with Interpolation Circuits

Pre-Amplifiers

CVn-1  Vn-1    CVn  Vn

Vin

Vrn-1    Reference Resistor    Vrn

*Gate width ratio*
*W1:W2=(m-n)/m : n/m*

CLK

VDD

m11 m9        m10 m12

Out+
Out-

m7        m8

m5        m6

In1+    In2+In1-    In2-

m1  m2        m3  m4

W1  W2      W1  W2

VSS

Matsuzawa & Okada Lab.
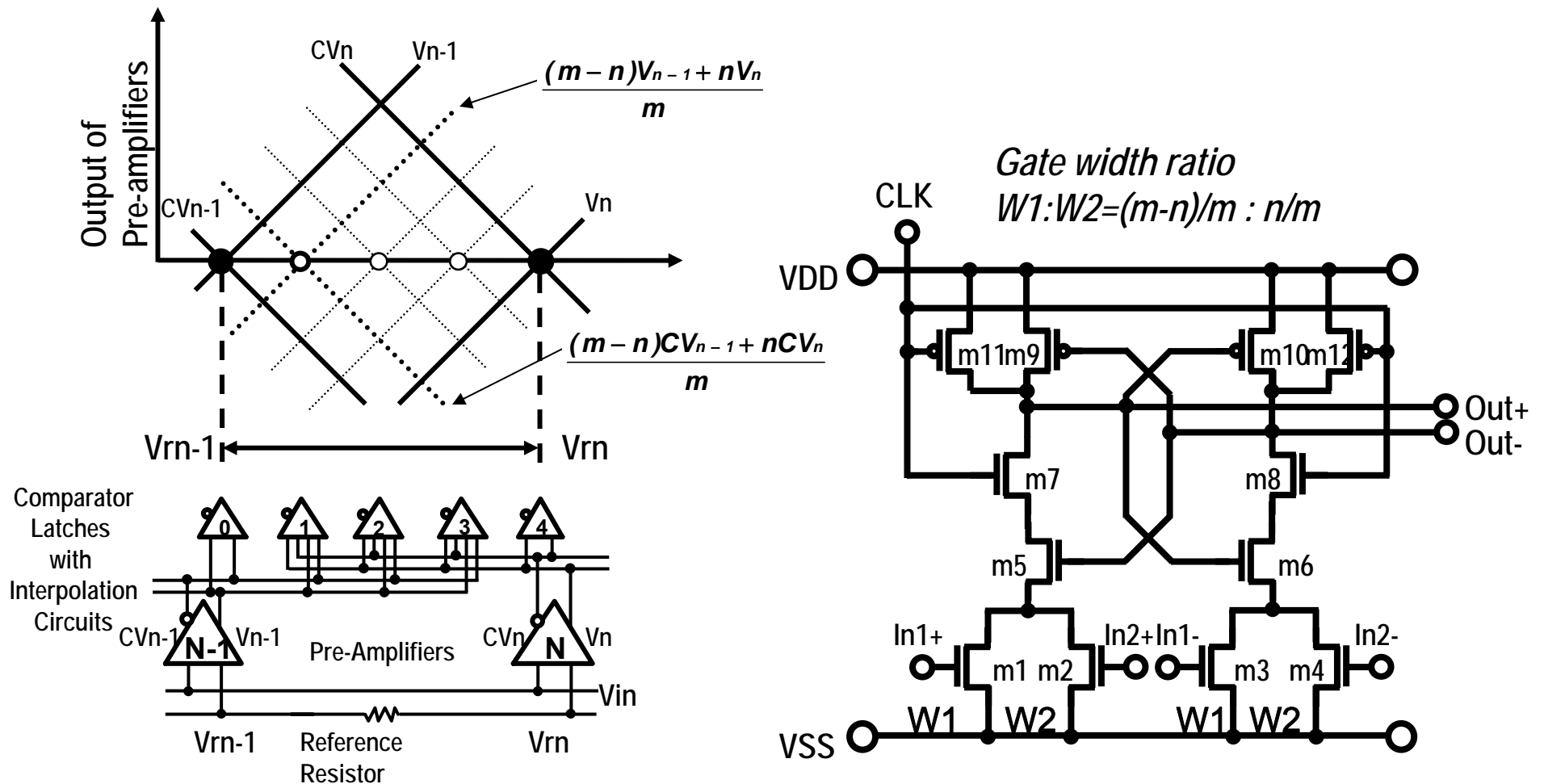
# 7b, 450MHz, 50mW CMOS ADC

**A 7b, 450MHz, 50mW CMOS ADC has been developed for the mixed signal SoC**

**This power dissipation is about 1/10, compared with the conventional high speed ADCs.**

**K. Sushihara and A. Matsuzawa, ISSCC 2002.**
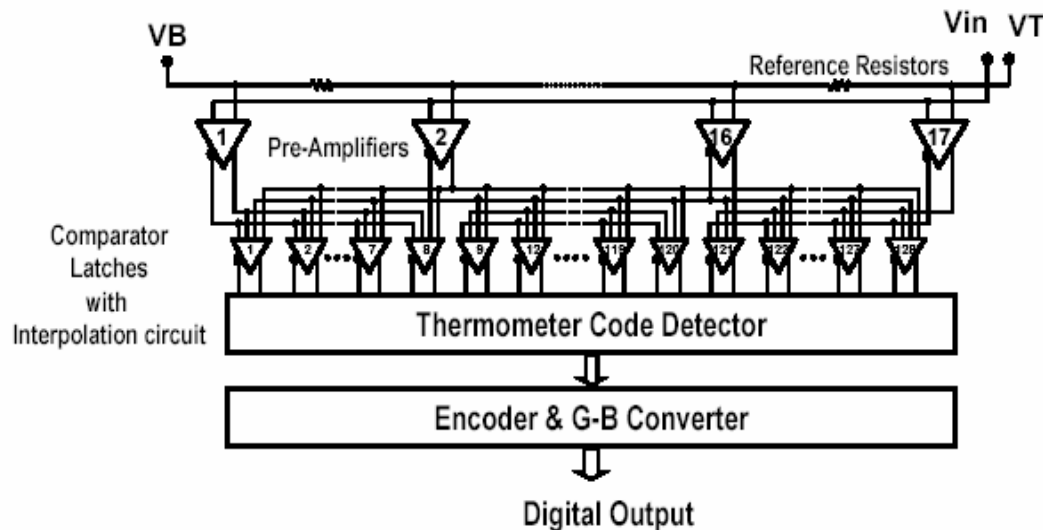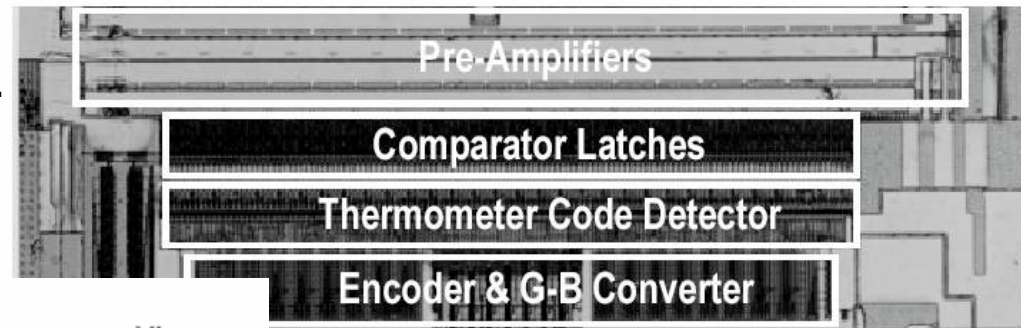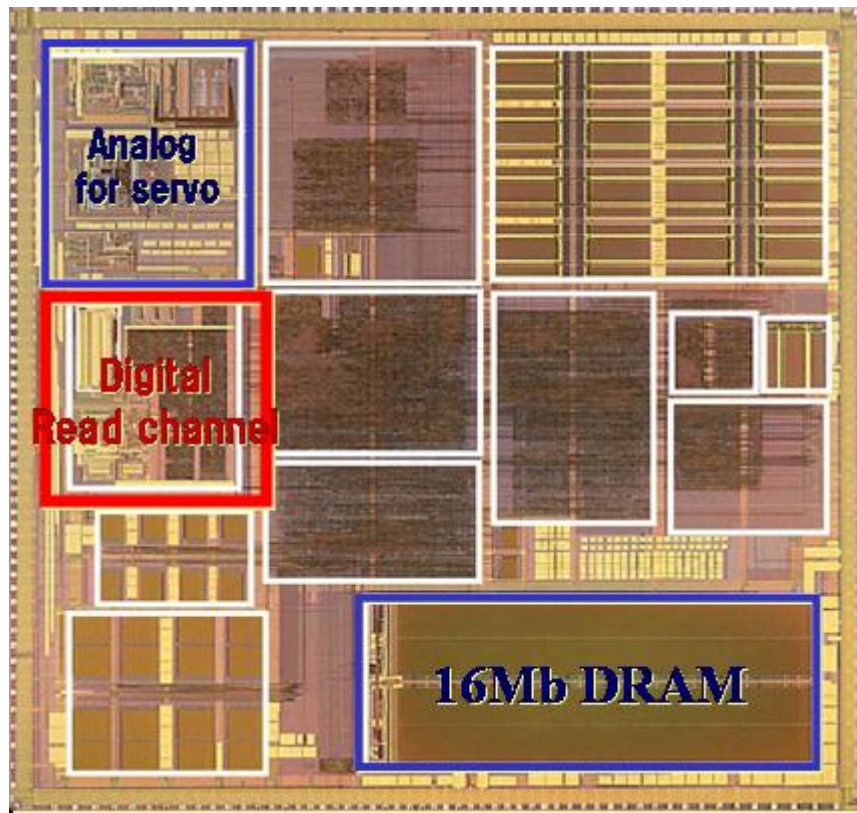


Technology : 0.18um CMOS(3AL,1PS)
Area : 0.88mm X 0.34mm

**Digital read channel can realize high readability for weak signal from DVD RAM pickup.**

**World fastest and highly integrated mixed signal CMOS SoC**



S. Goto… A. Matsuzawa, ISSCC 2001.
JSC 2001.

0.18um- eDRAM

24M Tr
16Mb DRAM

500MHz
Mixed Signal

**Advanced mixed signal SoC has been successfully developed.**

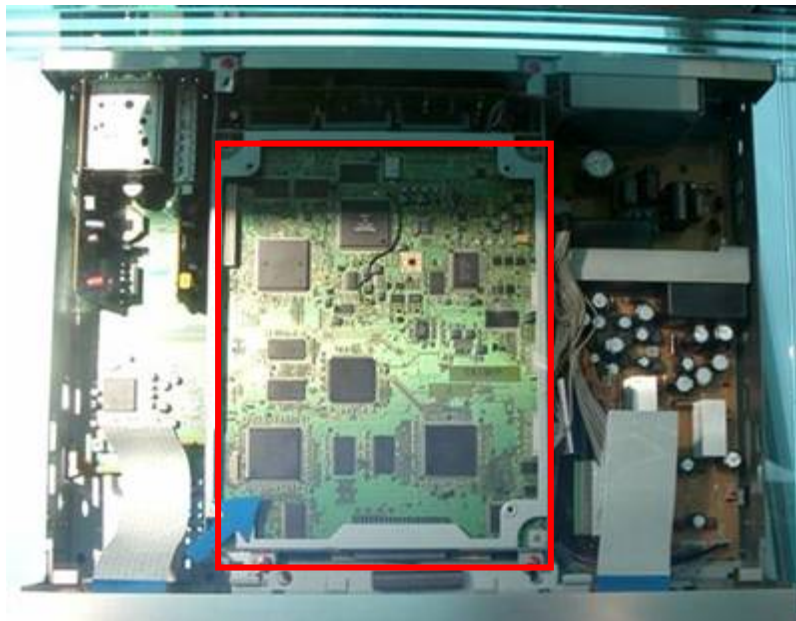Okamoto,…, A. Matsuzawa., ISSCC 2003, JSC 2003.    0.13um, Cu 6Layer, 24MTr
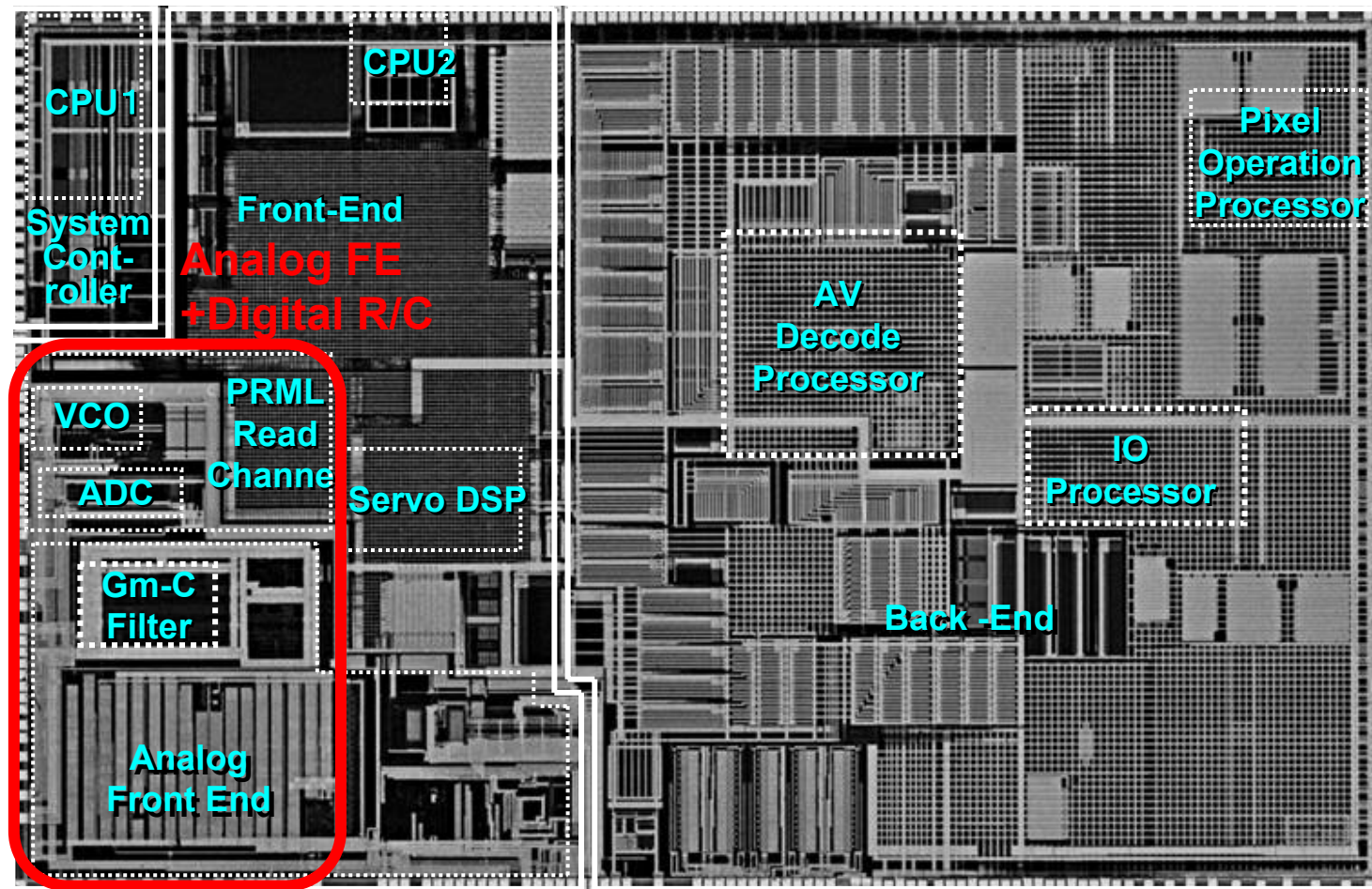
# Cost reduction in DVD Recorder

*TOKYO TECH*
*Pursuing Excellence*

One-chip integration of hole DVD system has been realized.
This makes circuit board simpler and contributes to the cost down,
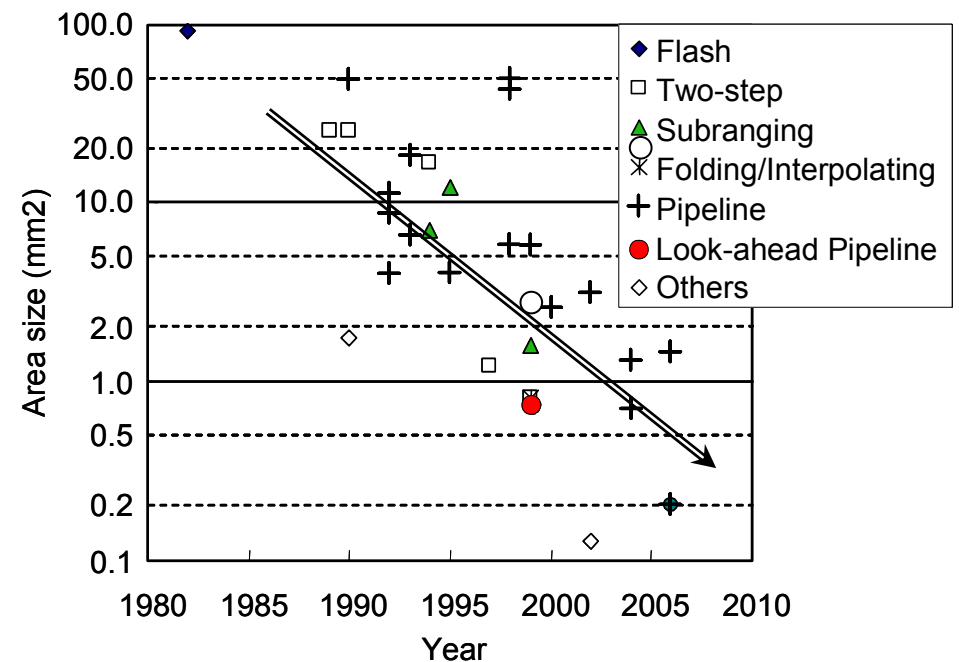as well as performance up.

'2000 Model



'2003 Model

NTU A. Matsuzawa

**Matsuzawa & Okada Lab.**

# Power and area reduction of video-rate 10b ADCs

**Power and area of ADC have been reduced continuously.
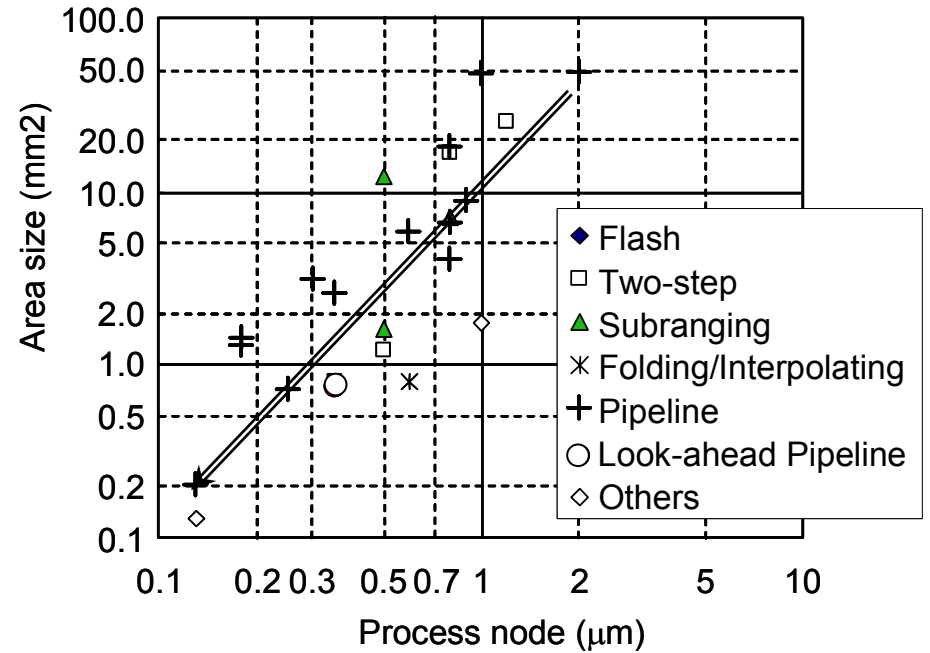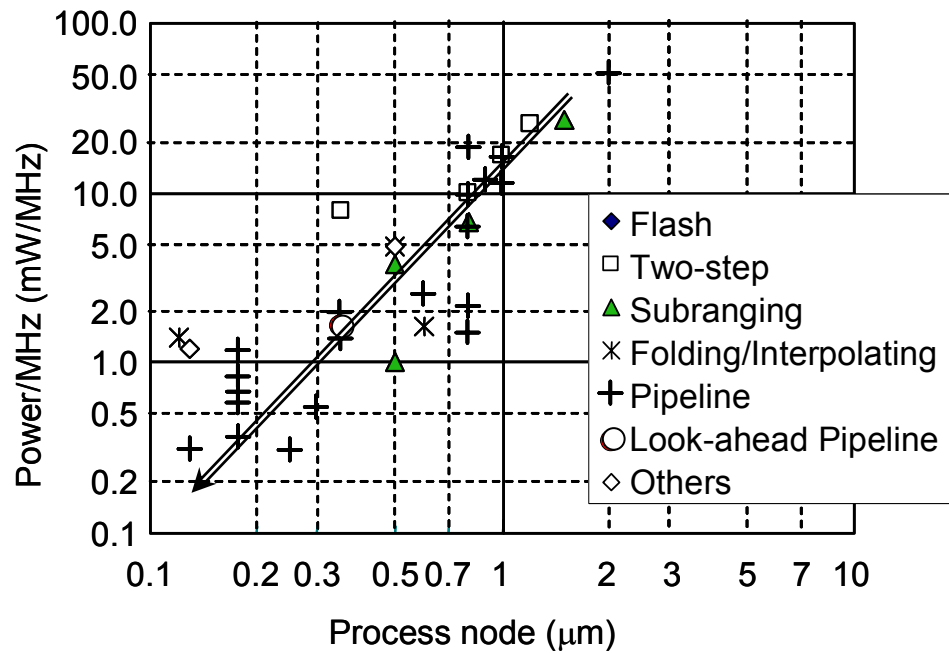Currently, ADC can be embedded on a chip**

### Power reduction

### Area reduction

NTU A. Matsuzawa

M. Hotta et al. IEICE 2006. June
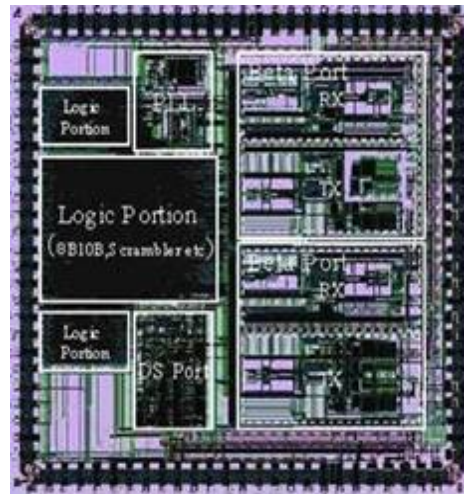
# Developed mixed signal CMOS LSIs

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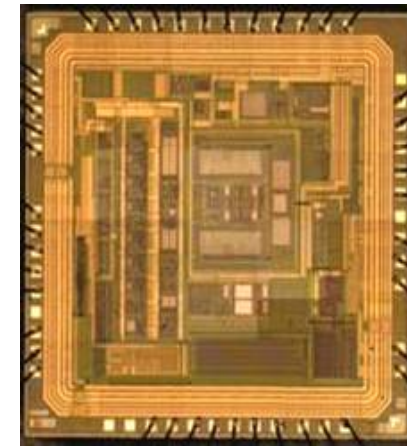**5G RF LAN** *12b 50MHz ADC 2ch*
*12b 50MHz DAC 2ch*
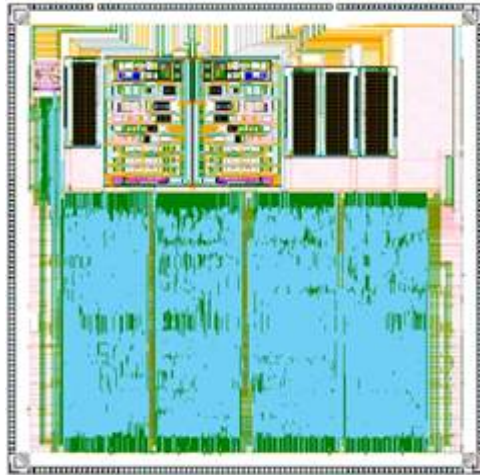
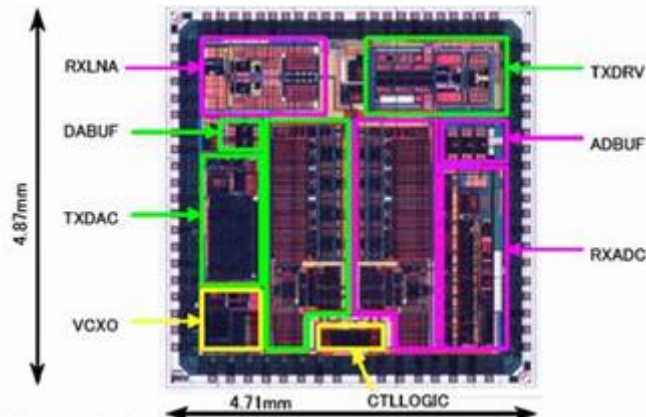**Digital network 1394b (1GHz)**

**AFE (Analog Front End)**

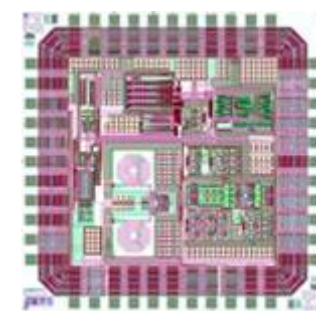**AFE for Digital Camera**

*12b 20MHz ADC+AGC*



**AFE for ADLS** *12b 20MHz ADC+DAC*
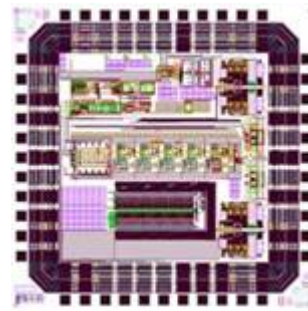
**2GHz RF CMOS**

NTU A. Matsuzawa

**Matsuzawa & Okada Lab.**
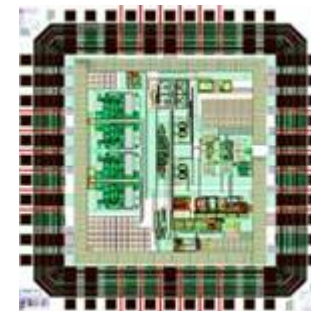
**Elected IEEE fellow in 2002**



INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

**Fellow Award** 2002

Akira Matsuzawa

for CONTRIBUTIONS to

high-speed A/D converters and mixed-signal integrated circuits.