Design Space Exploration of Low-Phase-Noise LC-VCO Using Multiple-Divide Technique

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***Abstract*— This paper proposes a multiple-divide technique using by-2, by-3, and by-4 frequency dividers to realize a lower phase-noise LC-VCO, and explores the design space of low-phase-noise VCO using the multiple-divide technique. In the simulated results using 90-nm CMOS model parameters, the optimum frequency range, achieving better than −191 dBc/Hz of FoM, can be extended from 6-12 GHz to 1.5-12 GHz.**

I. Introduction

Recently, Si CMOS technology has obtained higher f_{T} and f_{max}, which enables large possibilities for CMOS RF applications. Many kinds of commercial RF products have been realized by the CMOS technology due to high-density integration, mixed-signal implementation, and lower fabrication cost. On the other hand, one of the biggest problems is that on-chip inductors have only 15 of quality factor at most because of thin metal thickness and Si substrate loss, which limits performances of CMOS RF circuits. Especially, LC-VCO (Voltage-Controlled Oscillator) has a poor performance due to the low-Q on-chip inductor even if it is one of the most important key components of wireless communication circuits.

There are several circuit techniques to improve phase noise of VCOs [1], [2]. However, the phase noise is basically limited by quality factor of inductors. The quality factor of on-chip inductor depends on spiral topology, metal resistivity, substrate conductivity, dielectric characteristics of ILDs, and the optimum structure is unique for each frequency and each process. It is experimentally known that higher Q inductors can be realized at higher frequencies. Thus, this paper proposes a multiple-divide technique to synthesize the required frequency as shown in Fig. 1. To avoid the local leakage, it is a common technique to use a doubled-frequency VCO with a divide-by-2 frequency divider. In some cases, better phase-noise characteristics can be obtained by such the dividing architecture at the cost of larger power consumption of VCO. On the other hand, recent miniaturized CMOS transistors can provide higher oscillation frequency with reasonable power consumption due to the higher f_{T} and f_{max}, which might be employed for improving phase noise performance in the recent deep-submicron era. To extend this idea, the multiple-divide technique using by-2, by-3, and by-4 dividers is proposed.

In this paper, simulated results using 90-nm CMOS model parameters are presented, and it is also shown that the optimum frequency range achieving better phase noise can be extended by the proposed multiple-divide technique.

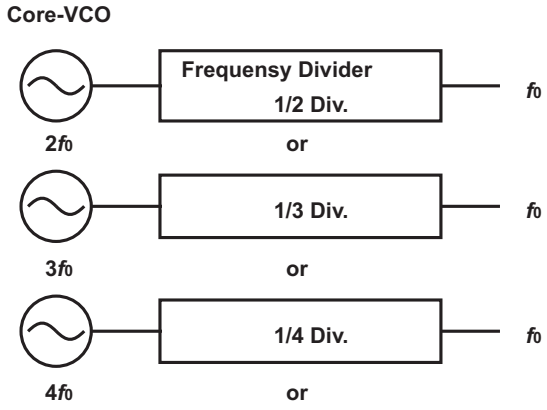

Fig. 1. The proposed system diagram.

II. Design of VCO Using Frequency Divider

This section explains design consideration of LC-VCO using a multi-divide frequency divider to achieve lower phase-noise and smaller power dissipation.

Figure 2, 3 shows the proposed circuit. There are several trade-offs to choose a circuit configuration according to the required frequency. In this paper, VCO consisting of PMOS cross-coupled pair and PMOS current source is utilized as shown in Fig. 2 because of low noise characteristic of PMOS transistors. 3-stage ILFD (Injection-Locked Frequency Divider) is employed as shown in Fig. 3. Phase noise is deeply linked to power consumption of VCO, and the total power consumption of the proposed circuit is increased by higher oscillation and additional power dissipation of frequency divider while lower phase-noise might be obtained.

In this section, power consumption and phase noise are discussed, and it is shown that the design space of LC-VCO can be expanded by using the multiple-divide technique.

A. VCO Analysis with Frequency Divider

Here, VCO performances, *i*.e., phase noise, power consumption, etc, are discussed in consideration of a frequency divider.

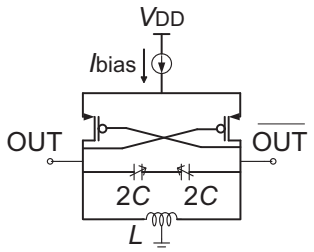

Fig. 2. VCO topology.

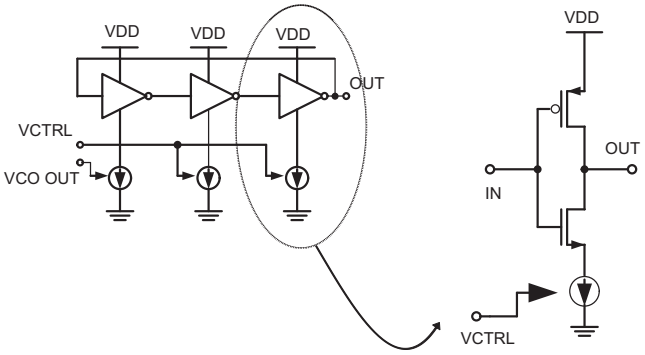

Fig. 3. 3-stage injection-locked frequency divider.

Phase noise at output of a divide-by-2 frequency divider is 6 dBc/Hz better than that of VCO. In general, divide-by-N dividers can improve $20\log N$ [dBc/Hz] of phase noise, because the frequency divider narrows side-lobe of phase noise as carrier frequency becomes small.

On the other hand, phase noise depends on oscillating frequency, oscillation amplitude, and quality factor of LC tank. Phase noise $\mathcal{L}$ can be estimated by the following model [3].

$$\mathcal{L}(f_{\rm offset}) = 10\log\left[\frac{2{\rm kT}}{P_{\rm sig}}\left(\frac{f_0}{2Q_L f_{\rm offset}}\right)^2\right] \quad (1)$$

where k is Boltzmann's constant and T is temperature, $P_{\rm sig}$ is the average power dissipated in the resistive part of the tank, f_0 is the oscillation frequency, and $f_{\rm offset}$ is the offset frequency. Q_L is quality factor of inductor, which is almost equal to the effective quality factor of LC-tank. Q_L and $P_{\rm sig}$ are calculated as follows.

$$\begin{aligned} Q_L &= \frac{R_{\rm p}}{\omega L} & (2)\\ P_{\rm sig} &= I_{\rm bias}^2 R_{\rm p} = I_{\rm bias}^2 Q_L \omega L & (3)\end{aligned}$$

where L is inductance, $R_{\rm p}$ is parallel resistance of LC-tank, and $I_{\rm bias}$ is bias current. Therefore, the following equation can be derived.

$$\begin{aligned} \mathcal{L}(f_{\rm offset}) &= 10\log\left[\frac{kTf_0}{4\pi I_{\rm bias}^2 {Q_L}^3 L f_{\rm offset}^2}\right] & (4)\\ \mathcal{L}(f_{\rm offset})' &= 10\log\left[\frac{kTf_0'}{4\pi I_{\rm bias}'^2 {Q_L'}^3 L' f_{\rm offset}'^2}\right] - 20\log N & (5)\end{aligned}$$

To evaluate the total performance, the following FoM (Figure of Merit) is utilized.

$$FoM = \mathcal{L}(f_{\rm offset}) - 20\log\left(\frac{f_0}{f_{\rm offset}}\right) + 10\log\left(\frac{P_{\rm total}}{1{\rm mW}}\right) \quad (6)$$

where $P_{\rm total}$ is the total power consumption considering both VCO and divider. FoM and FoM' can be derived as follows.

$$\begin{aligned} FoM &= 10\log\left[\frac{kTf_0}{4\pi I_{\rm bias}^2 {Q_L}^3 L f_{\rm offset}^2}\right] \\ &\quad -20\log\left(\frac{f_0}{f_{\rm offset}}\right) + 10\log\left(\frac{P_{\rm total}}{1{\rm mW}}\right) & (7)\\ FoM' &= 10\log\left[\frac{kTf_0'}{4\pi I_{\rm bias}'^2 {Q_L'}^3 L' f_{\rm offset}'^2}\right] - 20\log N \\ &\quad -20\log\left(\frac{f_0'/N}{f_{\rm offset}'}\right) + 10\log\left(\frac{P_{\rm total}'}{1{\rm mW}}\right) & (8)\end{aligned}$$

where FoM is figure of merit of VCO without a divider, and FoM' is figure of merit of VCO using a divider. If both signal amplitudes in LC-tank are equal to each other, the following relation can be obtained.

$$\begin{aligned} I_{\rm bias} R_{\rm p} &= I_{\rm bias}' R_{\rm p}' & (9)\\ I_{\rm bias} Q_L \omega L &= I_{\rm bias}' Q_L' \omega' L' & (10)\end{aligned}$$

Therefore, the condition to realize better FoM by the multiple-divide technique is as follows.

$$\begin{aligned} FoM' &< FoM & (11)\\ f_0' &= N f_0 & (12)\end{aligned}$$

$$\begin{aligned} \frac{P_{\rm total}'}{N I_{\rm bias}'^2 {Q_L'}^3 L'} &< \frac{P_{\rm total}}{I_{\rm bias}^2 {Q_L}^3 L} & (13)\\ \frac{P_{\rm VCO}' + P_{\rm divider}}{P_{\rm total}} &< \frac{N I_{\rm bias}'^2 {Q_L'}^3 L'}{I_{\rm bias}^2 {Q_L}^3 L} & (14)\\ \frac{P_{\rm VCO}' + P_{\rm divider}}{P_{\rm total}} &< \frac{Q_L' L}{N Q_L L'} & (15)\end{aligned}$$

where $P_{\rm divider}$ is the power consumption of frequency divider, $P_{\rm VCO}$ is the power consumption of VCO, and $P_{\rm VCO}'$ is the power consumption of VCO oscillating at N-times higher frequency. $I_{\rm bias}'$, Q_L' and L' are bias current, quality factor, and inductance of VCO using the multiple-divide technique. Eq. (15) provides power-consumption requirement to realize better FoM by the multiple-divide technique.

B. Trade-Offs in On-Chip Spiral Inductors

It is quite difficult to realize high-Q, *e*.g., more than 50, inductors at the present CMOS processes, because there are several trade-offs in designing on-chip spiral inductors. Quality factor of spiral inductors on Si substrate is limited by low metal resistivity and substrate loss. Basically, to obtain the highest quality factor, the optimal structure is unique for each frequency due to limited design parameters in CMOS processes. On the other hand, at higher frequencies, higher-Q inductors can be obtained.

From the aspect of layout design, diameter, line width, line space and a number of turns are the most common design parameters of on-chip spiral inductors. In addition, there are several options, *e*.g., symmetrical/asymmetrical patterned ground shield, multi-layer, etc. From the aspect of fabrication process, the following conditions have influence on inductor characteristics; metal thickness, metal resistivity, dielectric thickness, dielectric permittivity/loss, substrate structure, substrate conductivity/permittivity, permeability of each material, etc.

The number of turns of spiral inductor has a trade-off between layout area and mutual inductance. In CMOS chips, huge layout of spiral inductors, *e*.g., 500 μm $\times$ 500 μm is not preferable due to fabrication cost. On the other hands, inner spiral trace degrades mutual inductance per line length because magnetic flux penetrating the metal trace is counteracted by eddy current as known as Lenz's law. Thus, many numbers of turns are not preferable. In addition, the diameter also has a trade-off, and it is determined by the number of turned and required inductance.

The line space of spiral inductor should be minimized to reduce mutual inductance. Line-to-line capacitance is usually small because of thin metal thickness. Wider metal can improve resistive loss of spiral metal while it has larger parasitic capacitance between metal and substrate. The parasitic capacitance lowers self-resonance frequency, which also degrades peak quality factor. The wider metal also causes degradation of mutual inductance per length.

Quality factor of peak frequency can be simply obtained by the following equation.

$$Q_{\rm peak} = \frac{\omega_{\rm peak} L(\omega_{\rm peak})}{R} \tag{16}$$

$Q_{\rm peak}$ is the peak quality factor. $\omega_{\rm peak}$ is the peak frequency where quality factor has the highest value. $L(\omega_{\rm peak})$ is inductance at the peak frequency, and R is series resistance of inductor. When smaller inductance is used, self-resonance frequency ω_{SR} becomes higher as follows.

$$\omega_{SR} = \frac{1}{\sqrt{LC_L}} \tag{17}$$

where C_L is parasitic capacitance of inductor, and C_L is almost proportional to L because it is also proportional to line length ℓ. This relationship can be expressed by the following equations.

$$L = \quad k_L \ell \tag{18}$$

$$C_L = \quad k_C \ell \tag{19}$$

$$R = \quad k_R \ell \tag{20}$$

where k_L, k_C, k_R are proportional constants of inductance, capacitance, and resistance, respectively. The following equation can be derived.

$$Q_{\rm peak} = \frac{k_R}{\ell} \cdot \frac{\sqrt{k_L}}{\sqrt{k_C}} \tag{21}$$

k_R and k_C are almost constant, and k_L depends on the layout structure. At higher frequencies, k_L can be improved due to less numbers of turns, and line length ℓ is also shortened. Therefore, at higher frequencies, higher-Q inductors can be obtained.

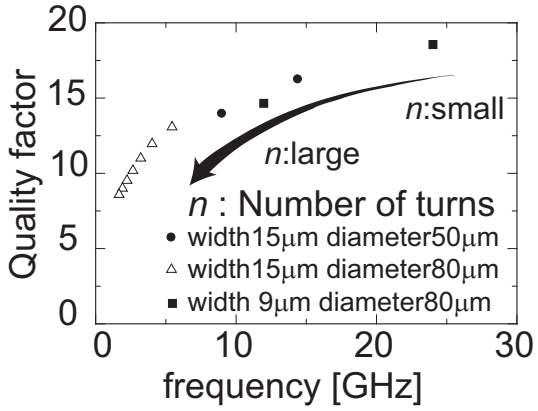

Fig. 4. Quality factor.

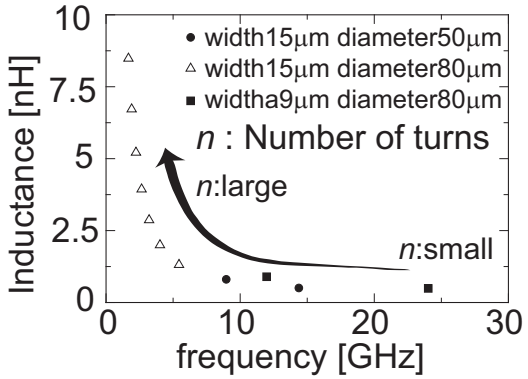

Fig. 5. Inductance corresponding to the structure in Fig. 4.

C. Frequency Divider

In this work, a ring-type ILFD is employed as shown in Fig. 3. The ring ILFD has wider locking range, which can be tuned by bias current. The ILFD can theoretically operate as a by-2, by-3, by-4 frequency divider. Power consumption of ILFD is determined by output oscillation frequency of ILFD, so power consumption can be kept very small even at higher input frequencies.

III. Simulation Results

Figure 4 shows quality factors at various structural configurations, which are derived from a commercial PDK for a CMOS process. The result reveals the optimum structure for each frequency. Figure 5 shows inductance corresponding to each structure in Fig. 4. The configurations of spiral inductors are 9 or 15 μm line width and 50 or 80 μm inner diameter. The number of turns is varied according to the required inductance. As shown in Fig. 4, the maximum quality factor becomes higher at higher frequencies, and improvement of phase noise can be expected.

To achieve lower phase noise, not only quality factor but also inductance have to be increased so that $Q_L^3 L$ is maximized

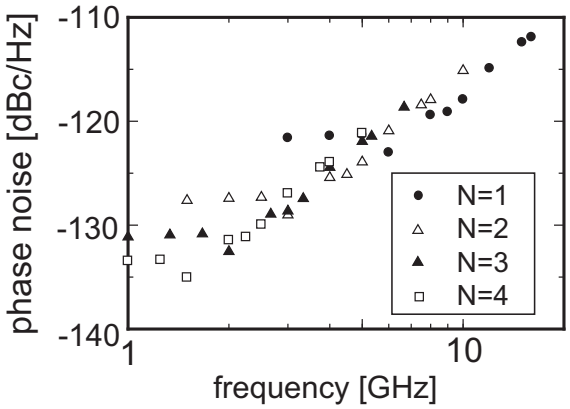

Fig. 6. Phase noise at 1-MHz offset.

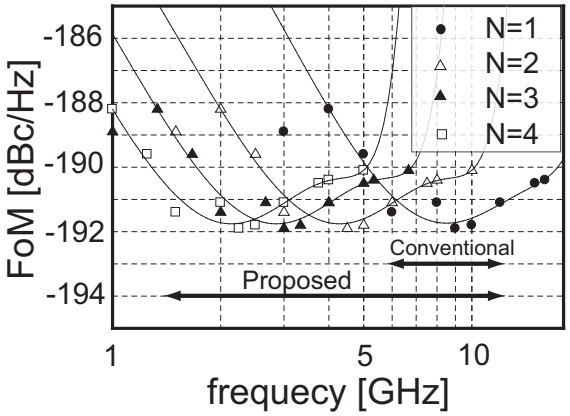

Fig. 7. Comparison of FoM.

as explained in Eq. (15). Thus, there is a suitable inductance for each frequency.

Next, simulated VCO performances are shown. A commercial 90-nm CMOS model parameter set is utilized. Figures 6 and 7 show phase noise and FoM of VCOs using the multiple-divide frequency divider. In Fig. 6, oscillation frequency of VCO is N-times higher than divided frequency. VCO and divider are optimally designed for each frequency.

Figure 7 is a normalized result, which shows intrinsic performance as a synthesizer. There is the optimum frequency range, which achieves better phase noise characteristics. In Fig. 7, non-divided oscillation, $N = 1$, has the optimum frequency range of 6$\sim$12 GHz, achieving better than -191 dBc/Hz of FoM. The range can be expanded by the proposed multiple-divide technique, and it becomes 1.5$\sim$12 GHz as shown in Fig. 7.

Figure 8 shows a phase-noise comparison between the conventional non-divided oscillation at 3 GHz, divide-by-3 oscillation at 3 GHz, and base oscillation at 9 GHz. Theoretically, the base oscillation at 9 GHz has 9 dB higher phase noise than the divide-by-3 oscillation at 3 GHz. At lower offset frequencies, $1/f$ noise can be considerably improved as compared with the conventional approach. Table I shows the summary of simulated results at 3 GHz of output. Phase

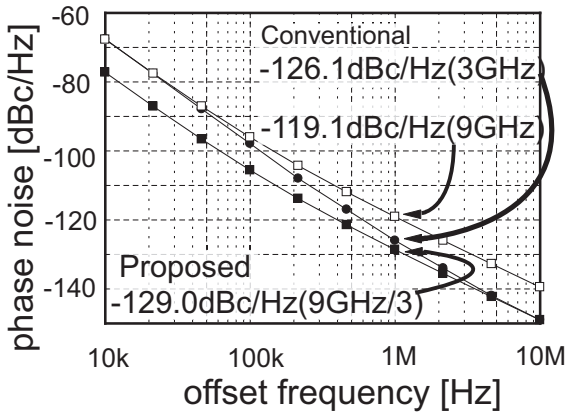

Fig. 8. Phase noise at 3 GHz frequency.

TABLE I
SUMMARY OF DESIGN RESULTS.

divide-by-#	not-divided	2	3	4
oscillation frequency f_0 [GHz]	3	6	9	12
phase noise at f_0 [dBc/Hz]	-126.1	-123.0	-119.1	-114.9
phase noise at 3 GHz [dBc/Hz]	-126.1	-129.0	-128.6	-127.0
$20 \log N$ [dBc/Hz]	+0	+6	+9	+12
$P_{\rm VCO}$ [mW]	4.0	5.3	4.2	3.5
$P_{\rm divider}$ [μW]	55.1	55.1	55.1	55.1
FoM [dBc/Hz]	-189.9	-191.4	-191.9	-191.1

noises at 1-MHz offset are listed in Table I. According to the result, divide-by-3 is the best choice to realize low-phase-noise VCO.

IV. CONCLUSIONS

This paper proposes the multiple-divide technique using by-2, by-3, and by-4 frequency dividers to realize a lower phase-noise LC-VCO. The simulated results, using 90-nm CMOS model parameters, reveals the design space of multiple-divide VCOs. In the results, the optimum frequency range, achieving better than -191 dBc/Hz of FoM, can be extended from 6 GHz-12 GHz to 1.5 GHz-12 GHz. The proposed multiple-divide technique can provide a lower phase-noise, lower power consumption, smaller layout area LC-VCO.

ACKNOWLEDGEMENT

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