PAPER Special Section on Analog Circuit Techniques and Related Topics

A Performance Model for the Design of Pipelined ADCs with Consideration of Overdrive Voltage and Slewing

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SUMMARY This paper proposes a performance model for design of pipelined analog-to-digital converters (ADCs). This model includes the effect of overdrive voltage on the transistor, slewing of the operational amplifier, multi-bit structure of multiplying digital to analog converter (MDAC) and technology scaling. The conversion frequency of ADC is improved by choosing the optimum overdrive voltage of the transistor, an important consideration at smaller design rules. Moreover, multi-bit MDACs are faster than the single-bit MDACs when slewing occurs during the step response. The performance model of pipelined ADC shown in this paper is attractive for the optimization of the ADC's performances.

key words: *analog to digital converter, pipeline operation, switched capacitor amplifier, low voltage operation, overdrive voltage*

1. Introduction

Together with the progress of digital systems the demand for high-performance analog-to-digital converters (ADCs) has increased. Pipelined ADCs especially have the ability to adapt to high performance communication applications such as digital television, WLAN, and ADSL, and so on. The key feature of pipelined ADCs is a relatively high conversion frequency at low power consumption. The conversion frequency and power consumption are dominated by the performance of the multiplying digital-to-analog converter (MDAC) as shown in Fig. 1 [1]. Moreover, recent technology scaling has made the design of MDAC a demanding issue, mainly due to the low-voltage operation. In order to maintain a high signal to noise ratio (SNR) despite the smaller signal swing a larger capacitance is required. This, however, leads to an increased current-consumption for the same gain bandwidth (GBW). Thus, it becomes more difficult to reduce the figure of merit (FoM) for high resolution pipelined ADCs.

Reference [2] reported the effect of technology scaling on the performance of pipelined ADCs. This performance model is attractive for estimating the performance of pipelined ADCs in conventional or future technology. However, the following influences were not considered in [2]:

1) The MDAC implementation in [2] is only single-bit per stage. The multi-bit MDAC structure can decrease number of MDAC in the ADC. This leads to the possibility of low power consumption and area saving. However, because the GBW of the multi-bit MDAC is decreased, it is difficult to use it at a high conversion frequency. Thus, this paper proposes a performance model of the multi-bit MDAC enabling a greater understanding between the benefits and tradeoffs made when choosing between single and multi-bit MDAC.

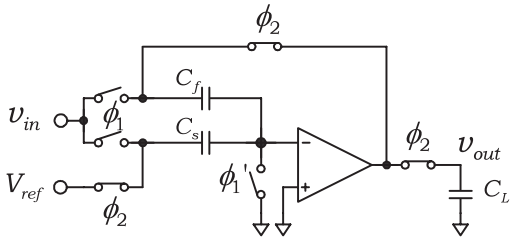

Fig. 1 A pipelined ADC's multiplying digital-to-analog converter.

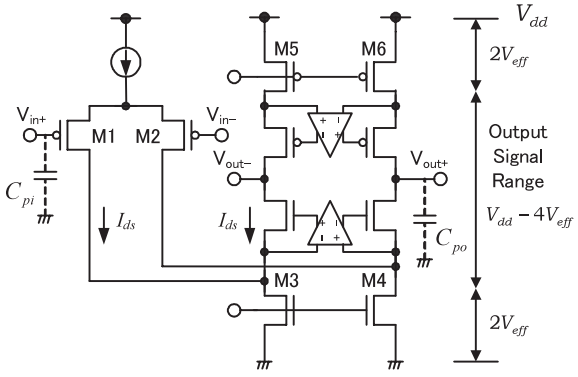

Fig. 2 Conventional OpAmp for a pipelined ADC.

2) The settling time includes the slewing time of the operational amplifier (OpAmp). However, the settling time reported in [2] assumed that the time of slewing is one third of the settling time without slewing. It is difficult to exactly calculate the settling time with slewing, but good approximations can be made in this paper.

3) The performance model in [2] assumes that the overdrive voltage of the transistor V_{eff} ($= V_{gs} - V_{th}$) is a constant value. In conventional design, V_{eff} is fixed between 0.15 V and 0.2 V because parasitic capacitance of a transistor increases with decreasing of V_{eff}. However, to increase signal swing by reducing the V_{eff} might be more advantageous in small design rule and low voltage design [3]. Reference [3] designed V_{eff} = 0.09 V in 90 nm CMOS and good FoM.

In this paper, a performance model of pipelined ADCs is proposed including the effect of the technology scaling, the multi-bit configuration of the MDAC and slewing of the operational amplifier. In addition, we confirm the influ-

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ence of the variance of V_{eff} on the performance of pipelined ADCs.

2. MDAC Implementation

Since the conversion frequency and most of the power consumption of pipelined ADCs are determined by the MDAC, it is most important to estimate the performance of the MDAC. An implementation of the MDAC to be analyzed in this paper is shown in Fig. 1. The MDAC consist of the OpAmp, sampling capacitors and switches. To simplify the analysis, we consider M bits per stage of the MDAC ($M = 1$, 2, 3, ...). In practice, M bits per stage of the MDAC is implemented with redundancy (e.g., 1.5 bit per stage), but the assumption of M bits per stage simplifies the explanation of our performance model.

During the sampling phase, the analog input is sampled into the sampling capacitors C_s and C_f. In the amplifying phase, C_s is connected to the reference voltage V_{ref}, whereas C_f forms the negative feedback loop around the OpAmp. C_s and C_f are given as multiples of the first stage's unit capacitance, C_o: $C_f = C_o$ and $C_s = mC_o$. The gain of the MDAC, G_{MDAC}, is given by

$$G_{MDAC} = m + 1 = 2^M \tag{1}$$

The sampling capacitor of the second stage equals the total sampling capacitor of the first stage MDAC divided by the gain of the first stage MDAC. This equals C_o since the total sampling capacitor is $(m+1)C_o$ and the gain of the first stage is $(m + 1)$. Therefore C_L in Fig. 1 equals to C_o.

2.1 Operational Amplifier

Figure 2 shows a conventional OpAmp for pipelined ADCs. A four-transistor stack is needed to form a folded cascode circuit which is inevitable for realizing a high voltage gain. If the voltage gain is not enough, gainboosting amplifiers are required to increase the gain.

The minimum drain-to-source voltage V_{ds} that keeps the transistor in the saturation region is V_{eff}. Therefore, the maximum signal swing V_{sig} is

$$V_{sig} = V_{dd} - 4\,V_{eff} \tag{2}$$

An OpAmp has parasitic input and output capacitances, C_{pi} and C_{po}. These capacitors are very important factors in estimating the performance of the MDAC.

2.2 Sampling Capacitance

Sampling capacitors C_s and C_f are very important factors in the pipelined ADC because these capacitors affect the resolution, the conversion frequency, power consumption and the layout area. In practical design capacitors are determined by the capacitance mismatch and the thermal noise. This analysis assumes that a digital error compensation technique is used for capacitance mismatch [4], therefore sampling capacitors are determined by the required signal to noise ratio (SNR). The noise of the switch resistance and the OpAmp are considered separately.

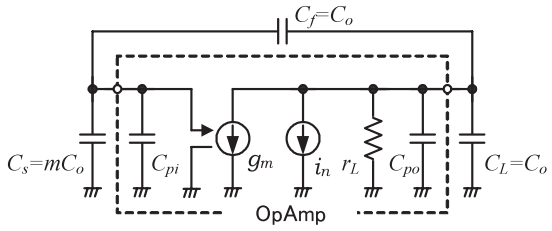


Fig. 3 The equivalent circuit of the MDAC shown in Fig. 1.

(a) Switch resistance noise
The switch resistance noise is sampled into C_s and C_f during the sampling phase. The noise charge q_n caused from switch resistance is given by

$$\overline{q_n^2} = \left(C_s + C_f\right)^2 v_{rn}^2 = kT \cdot (m+1)\, C_o \tag{3}$$

where v_{rn} is the noise voltage of the switch resistance, k is the Boltzmann constant and T is the absolute temperature. The noise charge is transferred to the feedback capacitor C_f. As a result, noise voltage of the output node is given by

$$\overline{v_{nsw}^2} = (m+1)^2 \frac{kT}{C_{s\_tot}} \tag{4}$$

where C_{s_tot} $(= C_s + C_f)$ is total sampling capacitance.

Since the MDAC has a gain of $(m + 1)$, input-referred noise is calculated as

$$\overline{v_{nsw\_in}^2} = \frac{kT}{C_{s\_tot}} \tag{5}$$

As a result, input-referred noise does not depend on multi-bit number m but depend on only the total sampling capacitance C_{s_tot}. The value of the total sampling capacitor of the next stage is assumed equals divided by the gain of the previous stage. Thus total input-referred noise is twice (5).

(b) OpAmp noise
Figure 3 shows the equivalent circuit of the MDAC for the OpAmp noise estimation. The equivalent circuit can be modeled using the sampling capacitors C_s and C_f, the parasitic input and output capacitors C_{pi} and C_{po}, the trans-conductance g_m, and the output impedance r_L of the OpAmp. The output noise of the OpAmp is given by

$$\overline{v_{n\_op}^2} = \frac{\overline{i_n^2}}{(g_m\beta)^2 + \left(\omega C_{eff}\right)^2} \tag{6}$$

with

$$\overline{i_n^2} = \frac{8}{3} n \cdot \gamma \cdot kT g_m \tag{7}$$

$$\beta = \frac{1}{(m+1) + \dfrac{C_{pi}}{C_o}} \tag{8}$$

and

$$C_{eff} = C_{po} + \left(1 + \frac{m + \frac{C_{pi}}{C_o}}{(m+1) + \frac{C_{pi}}{C_o}}\right) C_o \tag{9}$$

where n is the number of noise current source (e.g. telescopic type: $n = 2$, folded cascode type: $n = 4$), γ is the coefficient of the noise. The output noise is given in the form of the following integral,

$$v_{n\_op}^2 = \int_0^\infty \frac{i_n^2}{(g_m\beta)^2 + (\omega C_L)^2} df = \frac{2n\gamma \cdot kT}{3\beta C_L} \tag{10}$$

The input-referred noise of (10) is almost entirely determined by the total sampling capacitance. Finally, total input-referred thermal noise of the pipelined ADC is given by the sum of (5) and (10).

This analysis assumed that $n = 4$, $\gamma = 2$, $T = 400\,\mathrm{K}$, $C_s = C_{pi}$ and fully differential operation. Therefore input-referred thermal noise of the pipelined ADC is given by

$$v_{nin\_tot}^2 \approx \frac{16kT}{C_{s\_tot}} \tag{11}$$

(c) Capacitance requirement
As the input-referred thermal noise obtained from (11) should be equal to or less than the quantization noise to attain an SNR that is 3 dB lower than the ideal value, the following equation holds:

$$\frac{16kT}{C_{s\_tot}} \le \frac{1}{12}\left(\frac{V_{pp}}{2^N}\right)^2 \tag{12}$$

where V_{pp} is the maximum signal swing when the OpAmp is operating fully-differentially. Since V_{pp} is twice (2), total sampling capacitance of the first stage MDAC is given by

$$C_{s\_tot}\,(pF) \ge 2.66 \times 10^{-7}\left(\frac{2^N}{V_{dd} - 4\,V_{eff}}\right)^2 \tag{13}$$

The total sampling capacitance depends on not only V_{dd} but also V_{eff}.

3. Small Signal Analysis for Multi-Bit MDAC

The equivalent circuit of the multi-bit MDAC as shown in Fig. 3 can be used to obtain the gain-bandwidth of the multi-bit MDAC. To simplify the gain-bandwidth, we assume that $g_m r_L \gg 1$ and $i_n = 0$.

The closed loop gain bandwidth of the multi-bit MDAC is given by

$$GBW_{\_closed} = \frac{g_m}{2\pi C_{eff}}\beta \tag{14}$$

Equation (14) can be modified to

$$GBW_{\_closed} = \frac{g_m}{2\pi C_o} \frac{1}{\left((m+1)+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(m+\frac{C_{pi}}{C_o}\right)} \tag{15}$$

The parasitic input and output capacitances, C_{pi} and C_{po} are proportional to the channel width of the MOS transistors. If the transistors are kept in the saturation region, the channel width W is obtained from the following equation.

$$W \approx \frac{2L}{\mu C_{ox} V_{eff}^2} I_{ds} \tag{16}$$

If the channel length L and V_{eff} are kept constant, C_{pi} and C_{po} are additionally proportional to the drain current.

Thus, $C_{pi} = \alpha_{pi} I_{ds}$ and $C_{po} = \alpha_{po} I_{ds}$. With $g_m \approx \frac{2I_{ds}}{V_{eff}}$, (15) can be modified to

$$GBW_{\_closed} = \frac{I_{ds}}{\pi C_o V_{eff}} \frac{1}{\left((m+1)+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(m+\frac{\alpha_{pi} I_{ds}}{C_o}\right)} \tag{17}$$

The settling time of the step response is obtained from (17). Moreover, conversion frequency of the pipelined ADC is estimated from the settling time. The closed loop gain-bandwidth of the MDAC decreases with increase of m. However, multi-bit MDAC doesn't always decrease conversion frequency of the pipelined ADC because as the gain of the MDAC is increased, the tolerance of the settling-error is increased. The detailed discussion of this reasoning is provided in the next section.

4. Settling Time of the MDAC with Slewing

It is necessary to consider the slew rate (SR) of the OpAmp for estimating the settling time of the step response [5]. Figure 4 shows the outline chart of the step response with and without slewing. The step response without slewing is obtained by

$$v_{out} = (m+1)\ V_{in}\left(1 - e^{-\frac{2I_{ds}\beta}{V_{eff}C_{eff}}t}\right) \tag{18}$$

The settling error margin is assumed less than ±1/4LSB of each resolution. When maximum input signal is input to the MDAC, the settling time without slewing is given by

$$t_{set1} = \frac{C_{eff}V_{eff}}{2I_{ds}\beta}\ln\left(\frac{2^{N+2}}{m+1}\right) \tag{19}$$

The settling time with slewing t_{set2} is obtained from sum of t_{slew} and t_{s_ns}. The time slewing has ended,

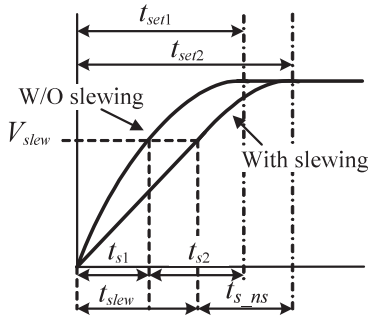


Fig. 4 The outline chart of the step response with and without slewing.

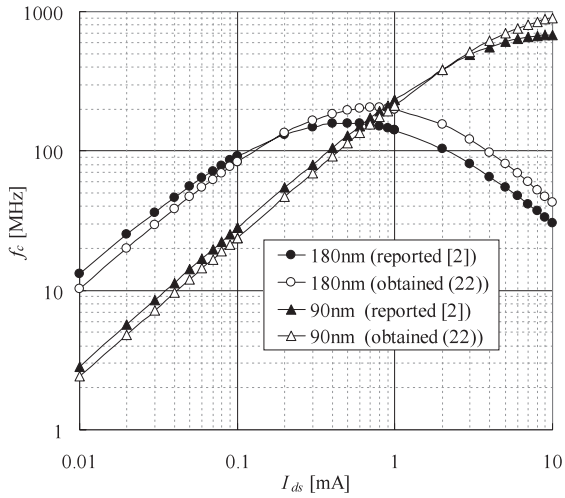


Fig. 5 The conversion frequency vs. I_{ds} obtained from (22) and reported [2]. (N=10 bit)

$$t_{slew} = \frac{C_{eff} V_{sig}}{I_{ds}} \left(1 - \frac{V_{eff}}{2V_{sig}\beta}\right) \tag{20}$$

The step response with and without slewing are assumed almost the same after the slewing has ended, $t_{s\_ns} \approx t_{s2}$ given by

$$t_{s\_ns} = t_{set1} - t_{s1} = \frac{C_{eff} V_{eff}}{2I_{ds}\beta} \ln\left(\frac{2^{N+2}}{m+1} \cdot \frac{V_{eff}}{2\,V_{sig}\beta}\right) \tag{21}$$

Finally, the settling time with slewing can be approximated as follow,

$$t_{set2} = t_{slew} + t_{s\_ns} \tag{22}$$

The condition that the slewing occurs is given by

$$\frac{V_{eff}}{2\,V_{sig}\beta} \leq 1 \tag{23}$$

The situations in which slewing can easily occur are as follows,

1) Small overdrive voltage V_{eff}.
2) Large signal swing V_{sig}.
3) Large feedback β.

The condition that the slewing occurs does not depend on C_{eff}. Because as GBW_closed decreases with an increase of C_{eff}, the requirement for the SR is decreased.

The conversion frequency as obtained from (22) and reported in [2] is plotted in Fig. 5. The conversion frequency is reciprocal of twice the settling time. Each parameter is shown in Table 1. These parasitic capacitances have been obtained by SPICE simulation for conventional foundry processes under the assumption that V_{eff} = 0.175 V, and the channel length being 1.1 times the minimum channel length.

The settling time reported in [2] assumed that the slewing occurs in all current regions and the time slewing has ended is 1/3 of the t_{set1}. However, with the condition that the slewing occurs depends on feedback factor β, the error reported in [2] is increased in low and high current region. For example, the error reported in [2] is about 10% in the 90 nm process and is about 30% in the 180 nm process. Because the signal swing V_{sig} in the 180 nm is larger than V_{sig} in the 90 nm, the influence of the slewing is larger in 180 nm process.

Table 1 Design rules, capacitances, and signal swing. ($@V_{eff}$=0.175 V)

DR [nm]	α_{pi} [fF/mA]	α_{po} [fF/mA]	C_{s_tot} [fF@10b]	V_{pp} [V]
350	1034	892	41	5.2
250	662	832	86	3.6
180	475	340	230	2.2
130	249	168	436	1.6
90	94	95	1116	1.0

5. The Effect of V_{eff} Scaling

5.1 Trans-Conductance g_m

When drain-source current I_{ds} is in the region of square-law characteristics, the trans-conductance g_m is given by

$$g_m \approx \frac{2I_{ds}}{V_{eff}} \tag{24}$$

However, the range where this approximation can be use is very narrow in modern CMOS technology. Because velocity saturation occurs, I_{ds} is proportional to V_{eff} in the large-V_{eff} region. Moreover, I_{ds} is close to a subthreshold behavior in low-V_{eff} region. Therefore, the range where (24) can use is around $0.15 < V_{eff} < 0.3$.

It is difficult to use large V_{eff} because signal swing depends on V_{eff}. Thus, a close approximation to g_m in low-V_{eff} region [6] should be used. The subthreshold behavior of I_{ds} in low-V_{eff} region is calculated by

$$I_{ds} = I_{dsws} \{\ln(1 + e^x)\}^2 \tag{25}$$

with

$$I_{dsws} = 2n\mu C_{ox} \frac{W}{L} U_T^2 \tag{26}$$

$$n = 1 + \frac{C_d}{C_{ox}} \tag{27}$$

$$U_T = \frac{kT}{q} \tag{28}$$

$$x = \frac{V_{eff}}{2nU_T} \tag{29}$$

where C_d is the depletion region capacitance and U_T is the thermal voltage. The characteristics between g_m and I_{ds} is obtained from (25)–(29) as follows,

$$g_m = \frac{I_{ds}}{nU_T\,(1 + e^{-x})\,\ln(1 + e^x)} \tag{30}$$

Moreover, (30) can be rewritten to $g_m = \frac{2I_{ds}}{V'_{eff}}$, the effective overdrive voltage V'_{eff} in subthreshold region is given by

$$V'_{eff} = 2nU_T\,(1 + e^{-x}) \ln(1 + e^x) \tag{31}$$

5.2 Parasitic Capacitance

The coefficients of the parasitic input and output capacitances, α_{pi} and α_{po} has been obtained in the case of V_{eff} = 0.175 V, as shown in Table 1. In this chapter, we obtain the coefficients of the parasitic capacitance α'_{pi} and $\alpha'_{o'i}$ with variance of V_{eff} as follows,

$$\alpha'_{pi} = \left(\frac{0.175}{V_{eff}}\right)^2 \alpha_{pi} \tag{32}$$

$$\alpha'_{po} = \left(\frac{0.175}{V_{eff}}\right)^2 \alpha_{po} \tag{33}$$

Thus, GBW_{closed} of the MDAC with variance of V_{eff} is given by

$$GBW\_{closed} = \frac{I_{ds}}{\pi C_o V'_{eff}} \cdot \frac{1}{\left((m+1)+\frac{\alpha'_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha'_{po} I_{ds}}{C_o}\right)+\left(m+\frac{\alpha'_{pi} I_{ds}}{C_o}\right)} \tag{34}$$

Equation (34) can be used to estimate the conversion frequency of the pipelined ADC with variance of V_{eff}.

6. Estimation of ADC Performances

6.1 Technology Scaling

Figure 6 shows the conversion frequency of the ADC obtained from (22) and (34) as a function of I_{ds} and V_{eff} in case of 180 nm process, V_{dd} = 1.8 V, N = 12 bit and m = 1. The conversion frequency includes the margin for non-overlapping clock and process variance. The time margin is assumed 20% of the sampling period obtained from (22) and (34). The optimum points for the conversion frequency exist as a function of not only I_{ds} but also V_{eff}.

1) V_{eff} has an optimum point effect on the conversion frequency. For example, if the drain current is kept at I_{ds} = 10 mA, the optimum conversion frequency for V_{eff} = 0.15 V is 138 MHz and for V_{eff} = 0.22 V is 196 MHz.

2) The optimum V_{eff} for the conversion frequency increases with the increase of I_{ds}. This is because when V_{eff} is constant, input parasitic capacitance C_{pi} increases with the increase of I_{ds}. Thus, the feedback factor β decreases with the increase of I_{ds} as shown in Fig. 7(a). To prevent the decrease of β, C_{pi} should be decreased by increasing V_{eff}. However, if V_{eff} is increased too much, the sampling capacitor becomes larger as shown Fig. 7(b). Therefore, V_{eff} has an optimum point for the conversion frequency in each I_{ds}.

Figure 8 shows the conversion frequency of 90 nm and 180 nm process in case of N = 10 bit and 12 bit. In the small-current region, the 180 nm process is faster than the 90 nm process. However, when V_{eff} is constant, the 90 nm process achieves higher conversion frequency with an increase of the I_{ds}. Moreover, in the small-current region, the 90 nm process becomes faster with a decrease of V_{eff}. Because parasitic capacitance of the 90 nm process is smaller than the 180 nm process, parasitic capacitance C_{pi} doesn't increase too much with a decrease of V_{eff}. Therefore, because signal

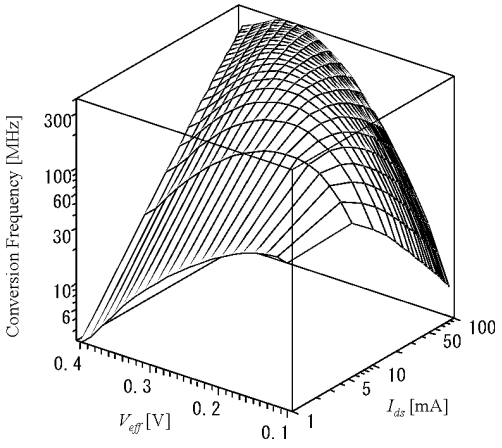
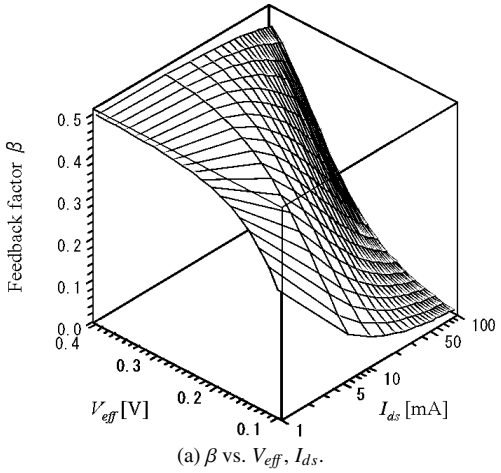
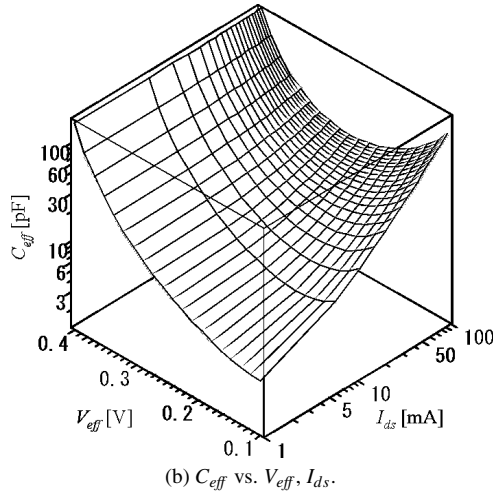


Fig. 6 The conversion frequency vs. V_{eff}, I_{ds}. (180 nm, N = 12 bit)

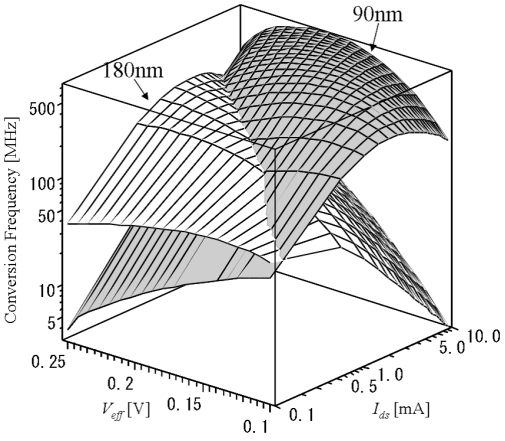


(a) β vs. V_{eff}, I_{ds}.

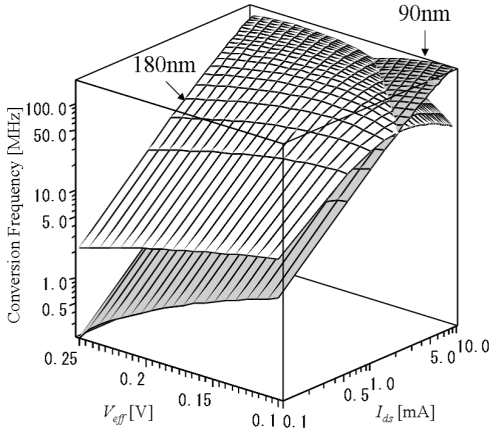


(b) C_{eff} vs. V_{eff}, I_{ds}.

Fig. 7 The feedback factor β and effective load capacitance C_{eff} vs. V_{eff}. (180 nm, V_{dd} = 1.8 V, N = 12 bit)

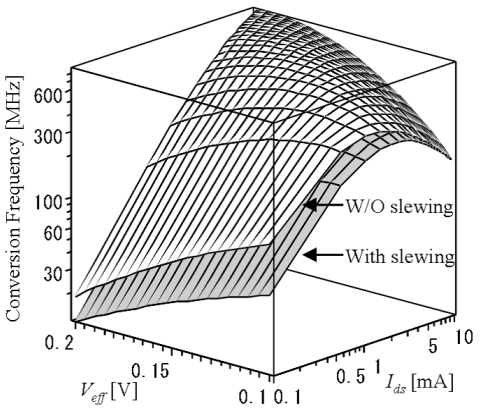


(a) $N = 10$ bit.

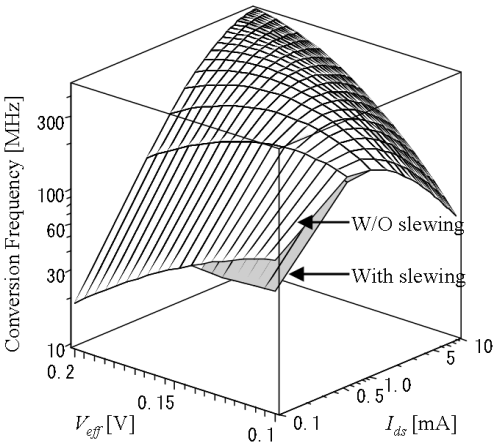


(b) $N = 12$ bit.

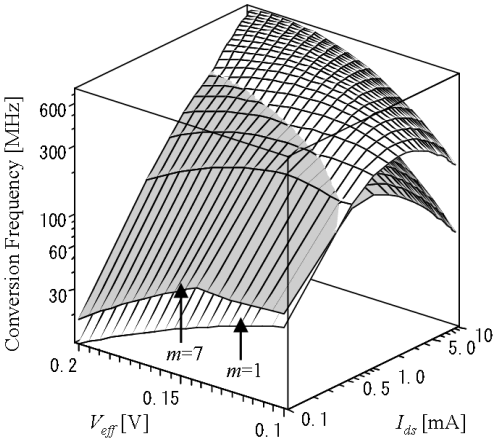
Fig. 8 The conversion frequency vs. V_{eff}, I_{ds}.



(a) 90 nm, $V_{dd} = 1.2$ V, $N = 10$ bit, $m = 1$.



(b) 90 nm, $V_{dd} = 1.2$ V, $N = 10$ bit, $m = 7$.



(c) 90 nm, $V_{dd} = 1.2$ V, $N = 10$ bit, $m = 1, 7$, with slewing.

Fig. 9 The conversion frequency with and without slewing vs. V_{eff}, I_{ds}.

swing increases with a decrease of V_{eff}, the decrease of V_{eff} can reduce the signal capacitance without the decrease of β. Additionally, g_m increase with the decrease of V_{eff} is a factor in the reason why the conversion frequency becomes higher. In case of $N = 12$ bit and $V_{eff} = 0.2$ V, 180 nm process should be used in all current regions. However, in case of $V_{eff} = 0.1$ V, 90 nm process achieves higher conversion frequency for $I_{ds} > 2$ mA. The sensitivity of V_{eff} to the conversion frequency increases with a smaller design rule. Therefore, it is more important to determine the V_{eff} in nano-scale and low voltage design.

6.2 Multi-Bit MDAC

Figure 9(a) shows the conversion frequency with and without slewing in case of 90 nm process, $V_{dd} = 1.2$ V, $N = 10$ bit and $m = 1$ (1 bit per stage). The conversion frequency with slewing is lower than without slewing because slewing occurs in all the regions.

There are two reasons why slewing occurs easily when V_{eff} is decreased. One reason is that the signal swing increases with a decrease of V_{eff}. Another reason is that the trans-conductance g_m increases with a decrease of V_{eff}. When g_m increases, the requirement of the SR of the OpAmp increases, but the SR of the OpAmp does not increase because I_{ds} is constant. From this analysis, when only for the ratio of t_{set1} and t_{set2} is taken into account, conversion frequency improvement by reducing V_{eff} is effective.

Figure 9(b) shows the conversion frequency with and without slewing in the case of 90 nm process, $V_{dd} = 1.2$ V, $N = 10$ bit, $m = 7$ (3 bit per stage). Slewing doesn't occur easily for $m = 7$ and the conversion frequency deterioration by the slewing is suppressed. The following reasoning may

reveal why multi-bit MDACs have tolerance to slewing.

The effective load capacitance C_{eff} decrease with increase of m. In case of $m = 7$, the sampling capacitance of the next stage is scaled to $C_o/8$ because the MDAC has a gain of 8. Thus, SR ($= 2I_{ds}/C_{eff}$) increases with increase of m. Moreover, because the feedback factor β of the multi-bit MDAC is smaller than the single-bit MDAC, slewing does not occur easily (see Eq. (23)).

Figure 9(c) shows the conversion frequency with slewing in case of $m = 1$ (1 bit per stage) and $m = 7$ (3 bit per stage). The multi-bit MDAC should be chosen in the small current region. However, since the maximum conversion frequency of single-bit MDAC is faster than that of the multi-bit MDAC, the single-bit MDAC should be chosen if higher conversion frequency is needed for an application.

7. Conclusion

To estimate the performance of a pipelined ADC, the influence of the design rule, the overdrive voltage of the transistor, the slewing of the OpAmp and multi-bit structure of the MDAC is investigated in this paper.

The slewing of the MDAC occurs easily when not only signal swing is large but also when the feedback factor is large. Therefore, the influence of slewing is large in the small-current region where deterioration in the feedback factor is small. The conversion frequency of an ADC is improved by determining the optimum overdrive voltage of the transistor. The signal capacitance and the parasitic capacitance of the OpAmp change by changing the overdrive voltage of transistor. Thus, the optimum point exists where the feedback factor balances the effective load capacitance C_{eff}. Since sensitivity of the overdrive voltage to the conversion frequency increases with a smaller design rule, it is more important to determine the overdrive voltage in nano-scale and low voltage design.

The influence of the slewing for single-bit and multi-bit MDAC was also investigated. Slewing rarely appears in multi-bit MDAC whose capacitive load and feedback factor are smaller than that of the single-bit MDAC.

The performance model of a pipelined ADC shown in this paper is attractive for the optimization of ADC's performances.

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