A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs

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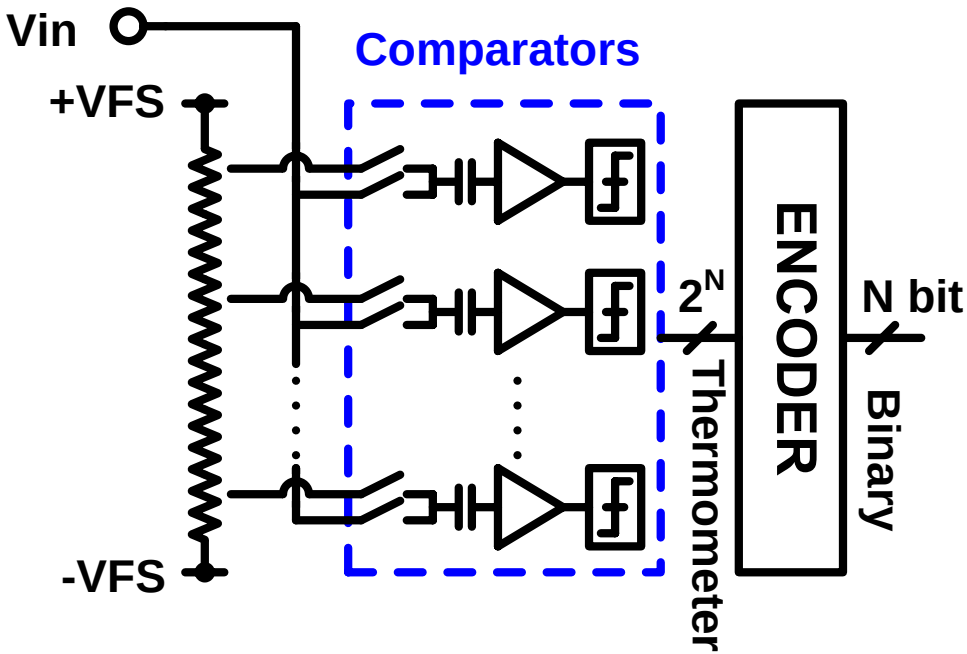
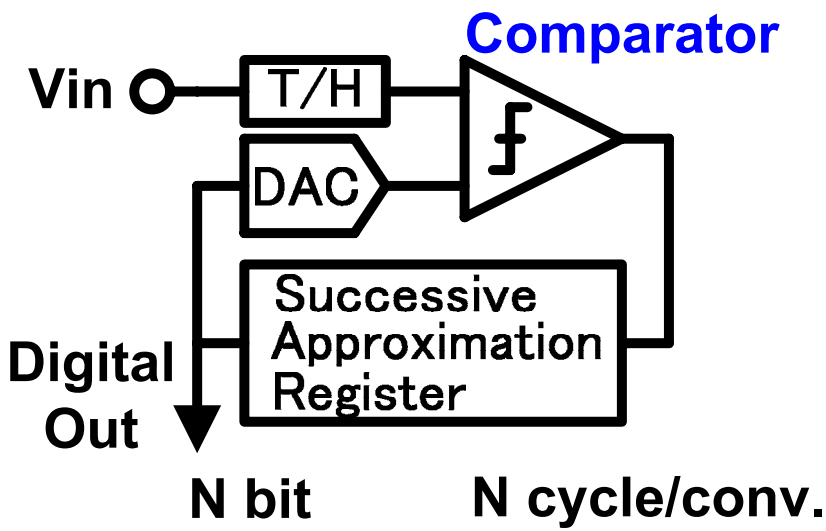
Outline

- Motivation
- The Calibration Scheme
- Proposed Comparator
- Measurement Results
- Conclusions

Motivation (I)

Comparator performance is important in comparator based ADCs.



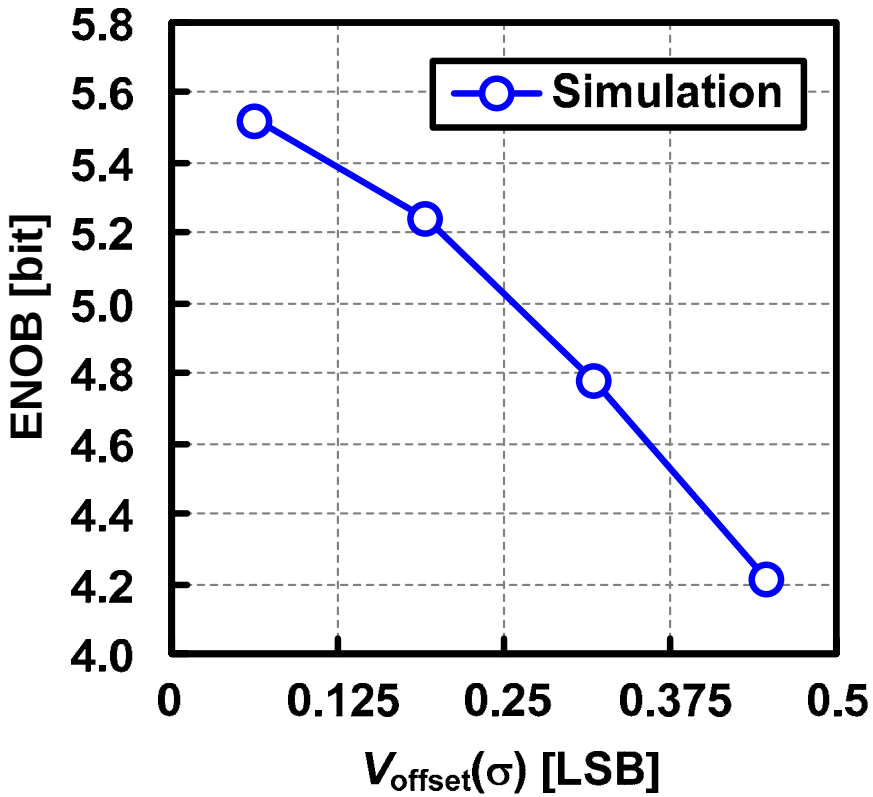


Comparator offset
⇒Low linearity
⇒Low SNDR

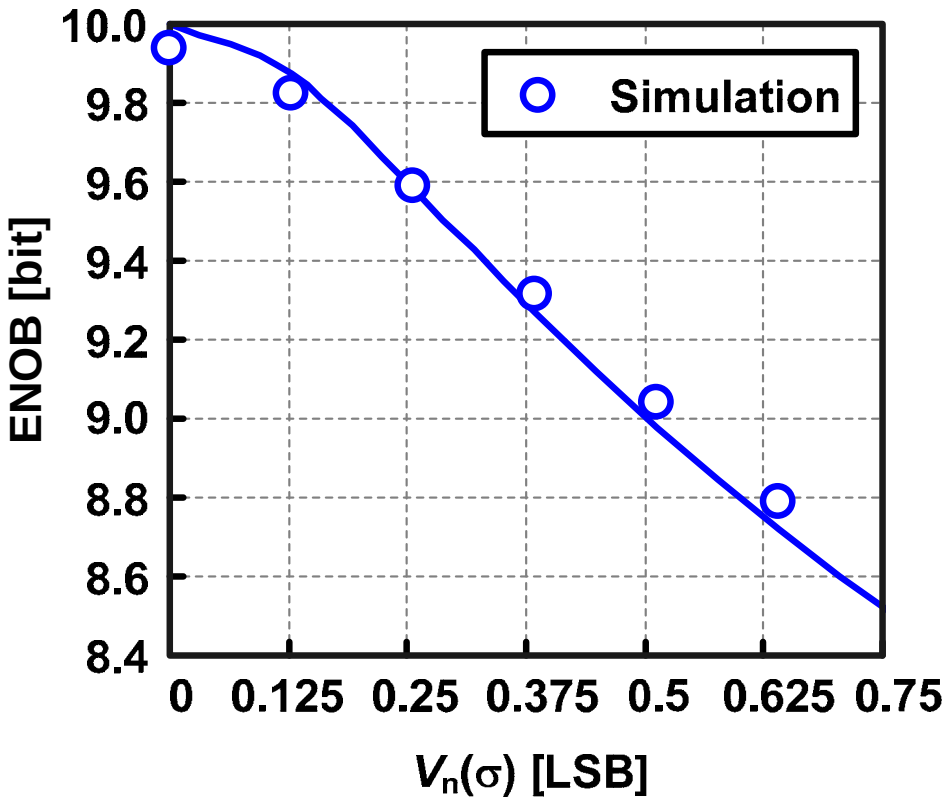
Comparator noise
⇒Low SNR

Motivation (II)

6bit Flash ADC



10bit SAR ADC

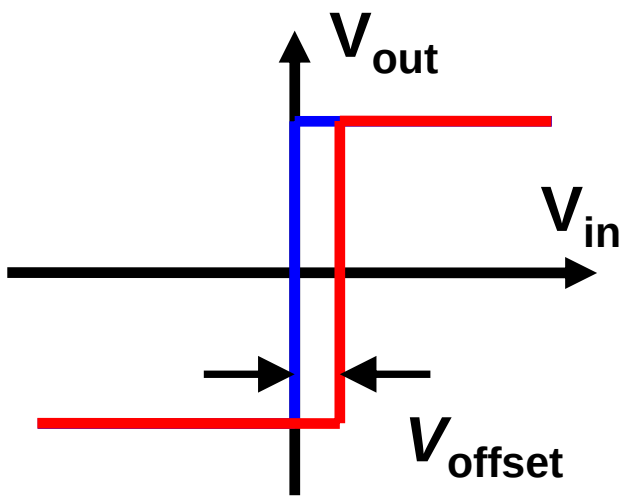


1bit down @$V_{offset}(\sigma)$ = 1/4 LSB

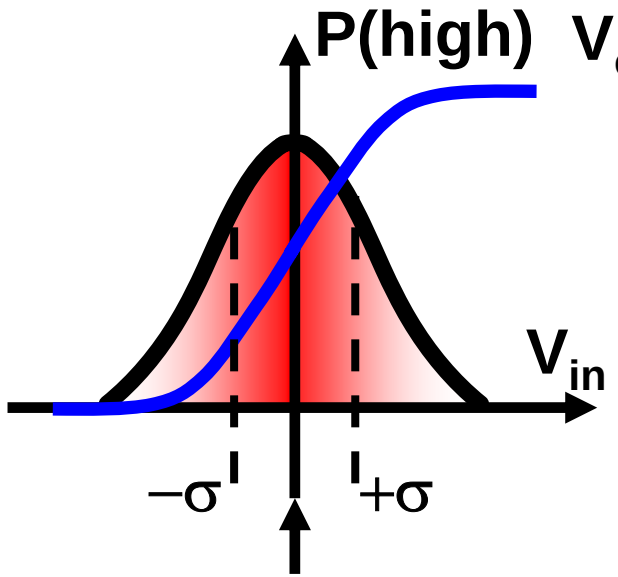
1bit down @$V_n(\sigma)$ = 1/2 LSB

Comparator Design Challenges

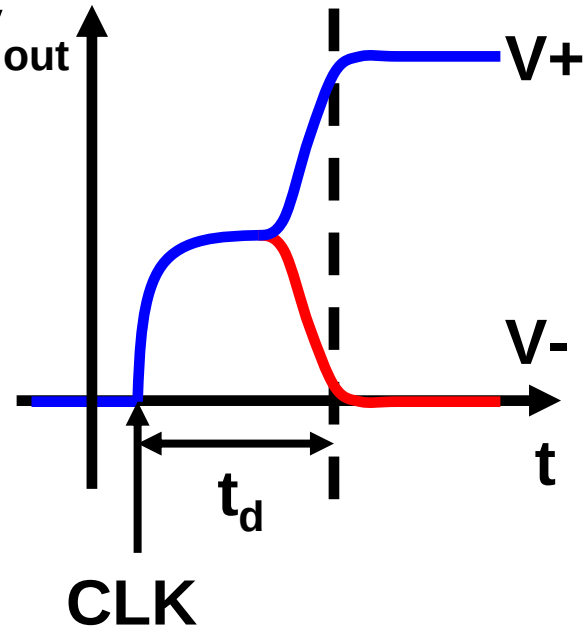
- **Offset Voltage**



- **Sensitivity**



- **Speed & Power**



- **Transistor mismatch**
- **Parasitic capacitance**
- **Transistor Noise**
- **Circuit topology**
- **Transistor size**

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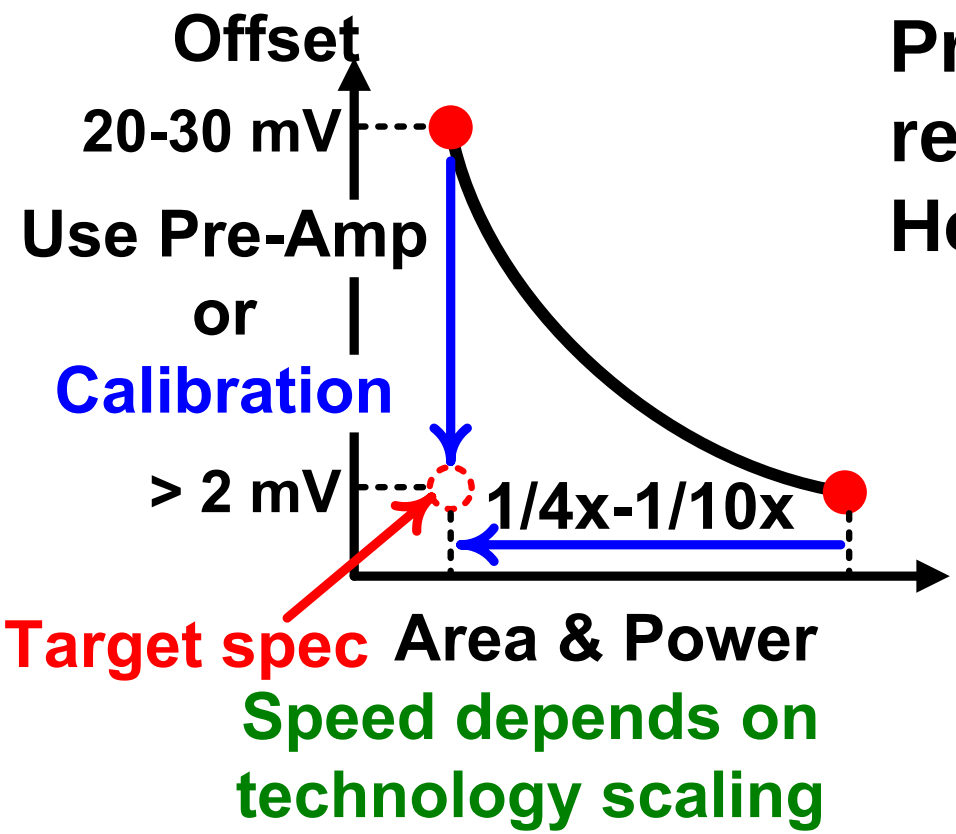
Design Concept

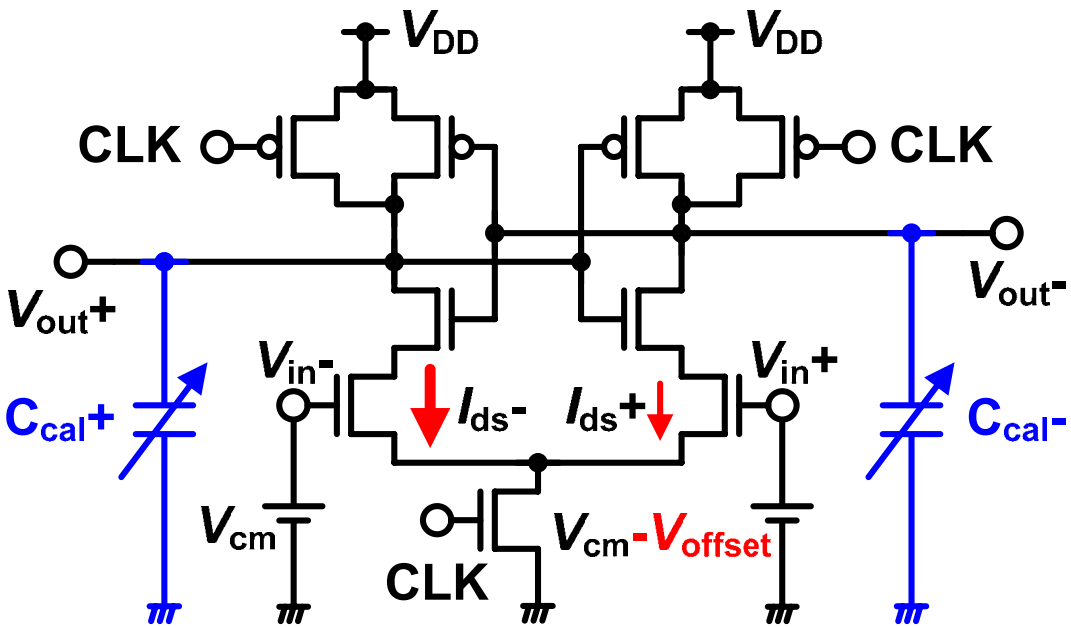


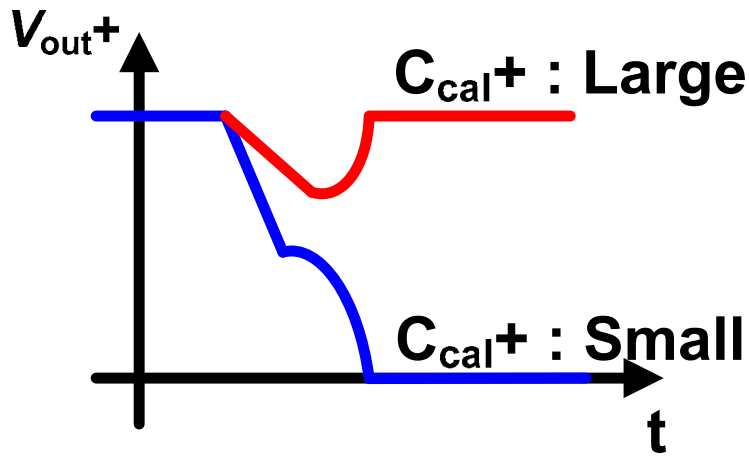
Pre-amplifiers are used to reduce to offset voltage. However…

- **High DC gain (> 10x)**
  => Difficult in deep sub-micron CMOS
- **Wide bandwidth (> 1 GHz)**
  => Large power consumption

Offset calibration techniques are more suitable in deep sub-micron CMOS design.

Conventional Offset Calibration





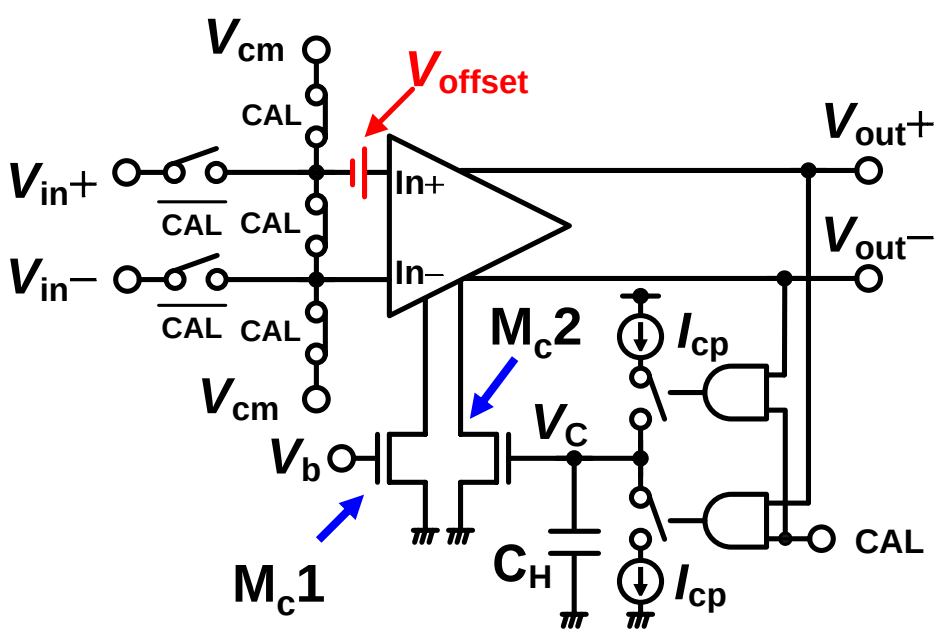
$$V_{offset} \propto \frac{\Delta C_L}{\Delta I_{ds}}$$

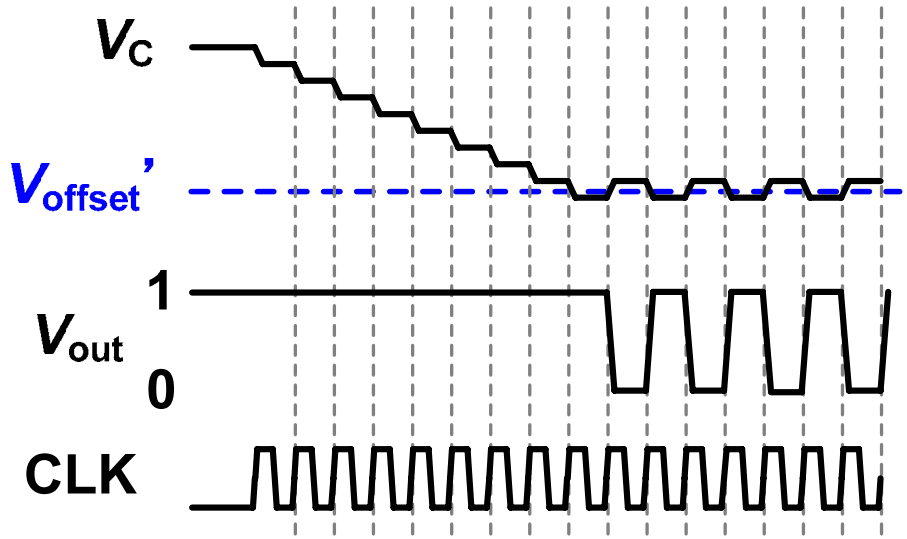
[2] G. Van del Plas et al. ISSCC 2006

Advantage: Dynamic circuit, no static power.

Drawbacks: Accuracy is limited by the resolution of C_{cal}.
Latch speed is slowed down.

Proposed Offset Calibration





$$V_{offset} \propto \frac{\Delta C_L}{\Delta I_{ds}}$$

Advantages: During the conversion mode, no static power.
Wide compensation range.
The resolution is variable by changing I_{cp}.

Drawback: Charge pump circuit must refresh C_H frequently.

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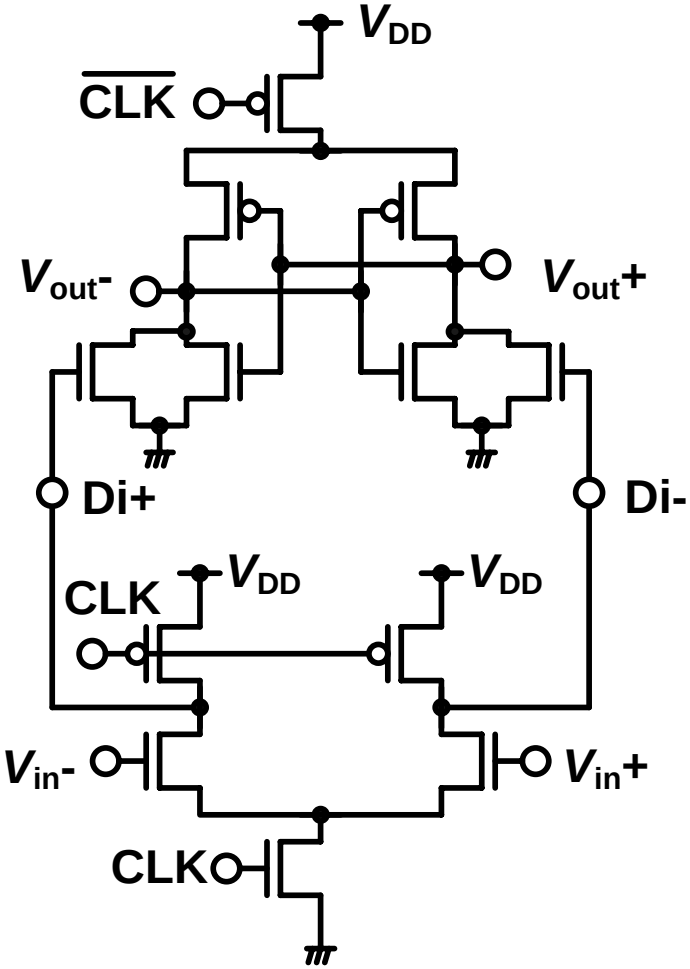
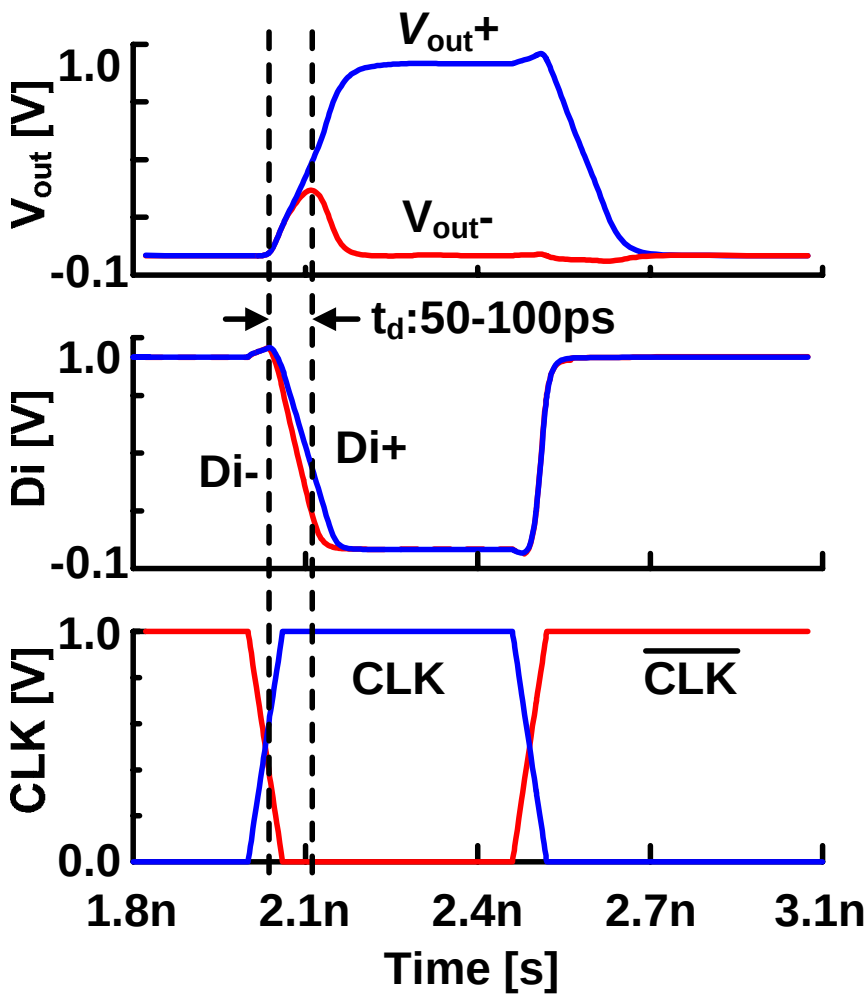
Double-Tail Latched Comparator

The 2nd latch stage has to detect ΔV_{Di} in a very short time.

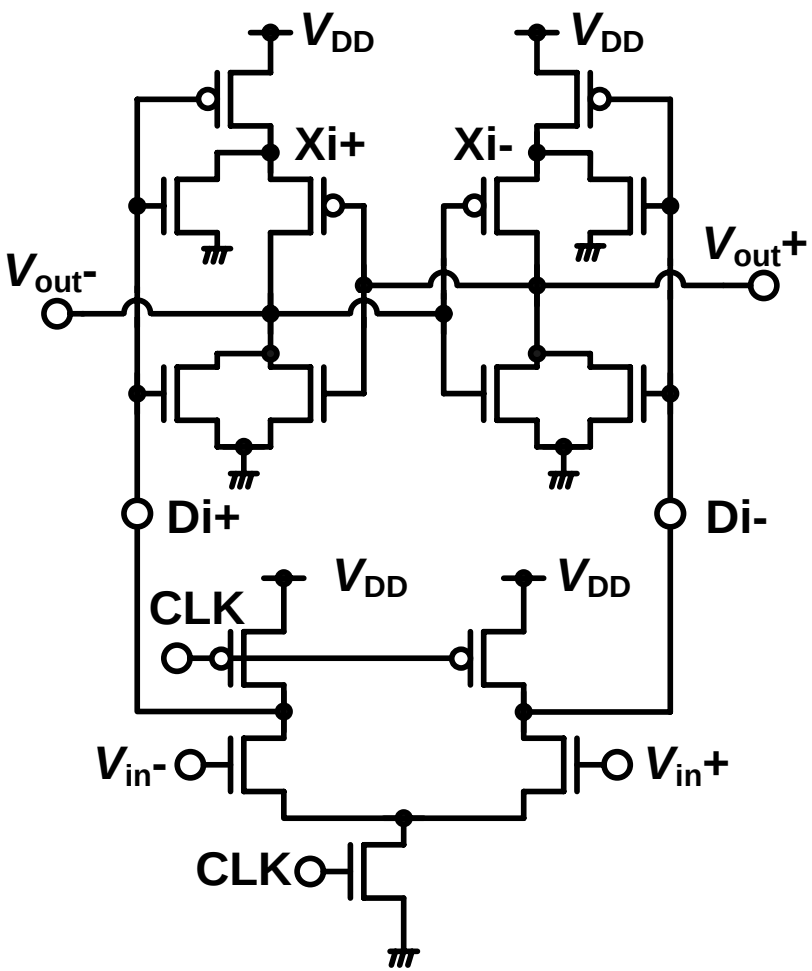


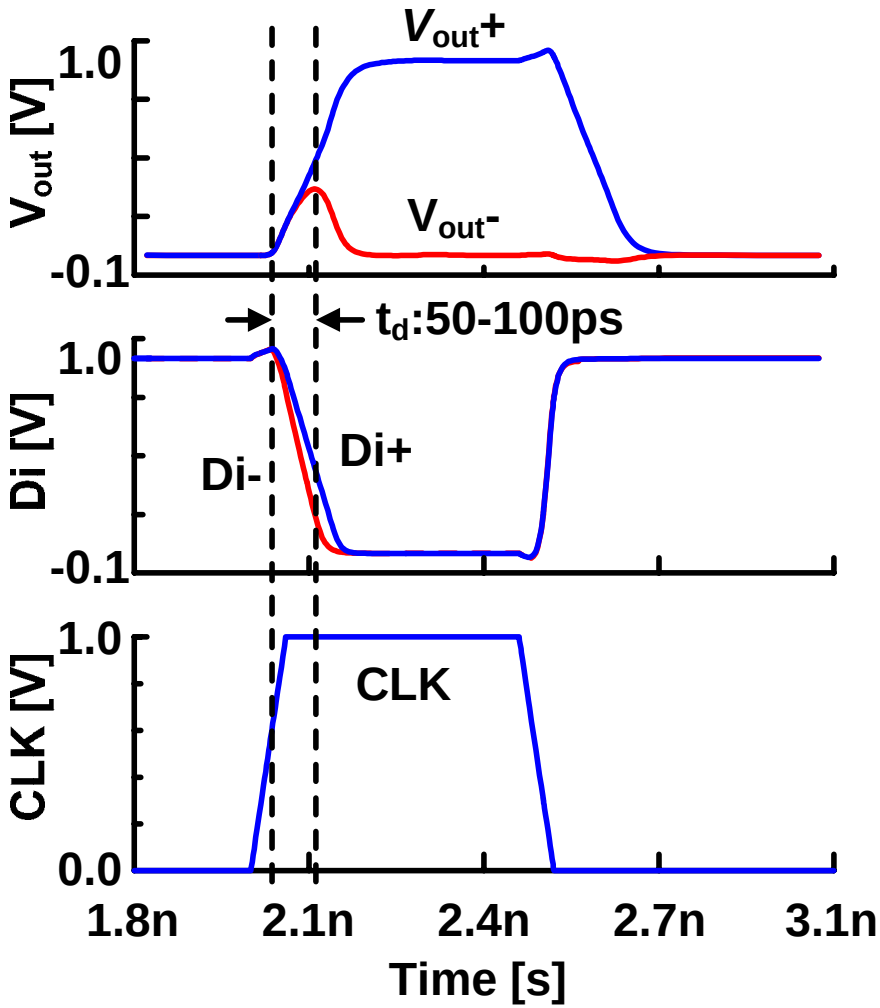
[4]D. Schinkel et al. ISSCC 2007



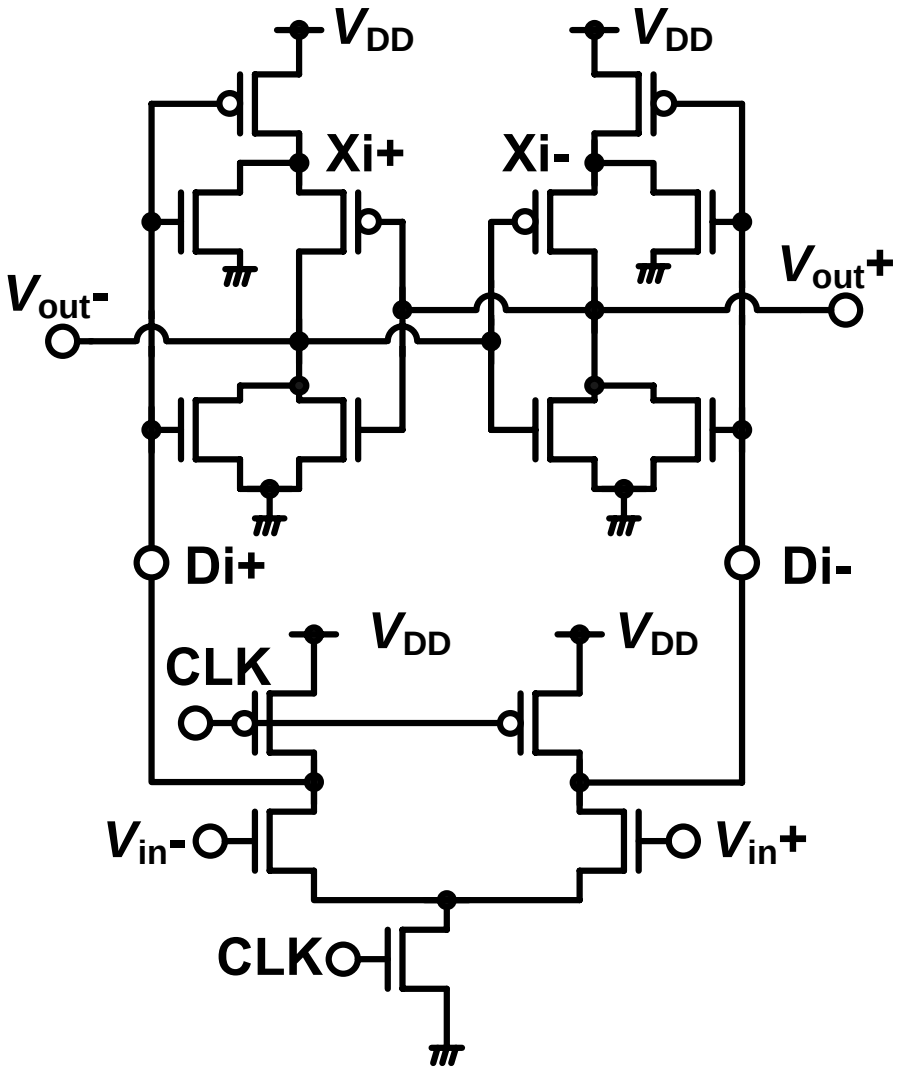
Proposed Comparator

Proposed comparator uses Di nodes voltage instead of $\overline{\text{CLK}}$ for 2nd stage latch timing.



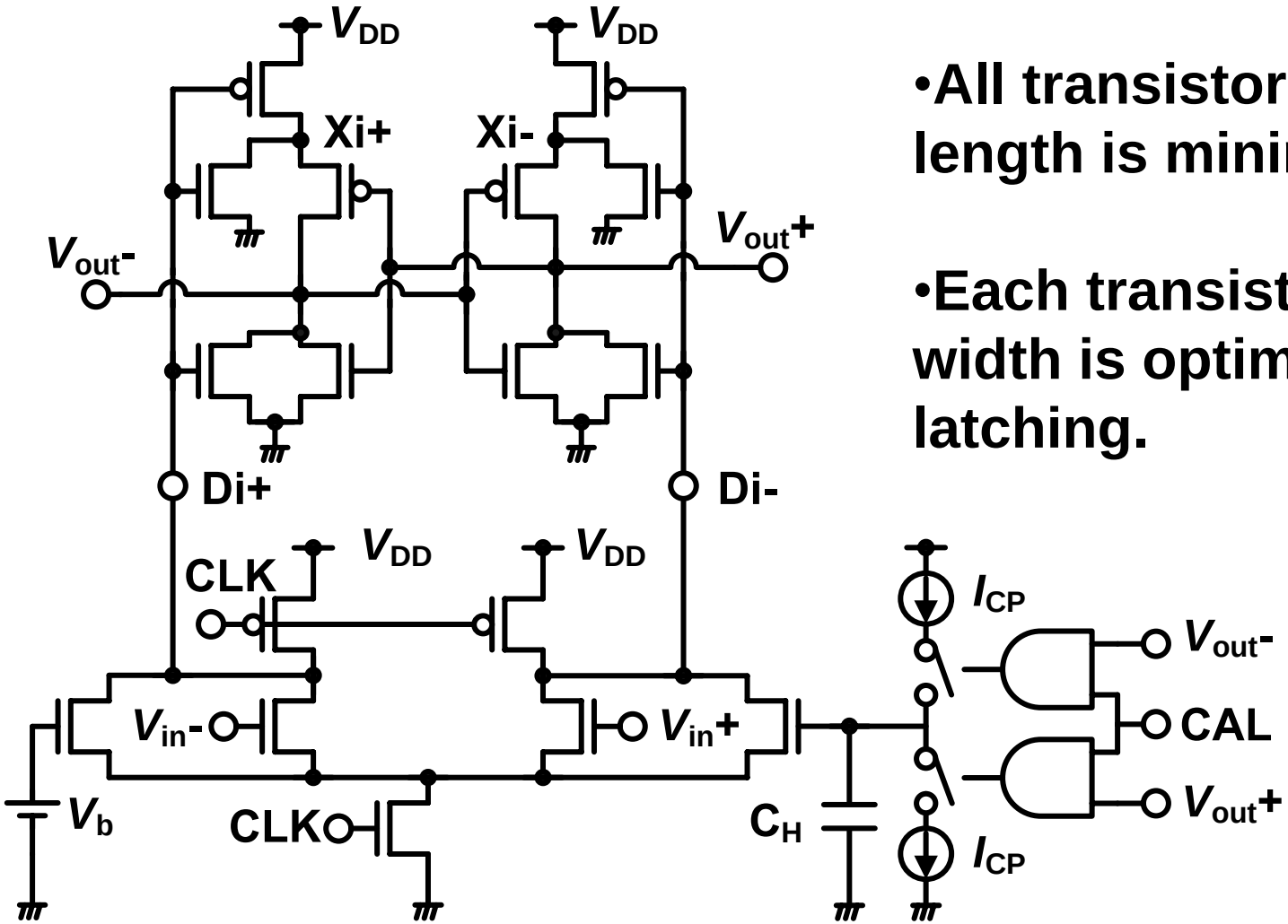


Proposed Comparator Advantages



- High 2nd latch G_m (~2x)
  => less noise from 2nd latch
- Wide area input transistor
  => less offset from 2nd latch
- Less clock driving
- Unaffected by clock skew

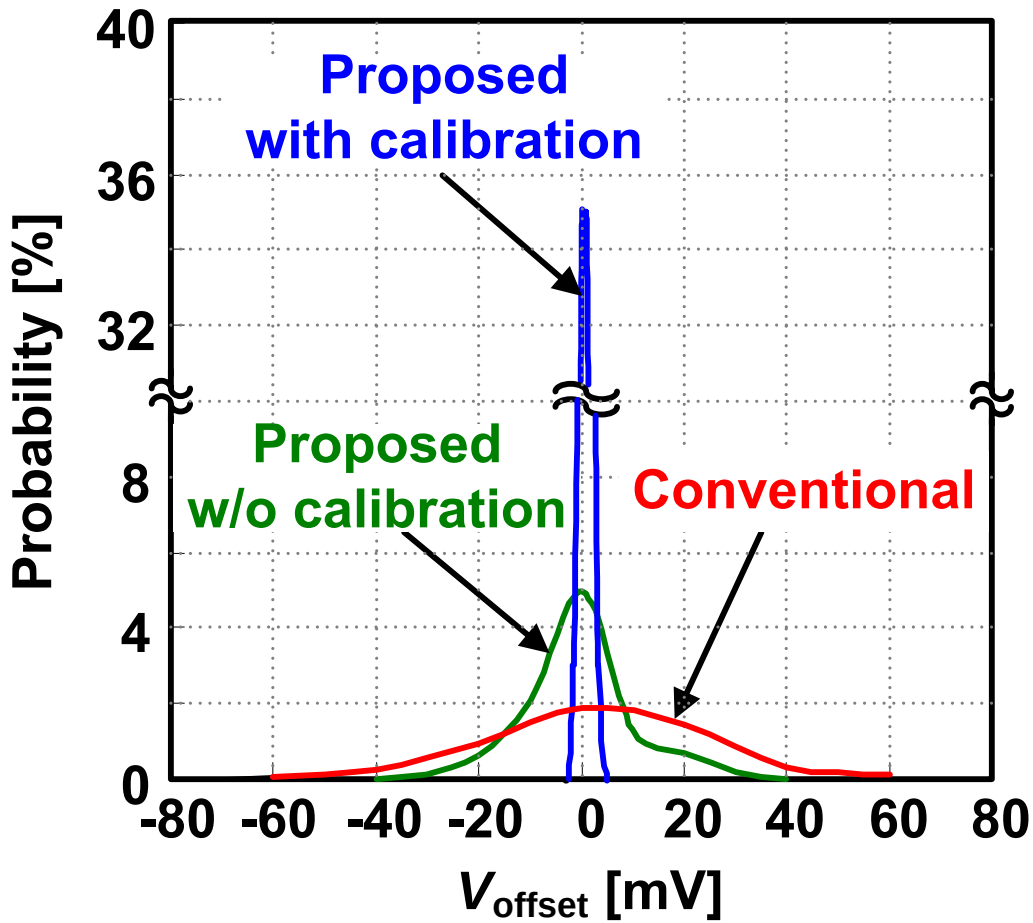
Proposed Comparator with Calibration



- All transistor channel length is minimized.
- Each transistor channel width is optimized for fast latching.

Comparison : Offset Voltage

90 nm CMOS, 100 times Monte Carlo simulations.
Same size transistors are used in each comparators.



Conventional
$V_{offset}(\sigma)$ = 21.5 mV

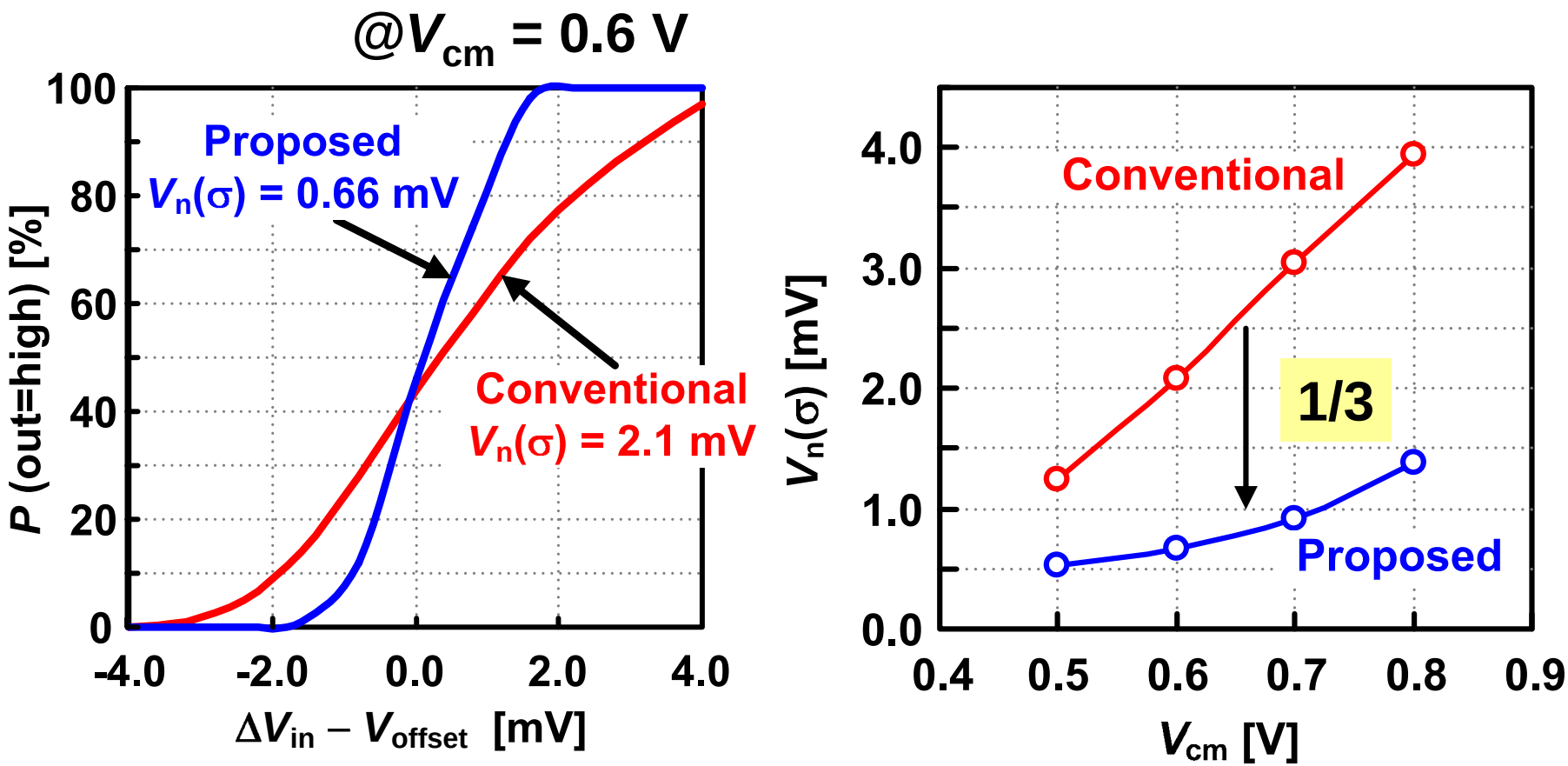
Proposed (CAL OFF)
$V_{offset}(\sigma)$ = 13.5 mV

Proposed (CAL ON)
$V_{offset}(\sigma)$ = 1.3 mV

Offset voltage 1/16

Comparison : Noise

V_{DD} = 1.0 V, Fc = 4 GHz, Transient-Noise simulations.
(Offset calibration is not used.)



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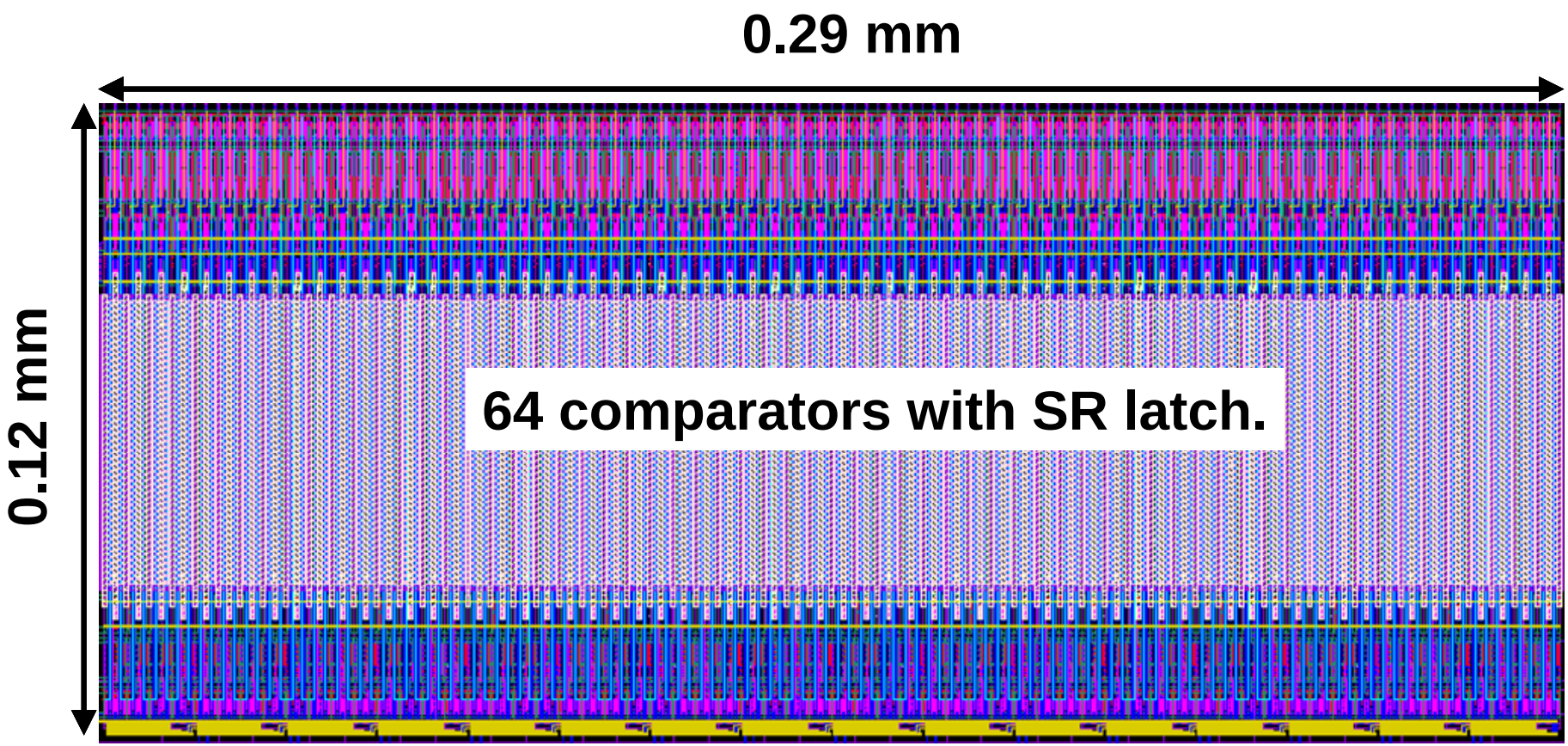
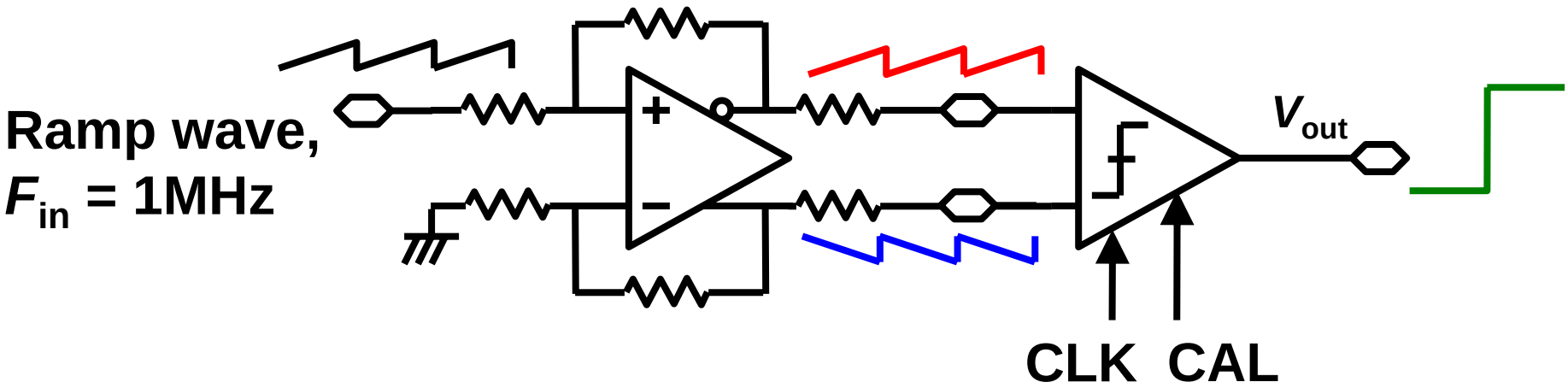
Layout

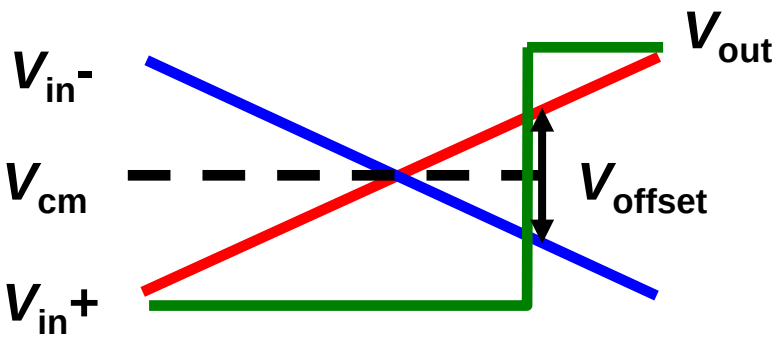
A prototype comparator has been realized in a 90 nm 10M1P CMOS technology with a chip area of 0.0348mm^2



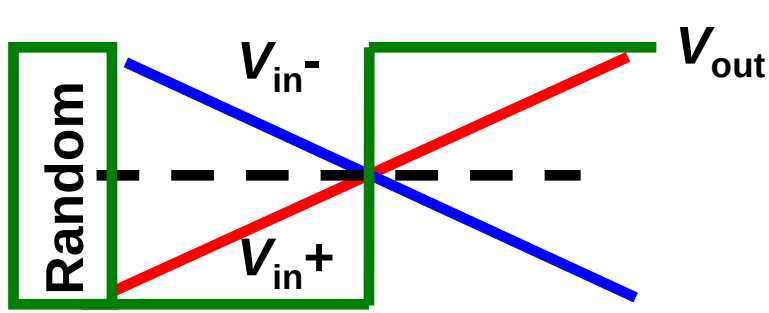
Measurement System



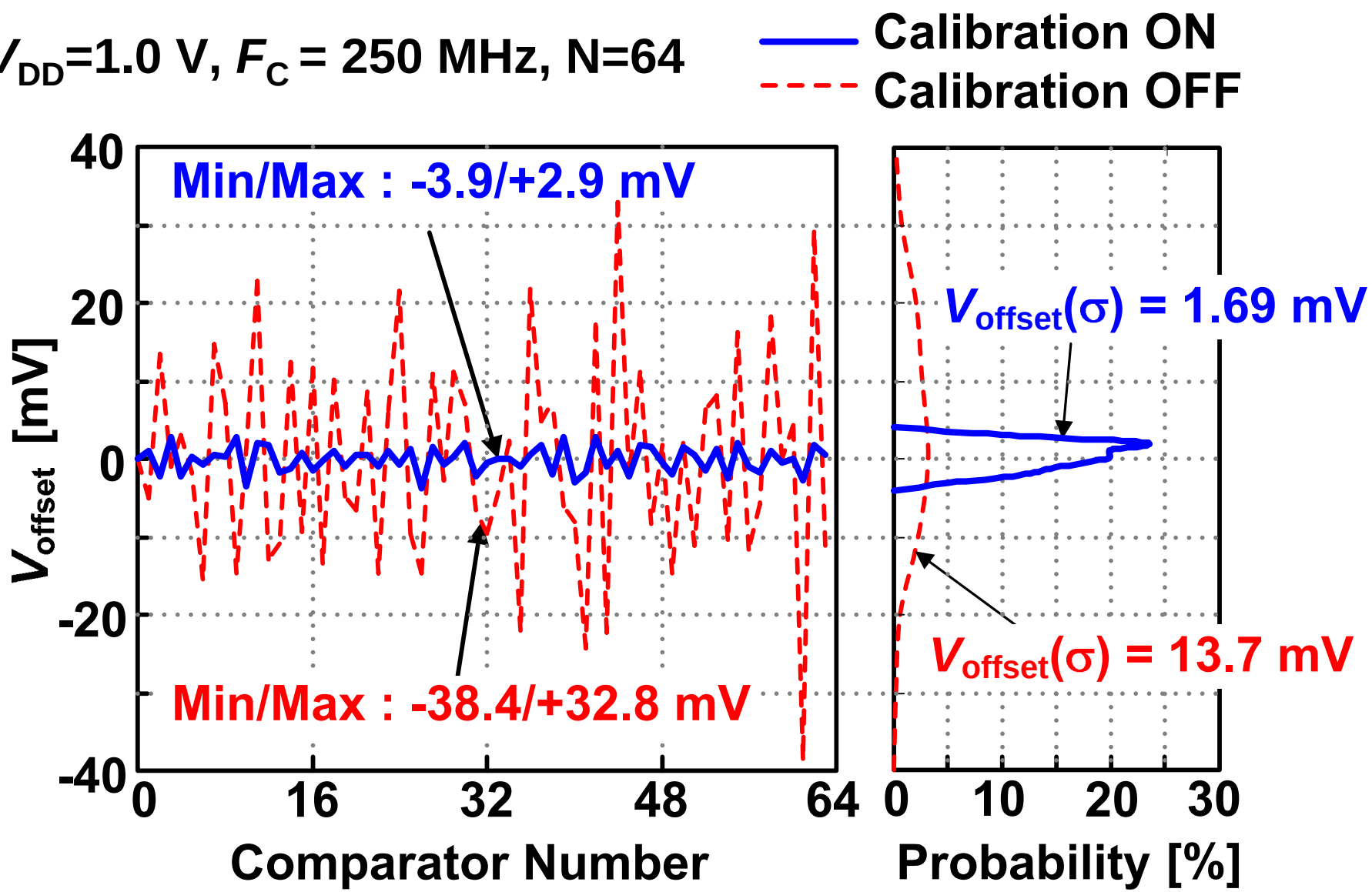
Without CAL



With CAL

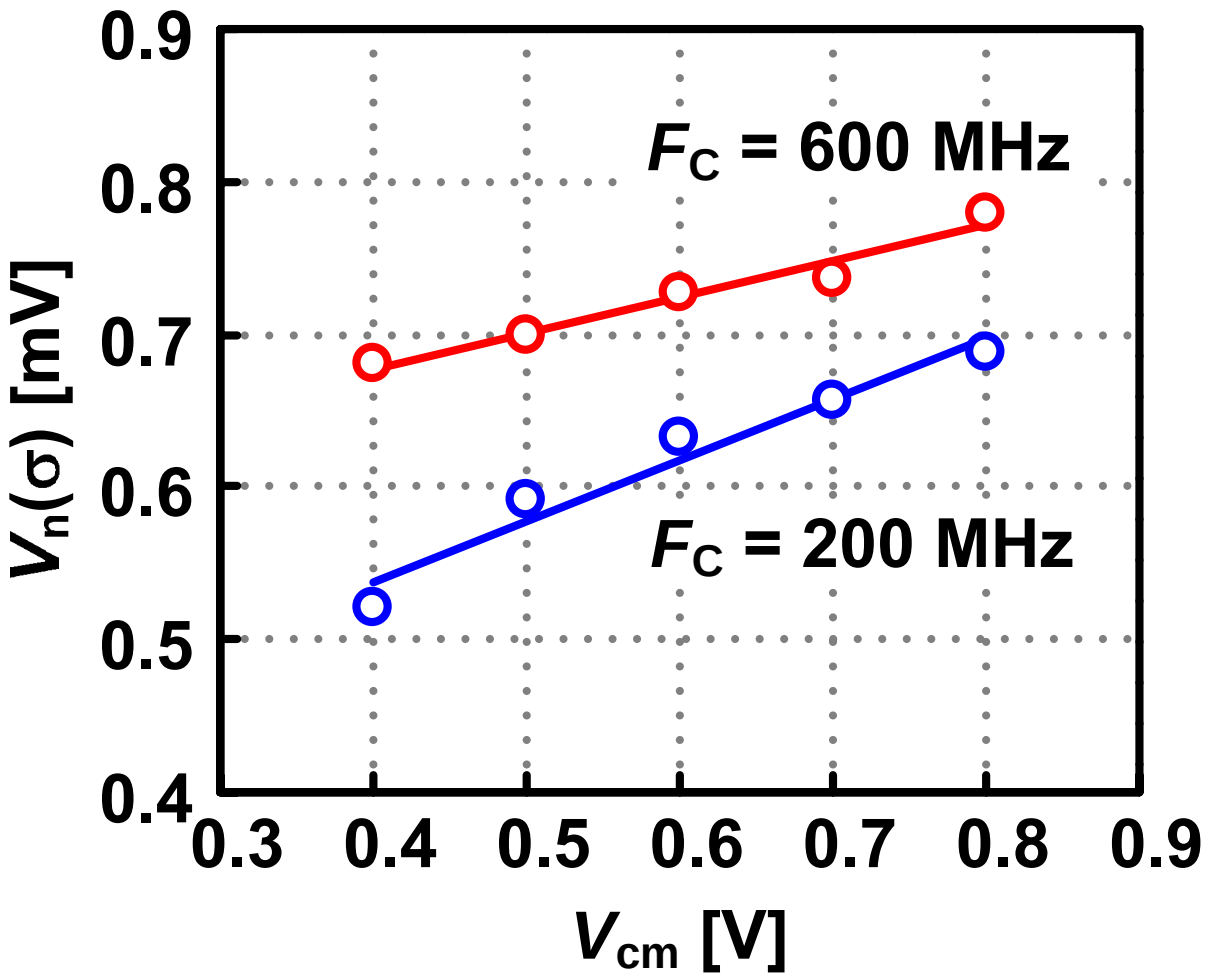


Measurement Results : Offset



Measurement Results : Noise

V_{DD}=1.0 V, Offset Calibration is not used.



Performance Summary

Technology	90nm, 1poly, 10metals CMOS
Active Area	120µm x 290µm (64 comparators)
$V_{offset}(\sigma)$ CAL OFF/ON	13.7mV / 1.69mV
Input eq. noise $V_n(\sigma)$	0.7mV @ F_c=600MHz, V_{cm}=0.5V
Supply Voltage	1.0V
Power consumption	40 µW/GHz (20 fJ/conv.)

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Conclusion

A low offset voltage, low noise dynamic latched comparator using a self-calibrating technique is proposed.

☺ **Features**

- **The new calibration technique does not require any amplifiers for the offset voltage cancellation and quiescent current.**
- **It achieves low offset voltage of 1.69 mV at 1 sigma, while 13.7 mV is measured without calibration.**
- **A low input noise of 0.6 mV at 1 sigma, three times lower than the conventional one.**

Thank you for your interest!

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