A 80GHz Voltage Controlled Oscillator With a Negative Varactor in 90nm CMOS Technology

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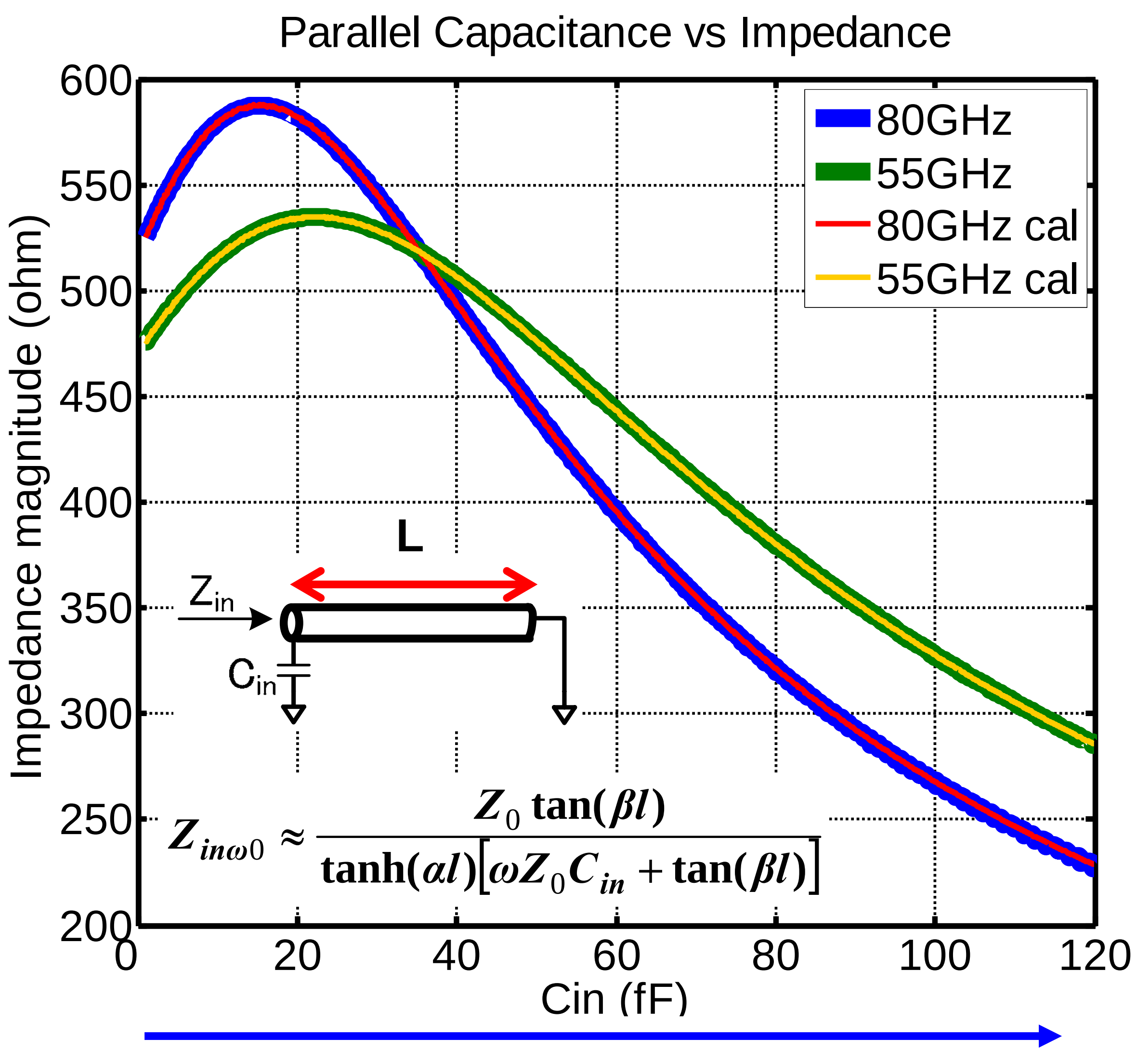
Outline

- Background
- Negative Equivalent Capacitance
- Schematic
- Measurement results

Background

- **Challenges of mm-Wave VCOs**
  – **Differential pair, varactor and switches increase loading capacitance**
  – **Input impedance decreases with loading capacitance**
  – **Increase of tail current has diminishing returns in producing negative resistance**

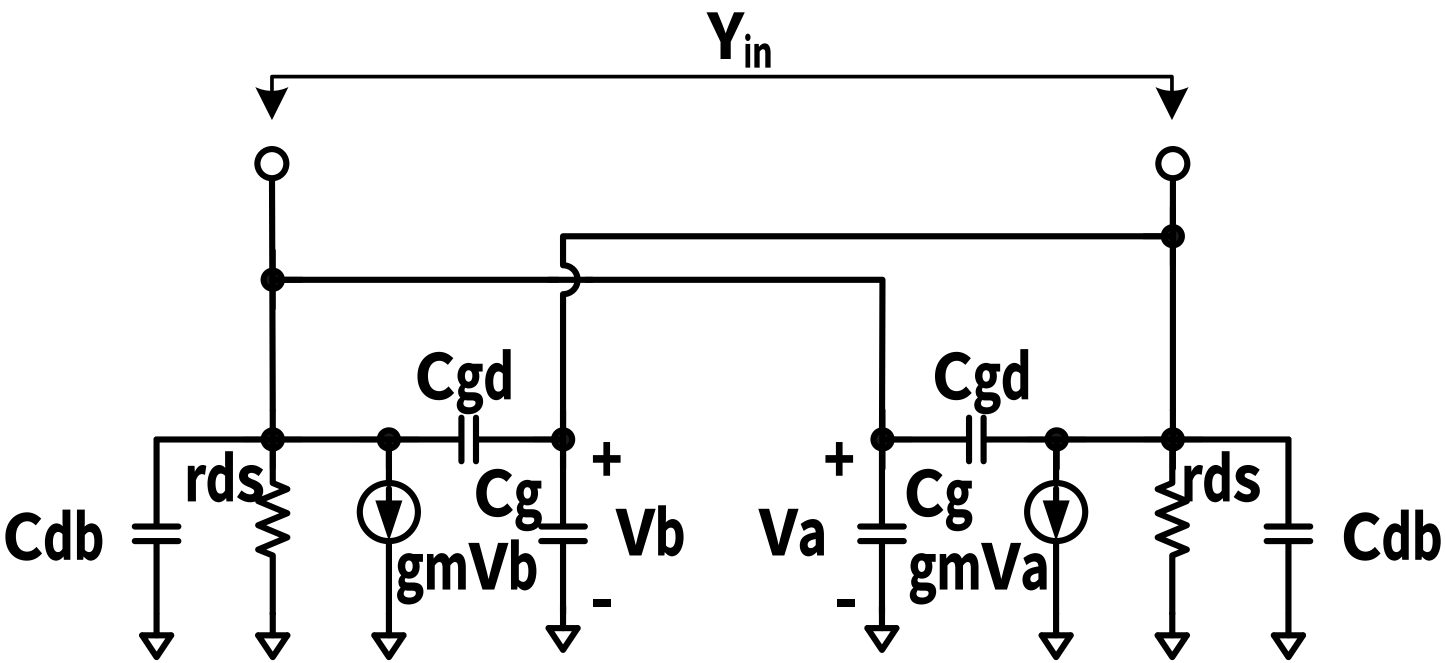
Imp. at f0 of Shorted T-line w/ Cap.



$$Z_{in\omega 0} \approx \frac{Z_0 \tan(\beta l)}{\tanh(\alpha l)\left[\omega Z_0 C_{in} + \tan(\beta l)\right]}$$

Decreasing Transmission line length L

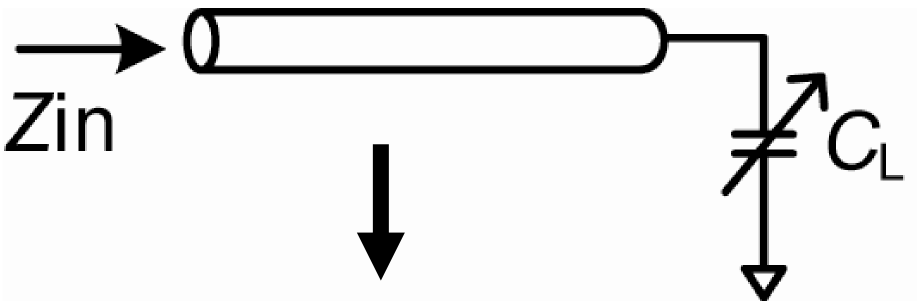
Impedance of Diff Pair

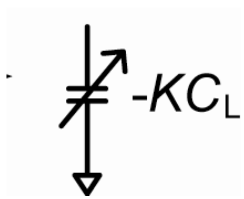


$$Y_{in} = \frac{1}{2 \cdot rds} - \frac{gm}{2} + j\left(\frac{\omega \cdot C_{db}}{2} + 2 \cdot \omega \cdot C_{gd} + \frac{\omega \cdot C_g}{2}\right)$$

Increasing current increases gm, and also 1/(2*rds)
There is a limit on how much current can be increased

Negative Varactor Capacitance





Condition for negative cap.

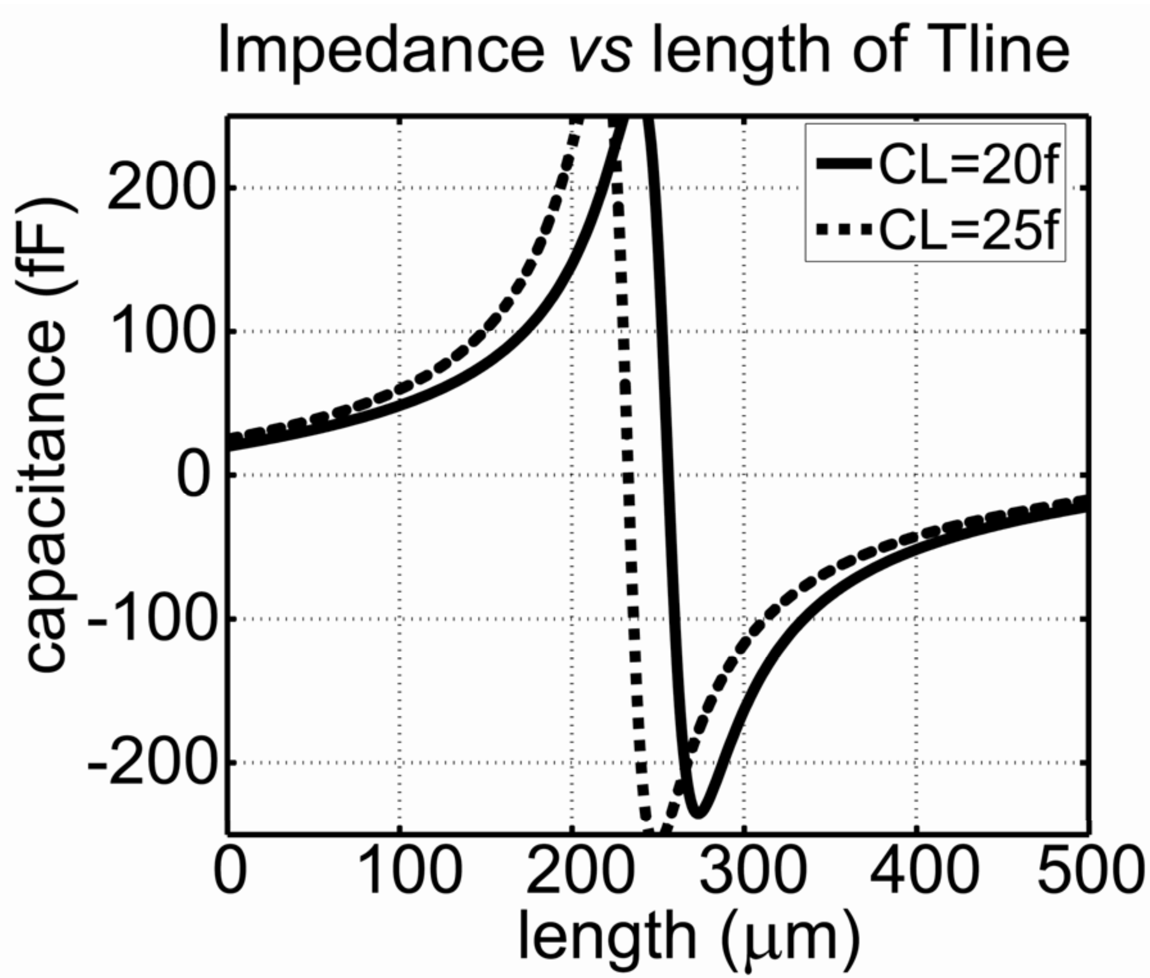
$$Z_0\omega C_L \tan\beta l > 1 \cap \frac{\tan\beta l}{Z_0\omega C_L} > -1$$

$$\frac{\tan\beta l}{Z_0\omega C_L} < -1 \cap Z_0\omega C_L \tan\beta l < 1$$

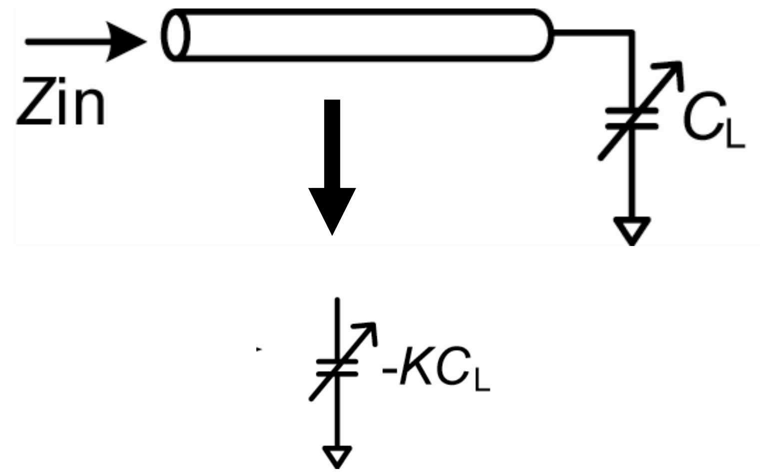
Equivalent input capacitance

$$C_{eq} = \mathrm{Im}\left(\frac{Z_0\omega C_L + \tan\beta l}{\omega Z_0\left(1 - Z_0\omega C_L \tan\beta l\right)}\right)$$

Equivalent Capacitance Plot

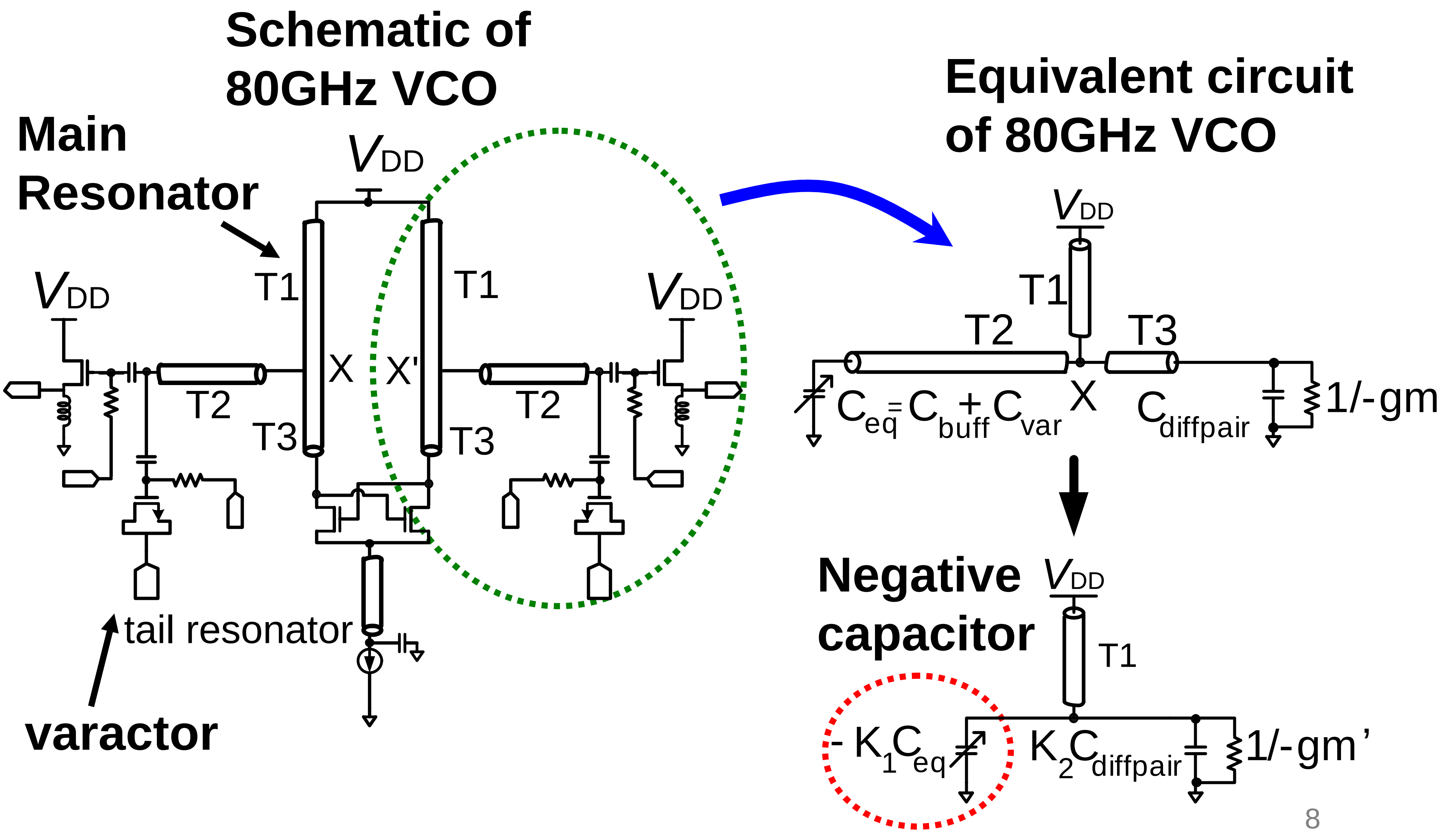


Transmission line with loaded capacitance



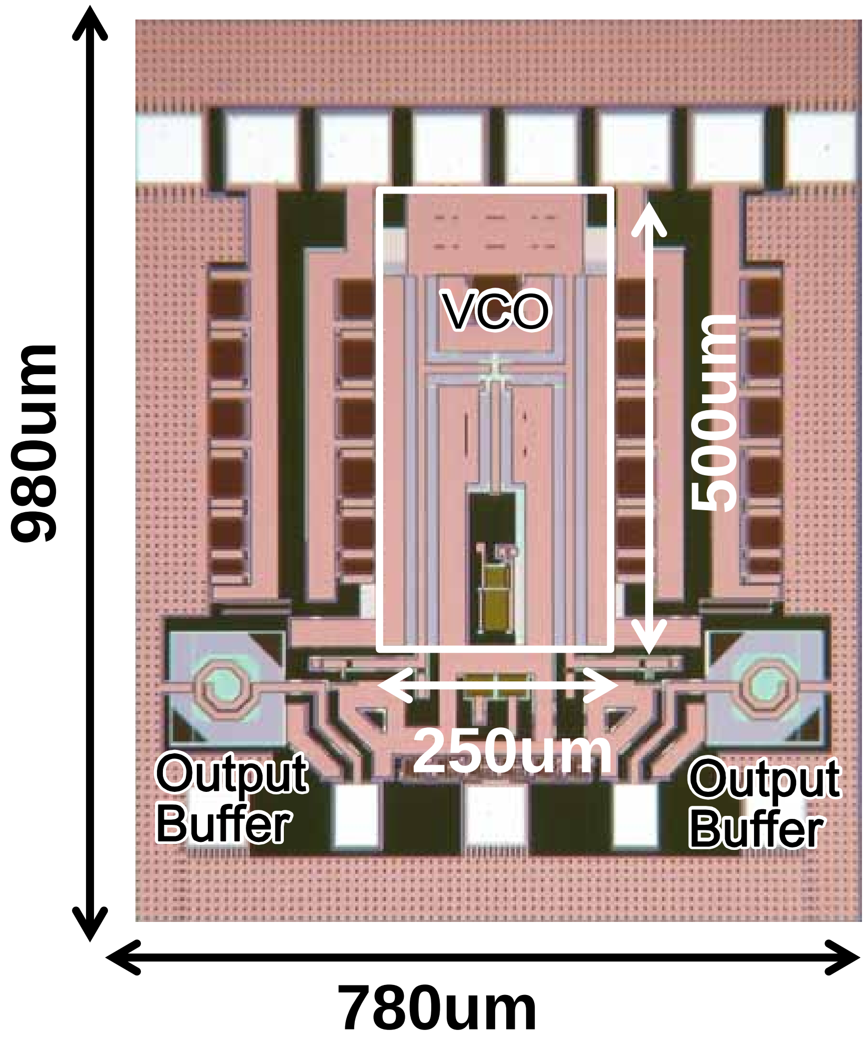
Equivalent capacitance

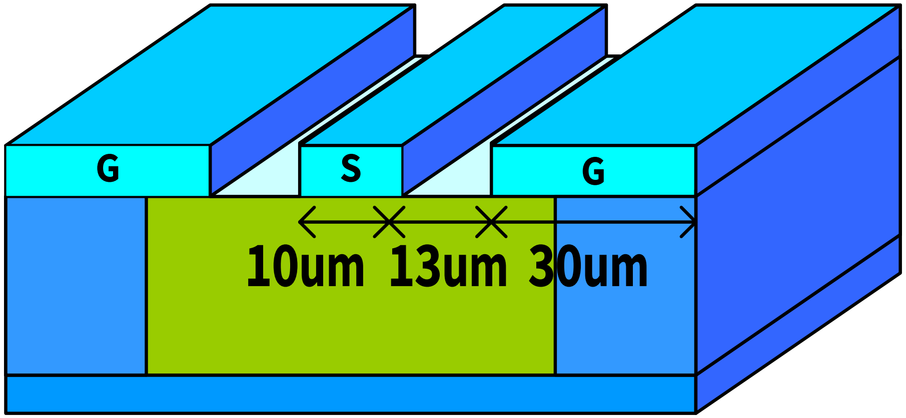
Equivalent Circuit



Chip Photo

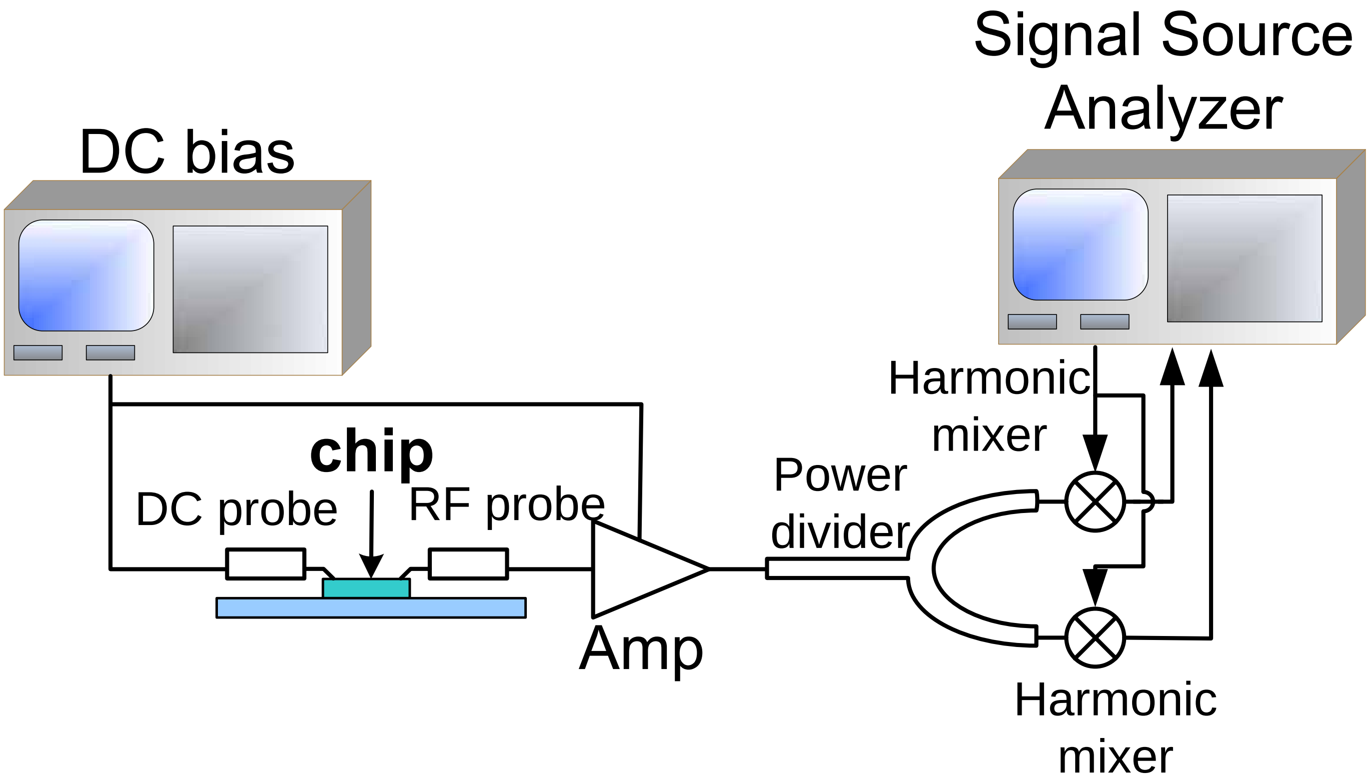
Chip Photo of mm-Wave VCO





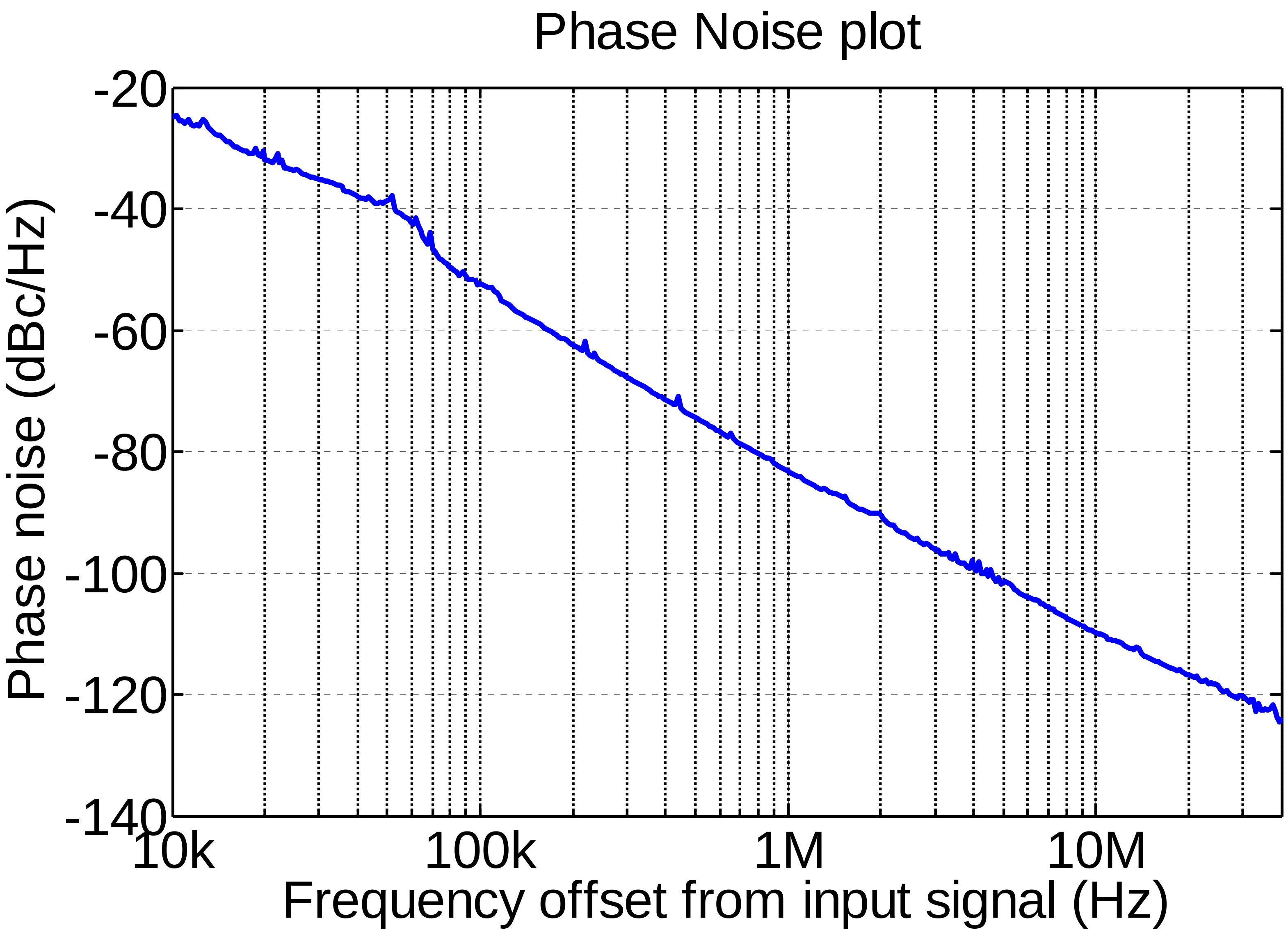
Simulated Q > 20

Measurement Setup



Harmonic mixer – up to 60dB loss
Amp – Max 30dB gain

Measured Phase noise



VCO Measurement Summary

	This	[1]	[2]	[3]
f0 (GHz)	83GHz	90.3	70.2	76.5
FTR (GHz)	0.68	2.9	6.68	5.5
PN (dBc/Hz)	-110@10MHz	-95@1MHz	-106@10MHz	-111@10MHz
Pdiss (mW)	13	57.7	5.4	13.58
FOM	-177	-176	-175.7	-176
Power supply	1.2V	1.2v	1.2	0.7V
Technology	90nm CMOS	65nm CMOS	65nm SOI	90nm CMOS

[1] Laskin, ISSCC08

[2] Kim, ISSCC07

[3] Ishibashi, VLSI 2007

Summary and Conclusion

- **Decreased tank impedance due to tank capacitance at high frequency limit the operation of oscillators at high frequencies**
- **Increasing the current and gm is limited by the decreased output impedance due to the drain source resistance**
- **Impedance transformation can help to create a negative capacitance to cancel out the parasitic capacitance of the tank, increasing oscillation frequency**