Introduction

Many publications about 60GHz transceivers and its blocks have been seen recently both from academia and industry. Obviously, the 9GHz unlicensed wide-band at 60GHz which can realize a data transfer rate up to several tens Gbps is a big lure for the study. Accompanying with the scaling down of the CMOS technology, f_t and f_{max} of transistors are achieved above 100GHz, making an all-CMOS solution at 60GHz feasible. The merits of low cost and high integration of CMOS process make it a good candidate for the 60GHz transceivers. As the first block in the receiver, the noise performance of the LNA determines that of the whole system. Therefore, it is important to minimize the noise figure (NF) and improve the gain of the LNA for better sensitivity of the whole system. Finding ways to reduce the NF of the CMOS LNA becomes a great challenge for all of the designers.

Cascode with source degeneration is the most commonly used topology in CMOS LNA circuits because of its unconditionally stable at the operating frequency, making the design more robust and simplifying the matching network [1]. However, at mm-wave frequency, due to the low gain of the common-source (CS) transistor and high noise of the common-gate (CG) transistor, the noise contribution of the CG transistor increases, which makes cascade topology poor noise performance for 60GHz LNAs. Moreover, the gain of cascode topology, although a few dB higher over CS topology, decreases heavily due to the low impedance on the inter-stage node [1], which makes it even less attractive for 60GHz LNAs.

This paper proposes a new three-stage LNA employing a dual noise-matching topology for further NF reduction. NF can not be improved by the conventional cascode LNA shown in Fig. 1(a) due to the higher NF of the CG stage, while lower gain-characteristic of mm-wave transistors can be compensated by the cascade configuration. Basically, CG can not take noise matching in contrast with CS, so the proposed topology utilizes CS with source degeneration in the second stage instead of CG as shown in Fig. 1(b). As a result, the proposed LNA realizes lower NF performance at a cost of larger power consumption. A cascode transistor is added as the third stage to obtain a gain above 15dB. The detail of the proposed LNA is discussed in Section II. Section III explains design considerations for the circuit and presents the simulation results, and section IV concludes the paper.

Noise Optimization for the two-stage cascaded CS topology

At mm-wave frequency, the measured maximum available gain (MAG) of 90nm nMOSFETs is 7.8dB as shown in Fig. 2 [3]. Even for a cascode configuration, the MAG is only near 10dB due to the low impedance on the inter-stage node [1]-[3]. What is more, considering the loss due to the impedance matching network, there is even less gain we can get from a single stage LNA. Therefore, multi-stage topology is needed for mm-wave LNAs to realize a reasonable gain for real applications. The total noise figure (NF_{tot}) for m stages is given by Friis equation [3].

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}}, \quad (1)$$

where NF_i is the noise figure of the i-th stage and A_{pi} is the available power gain. As can be seen, when the gain of the first stage is small, the noise contribution of the second stage will increase.

As specified above, due to the low gain of the CS transistor and high noise of the CG transistor, conventional cascode with source degeneration contributes much more noise than CS topology at mm-wave frequency. Therefore, using cascode architecture as the first stage for mm-wave LNAs will deteriorate the noise performance, and makes it impossible to realize a NF less than 5dB as far as we know.

Based on the above consideration, CS with source degeneration instead of cascode topology is chosen for the first and second stage in a three-stage LNA. The value of source degeneration impedance is adjusted in order to optimize the input matching for gain and noise simultaneously. The simulation is based on the measurement data of the transistor and the model is shown in Fig. 2 [3]. Slow-wave coplanar wave guide (CPW) transmission line is employed for the impedance matching network. Electromagnetic simulation with HFSS is utilized for implementing the CPW. The simulation value of the characteristic impedance is 60Ω and the loss about 0.457dB/mm at the frequency of 60GHz, respectively.

60GHz LNA Design and Simulation Results

A three-stage LNA is designed in a 90nm CMOS process and shown in Fig. 3. The first two stages utilize single transistor with source degeneration, while the third stage is implemented by cascode topology for high gain. It has been proved that a series inductor placed between the CS and CG transistors can improve the performance of the cascode architecture at mm-wave frequency [2]. However, in this design the drain and source parasitic inductance of the transistor have compensated the parasitic capacitance on the inter-stage node. Therefore, a zero length transmission line is used in this case. The bias voltages, transistor sizes and the length of the source degeneration transmission lines have been carefully optimized for gain and noise performance. A model based on the measurement data up to 110GHz including the parasitics is used for all of the transistors. The channel length of the transistors is 100nm, and the width per finger is 2.5μm. Even it is not an optimized finger width for LNA [1]-[2], good simulation results have been achieved. A comparison is also carried out between the proposed LNA and a conventional three-stage cascode LNA by using the same transistor model. The bias voltage for the CS transistors is 0.6V. The simulation results are shown in Table 1 and plotted in Fig. 4. As can be seen, an input matching and output matching result less than -10dB, a gain of 15dB and a NF of 5dB is achieved at 60GHz with a power consumption of 22mW at a voltage of 1.2V for the proposed LNA. Comparing with the conventional configuration, an improvement of 1.4dB of NF has been realized at the cost of 1dB gain decrease for almost the same power consumption.

Conclusions

A three-stage LNA employing a dual noise-matching topology has been proposed. The proposed LNA has two noise-matched CS amplifiers in the first and second stage instead of the conventional cascode configuration, and realizes lower NF than the conventional one. The simulation results of the proposed LNA show that an input matching and output matching result less than -10dB, a gain of 15dB and a NF of 5dB are achieved at 60GHz with a power consumption of 22mW at a voltage of 1.2V for the proposed LNA. Comparing with the conventional configuration, an improvement of 1.4dB of NF has been realized at the cost of 1dB gain decrease for almost the same power consumption. Both of the proposed and conventional LNA are simulated in a 90nm CMOS process.

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Figures

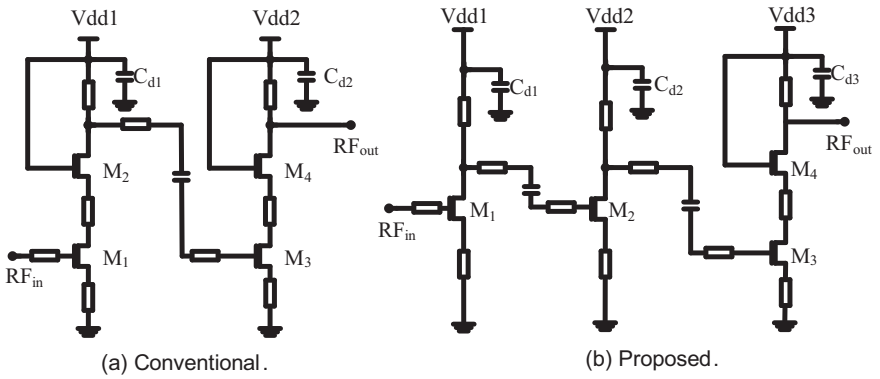

Figure 1. Simplified schematic of the LNA.

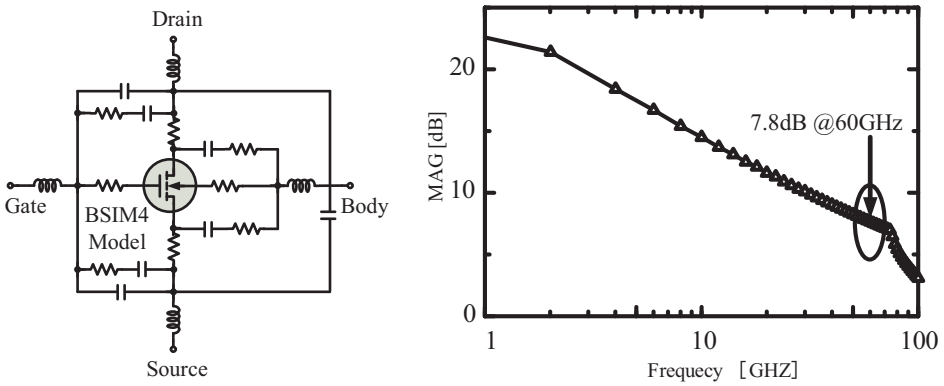

Figure 2. NMOS model and measured maximum available gain for single-transistor in 90nm CMOS technology, W_f=2.5μm, N_f=32, V_{gs}=0.8V and V_{ds}=0.8V.

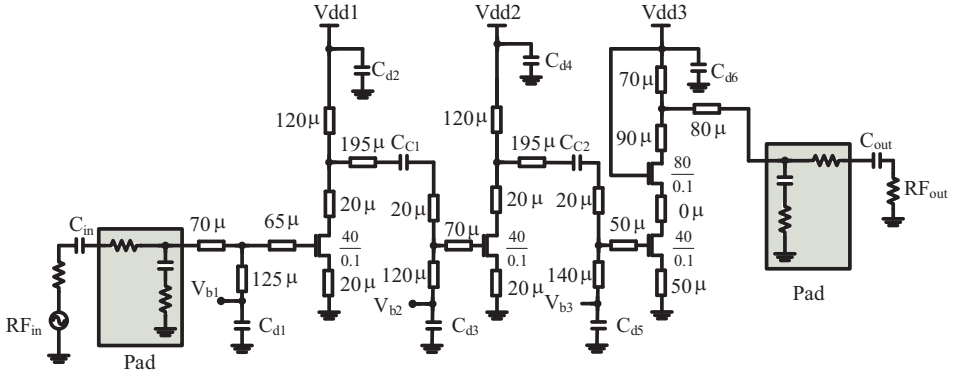

Figure 3. Schematic of the proposed LNA.

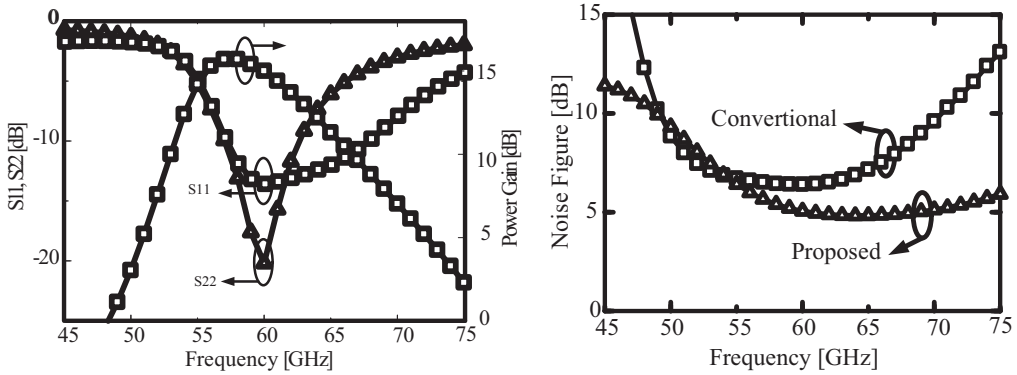

Figure 4. Simulated input and output matching, power gain and NF of the proposed LNA.

Table 1

	Simulation		Measurement			
	Proposed	Conventional	[2]	[5]	[6]	[7]
Technology	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS
Topology	Dual-CS	cascode	cascode	cascode	CS	cascode
f_{center} [GHz]	60	60	58	64	63	60
S11@ f_{center} [dB]	<-13	<-17	<-6	<-25	~ -5	<-15
Gain [dB]	15	16	14.6	15.5	12.2	22.3 (diff.)
NF [dB]	5.0	6.4	5.5 (sim)	6.5	6 (sim)	6.1
Vdd [V]	1.2	1.2	1.5	1.65	1	1.2
Power [mW]	22	19	24	86	10.5	35

Title:

A Three-Stage 60GHz CMOS LNA Using Dual Noise-Matching Technique for 5dB NF

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Abstract:

A three-stage LNA employing a dual noise-matching topology has been proposed. The proposed LNA has two noise-matched common-source amplifiers in the first and second stage instead of the conventional cascode configuration. The simulation results of the proposed LNA show that input and output matching of less than -10dB, a gain of 15dB and a NF of less than 5dB are achieved at 60GHz with a power consumption of 22mW at a voltage of 1.2V for the proposed LNA. Comparing with the conventional configuration, an improvement of 1.4dB of NF has been realized at the cost of 1dB gain decrease for almost the same power consumption. Both of the proposed and conventional LNA are simulated in a 90nm CMOS process.

Keyword:

Low noise amplifier, CMOS, mm-wave integrated circuit, 60GHz.

Acknowledgments:

This work was partially supported by MIC, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.