# A Three-Stage 60GHz CMOS LNA Using Dual Noise-Matching Technique for 5dB NF

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Matsuzawa & Okada Lab.

# Outline





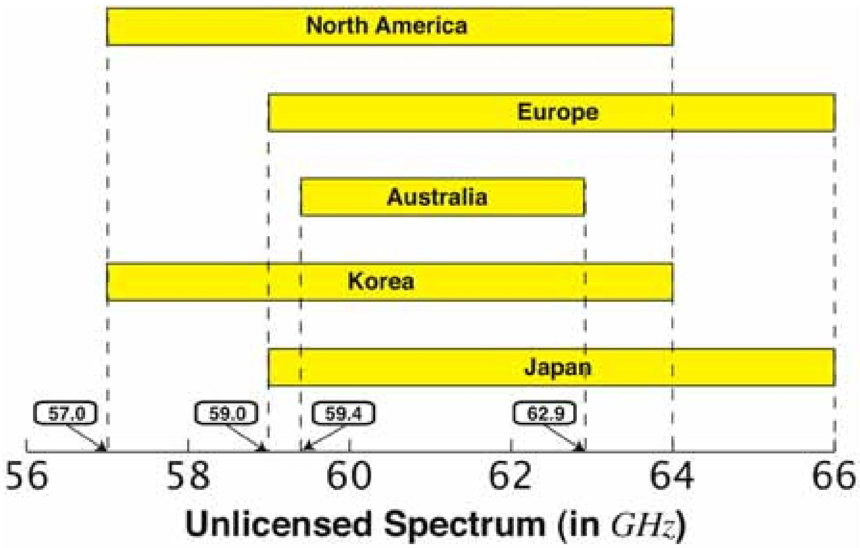
◆Background

◆60GHz LNA Design Method

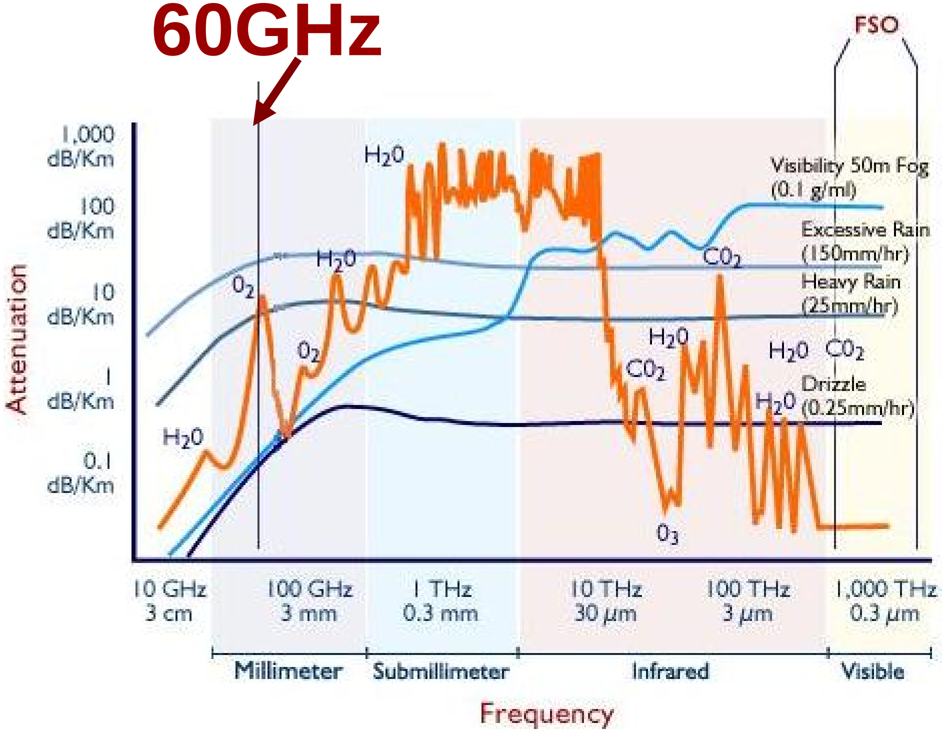
◆Circuit and Simulation Results

◆Conclusions

# Background




- 7 GHz unlicensed band at 60 GHz
- Gbps data transfer




- Short range
- Good isolation

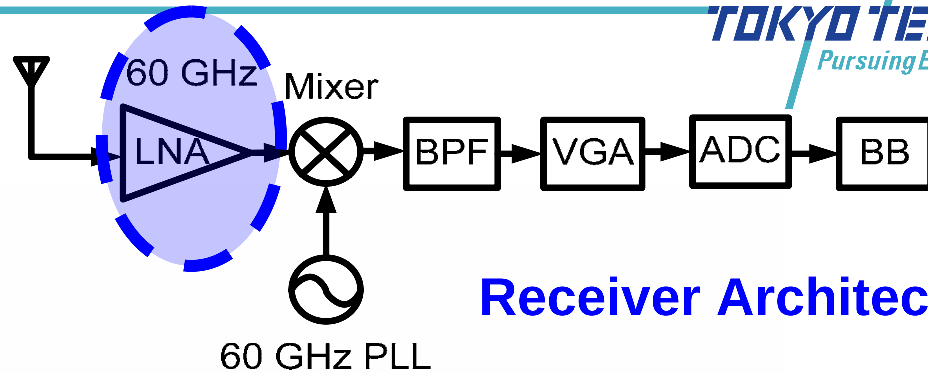
**Reference:**

1. http://windowsil.org/2008/03/13/60-ghz-wireless-communications/
2. http://www.dailywireless.org/2006/11/13/more-70ghz-radios/

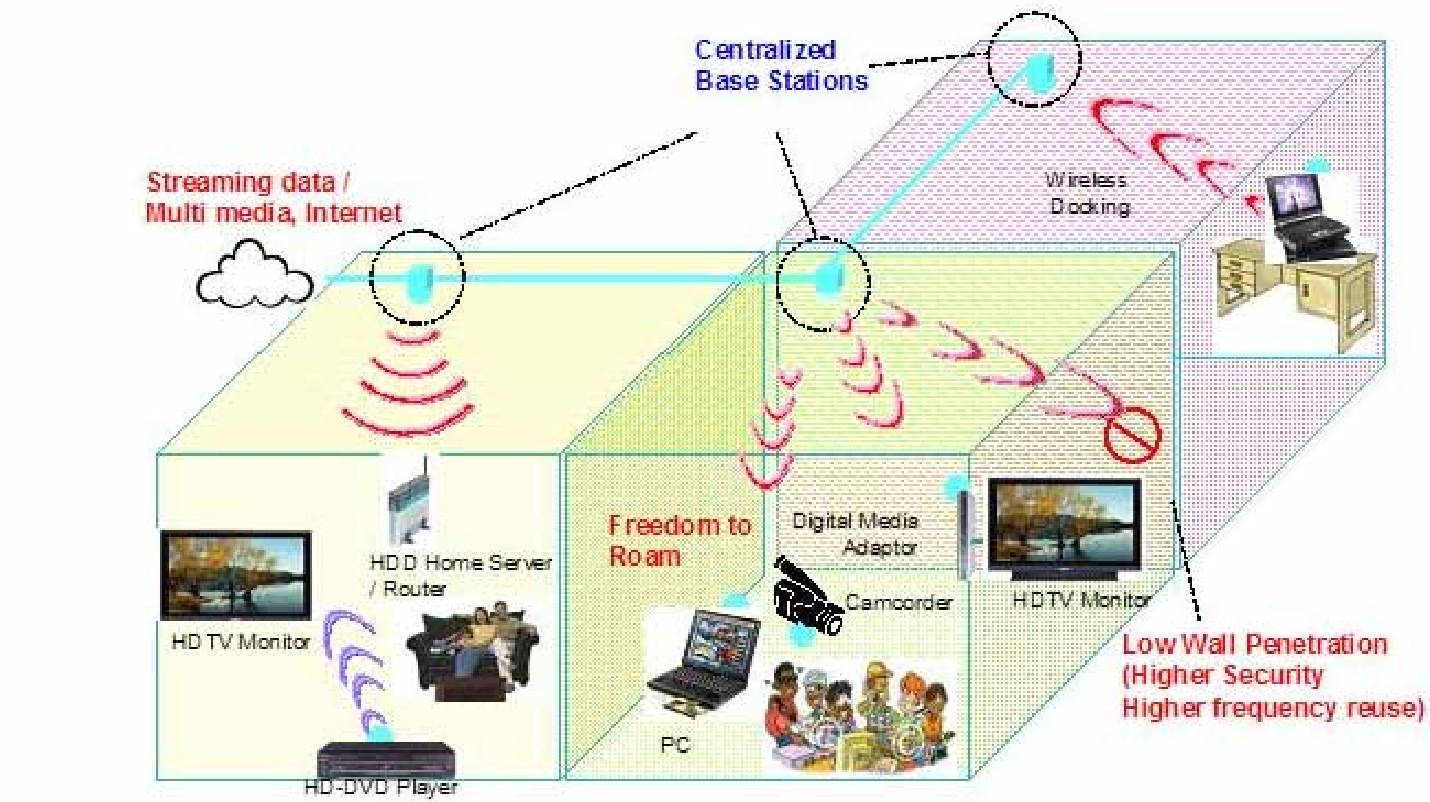
# Applications



- ◆WPAN
- ◆Wireless HDMI
- ◆Point to Point links




Receiver Architecture




Ref: http://domino.research.ibm.com/comm/research_projects.nsf/pages/mmwave.apps.html

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# When up to mm-wave CMOS LNA…

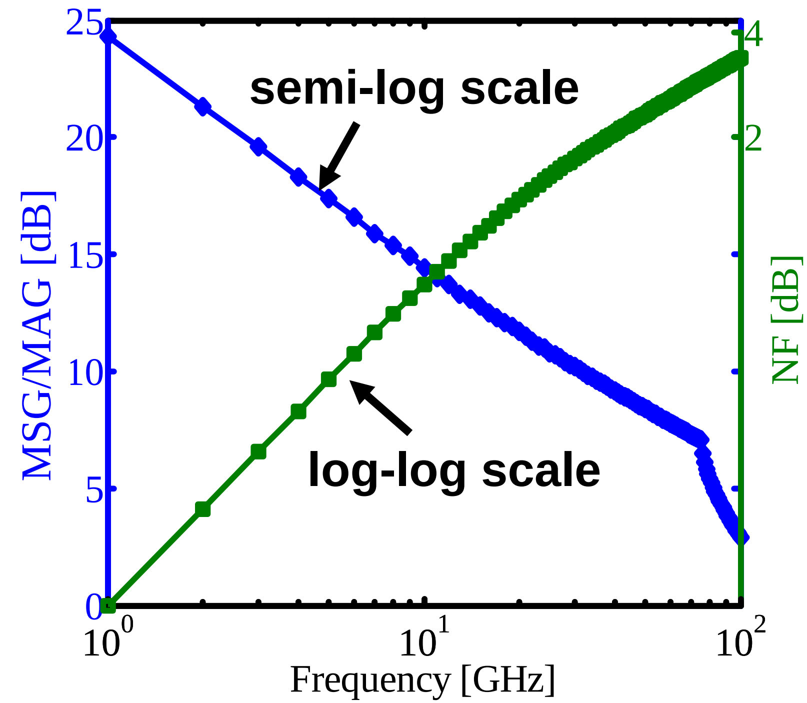
➢ High frequency

☹ Lower gain

- ☹ MAG is inversely proportional to the logarithm of the operating frequency $f_c$.

☹ Higher noise

- ☹ $NF_{min}$ is proportional to the operating frequency $f_c$.

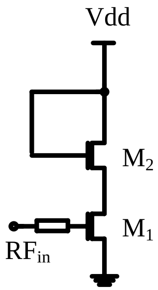



$W_f$=2.5 µm, $N_f$=32, $V_{gs}$=0.8V and $V_{ds}$=0.8V.

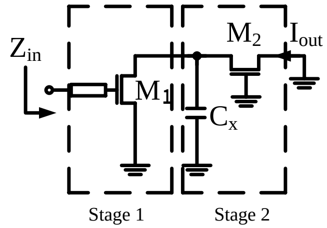
$$G_{MAG} \approx 20 \lg\left(\frac{\omega_{MAX}}{\omega_c}\right)$$

$$NF_{min} = 1 + \left(\frac{\omega_c}{\omega_T}\right)\sqrt{1.2 G_m (R_g + R_s)}$$

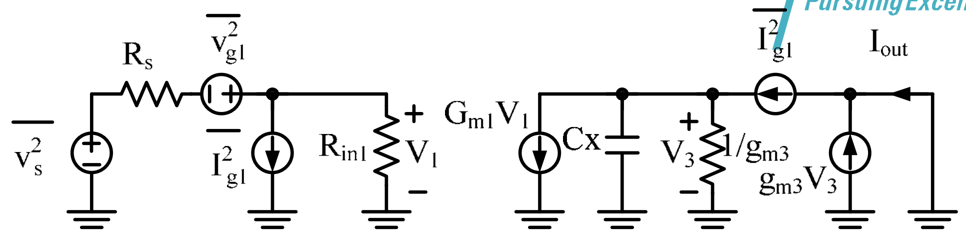
# Cascode Topology Noise




**Cascode**




**CS+CG**




**Small signal equivalent circuit**

$$F_{tot,cascode} = F_1 + 4R_s\gamma_2 g_{d02}\left(\frac{\omega_0^2}{\omega_T^2}\right)\left(\frac{C_x^2}{g_{m2}^2}\omega_0^2\right)$$

$$F_1 = 1 + \frac{\overline{(I_{g1}R_s + V_{g1})^2}}{4kTR_s} = 1 + \gamma g_{d01} R_s\left(\frac{\omega_0^2}{\omega_T^2}\right)$$

$$\omega_T = \frac{g_{m1}}{C_{gs1}}$$

$$C_x = C_{gs2} + C_{sb2} + C_{db1}$$

- **High noise contribution of M2 due to the large inter-stage node capacitance.**

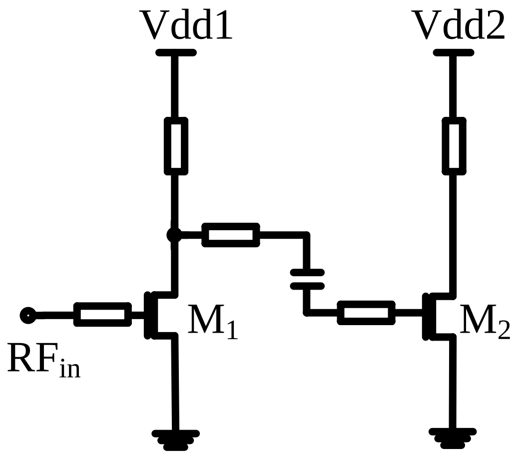
**Reference:**

**Hirad Samavati, et al., IEEE JSSC, VOL. 35, NO. 5, MAY 2000**

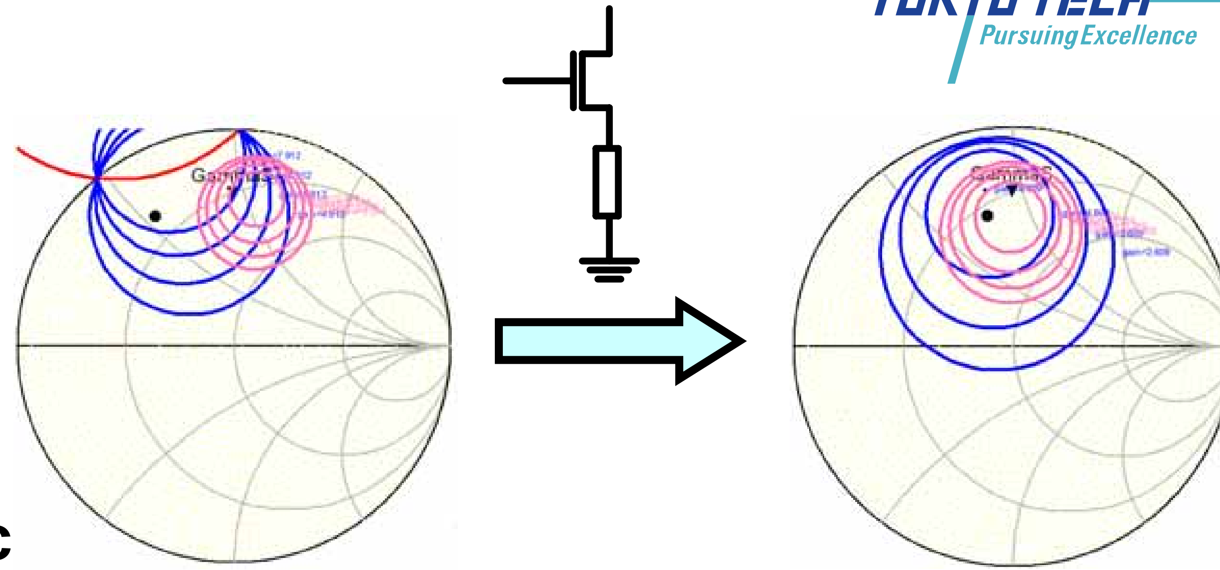
# CS-CS Noise








**Proposed schematic**



○ Noise Circles

○ Available Gain Circles

○ Source Stability Circle

- ◆Common source topology has a smaller NF.
- ◆Using source degeneration to adjust the value of the input impedance.

**Reference:**
**D.K. Shaeffer, et al., IEEE JSSC, VOL. 32, NO. 5, MAY 1997.**

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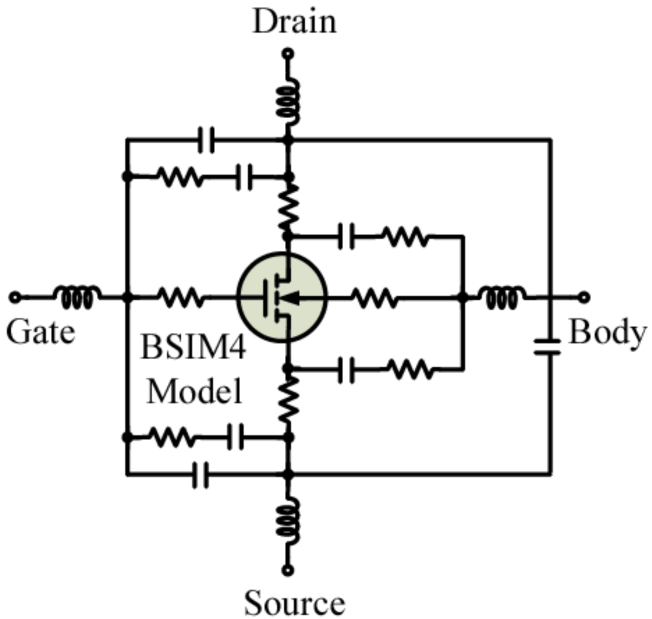
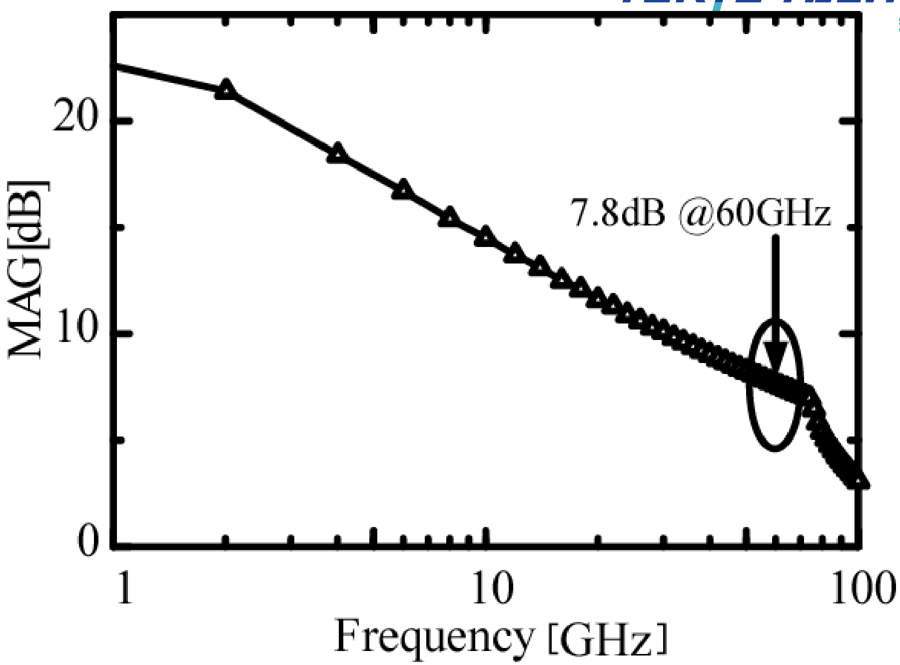
- ◆**Circuit and Simulation Results**
- ◆Conclusions

# Transistor Model at 60 GHz




- ◆**Based on BSIM4 model**
- ◆**Large signal**
- ◆**Scalable**
- ◆**Back-gate model**

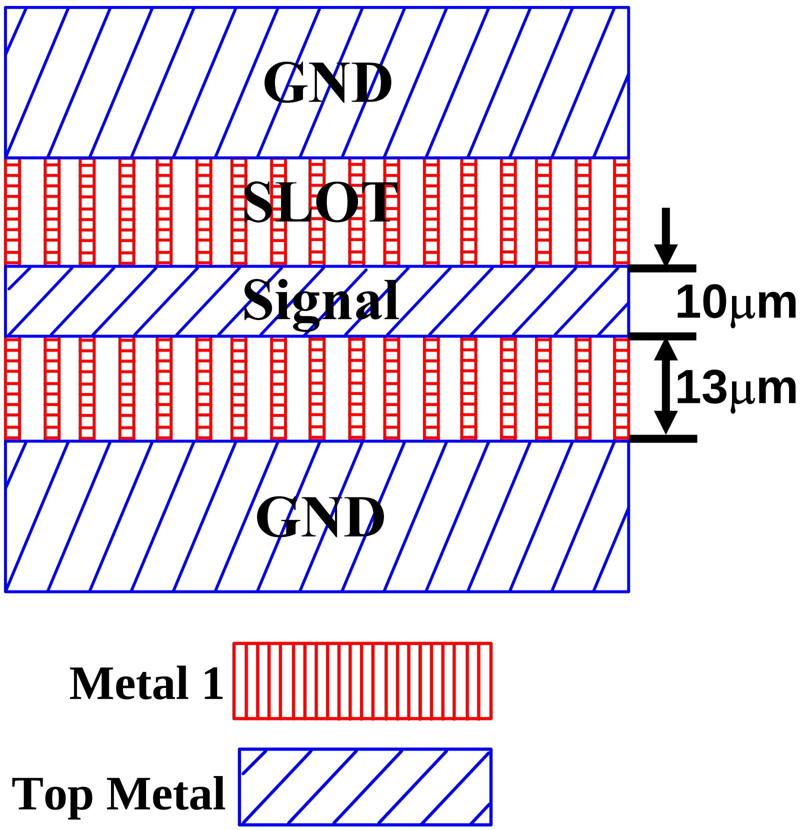
**Measurement condition:**

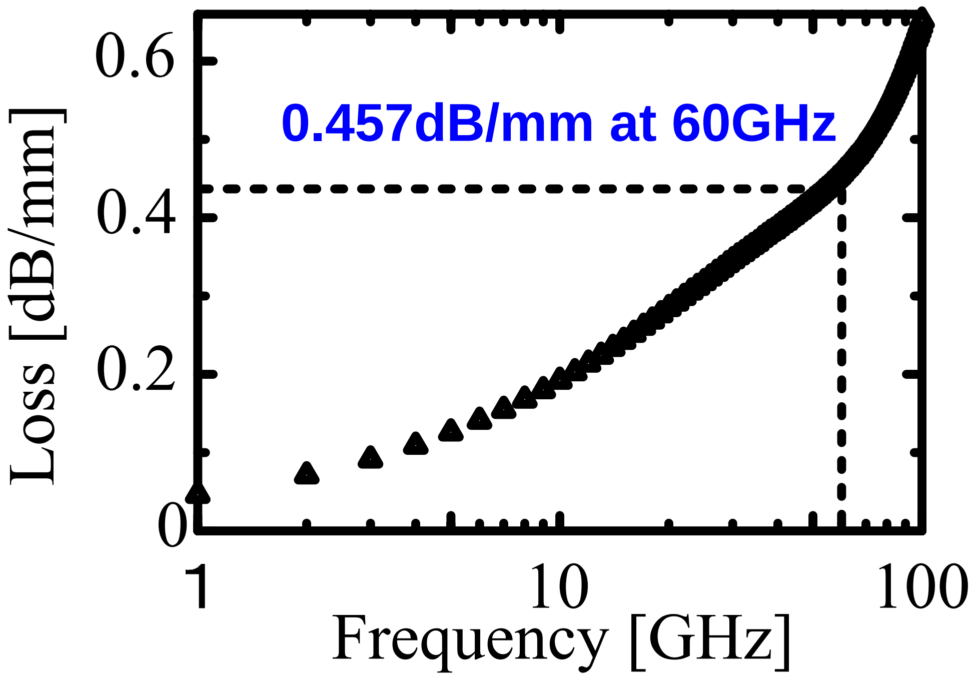
**$W_f$=2.5 µm, $N_f$=32, $V_{gs}$=0.8V and $V_{ds}$=0.8V.**

# Slow-wave Transmission Line








Small area!

**L → Constant**

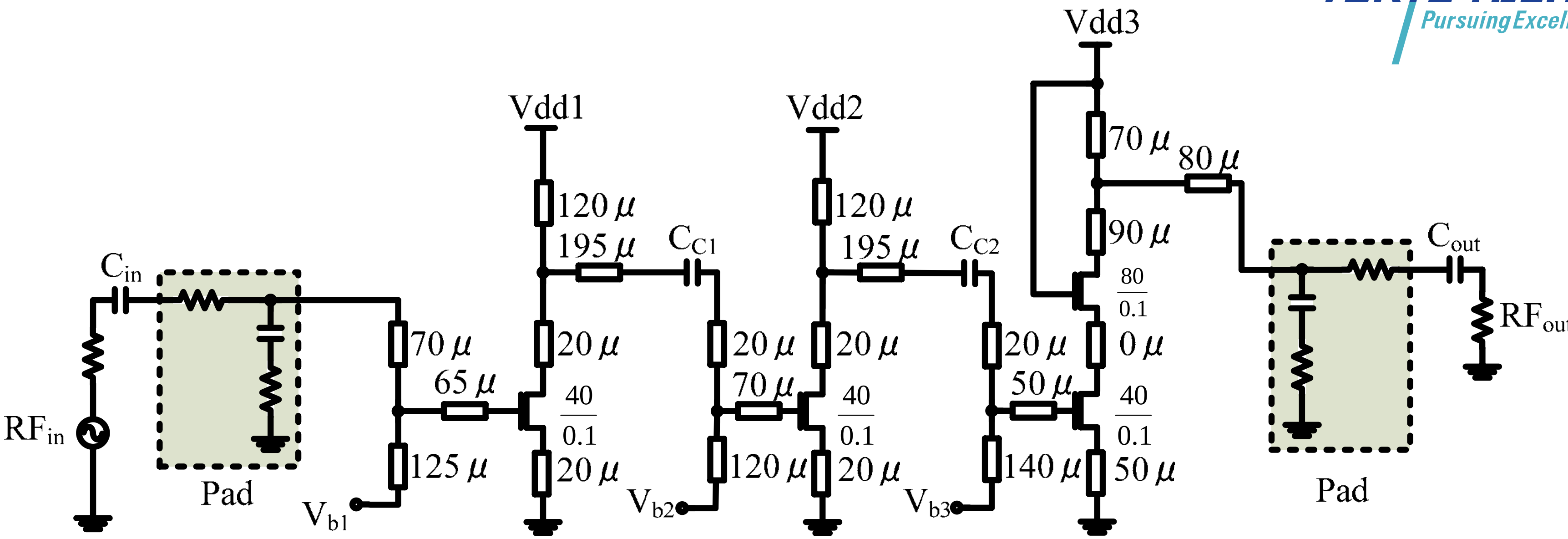
**C → Larger**

**Phase Constant:** $\beta \approx \omega\sqrt{LC}$ ↑

# Proposed LNA Circuit



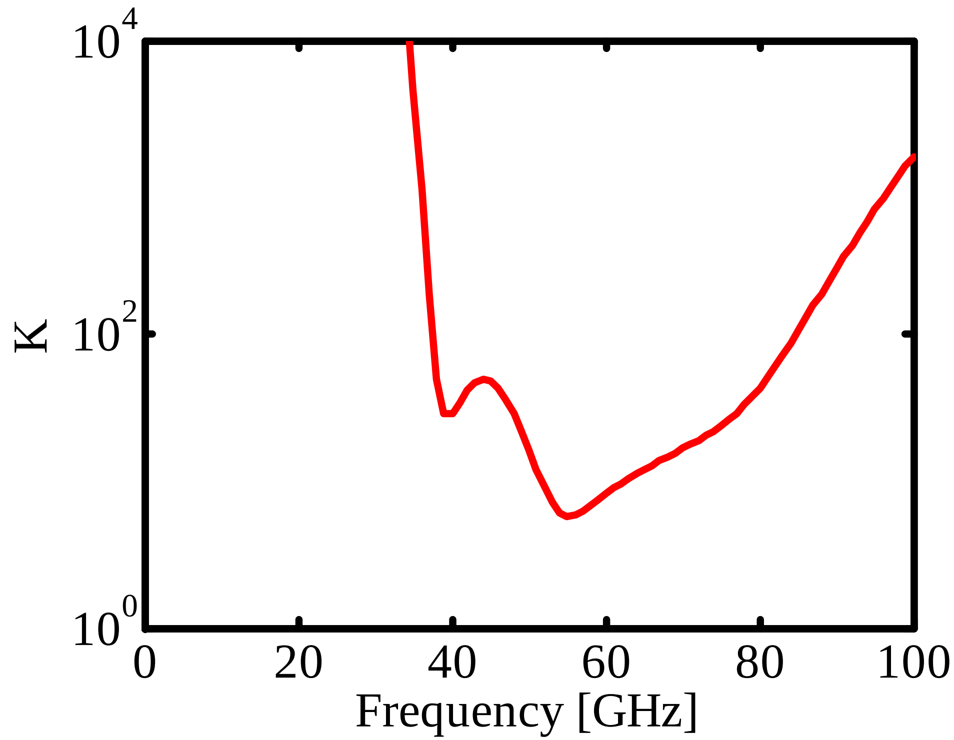





- **Multi-stage**
  - **Higher gain**
- **Dual noise-matching topology**
  - **Lower noise**

# Stability

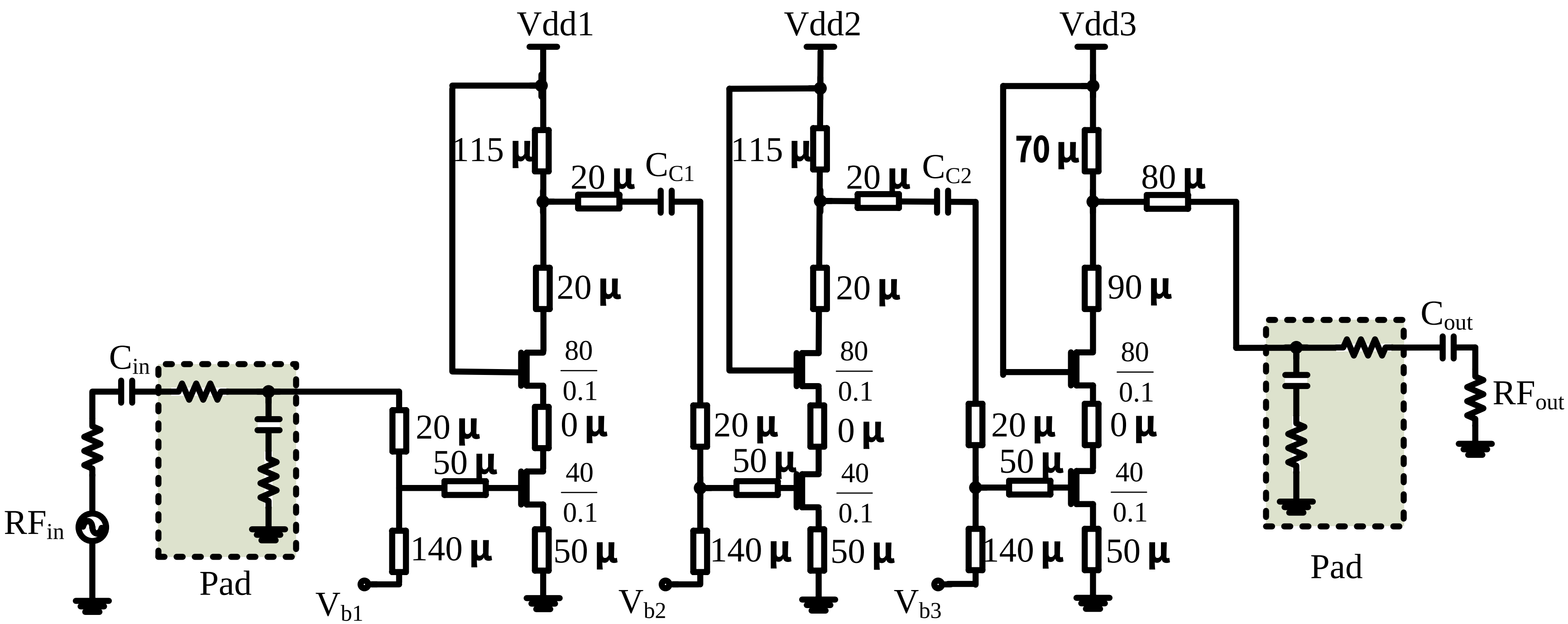
Common source is much more sensitive to process variations arising from the bilateral nature of the device.




- **Input matching**
- **Careful layout**

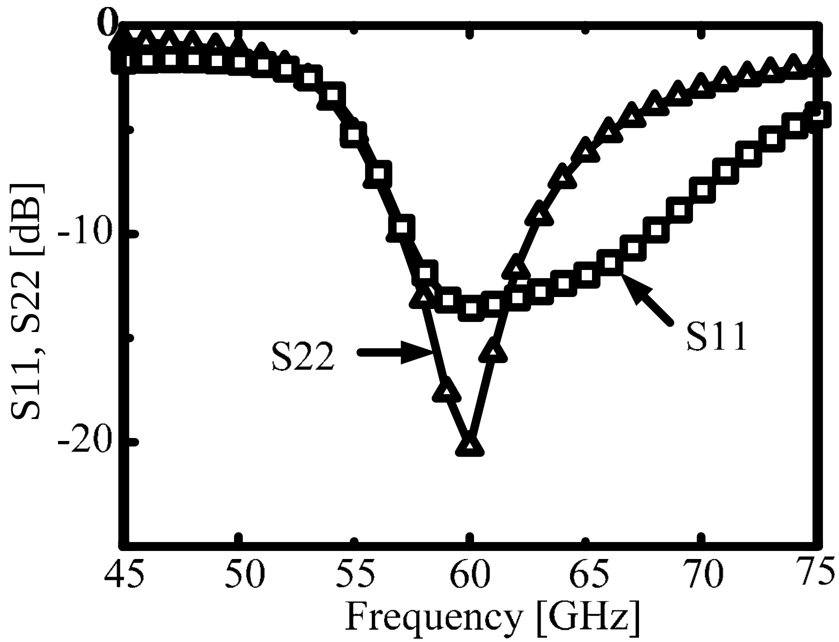
**Circuit is unconditionally stable from DC to 100GHz.**

# For Comparing…

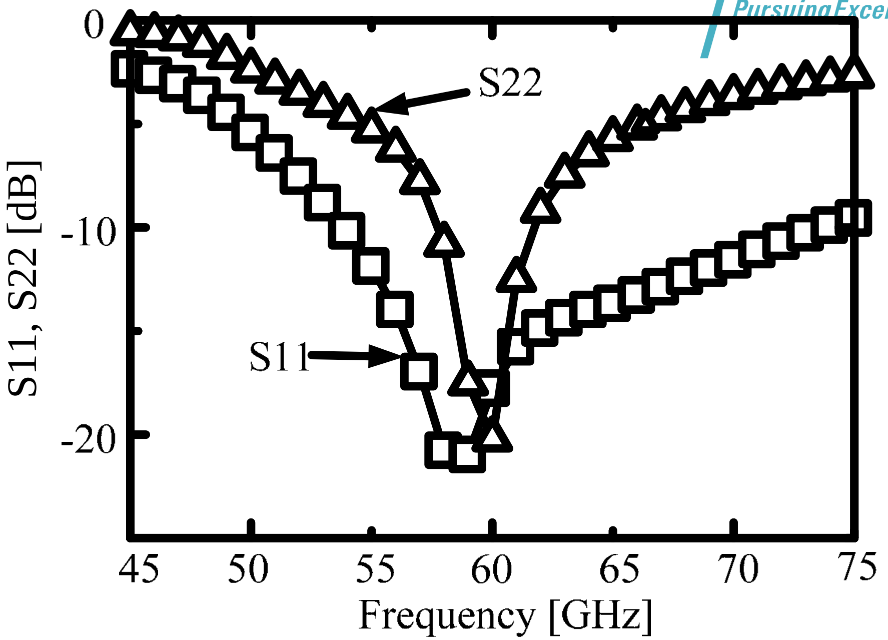



- **The same stage used**
- **Cascode topology**

# Simulation Results – S11, S22




**Proposed**



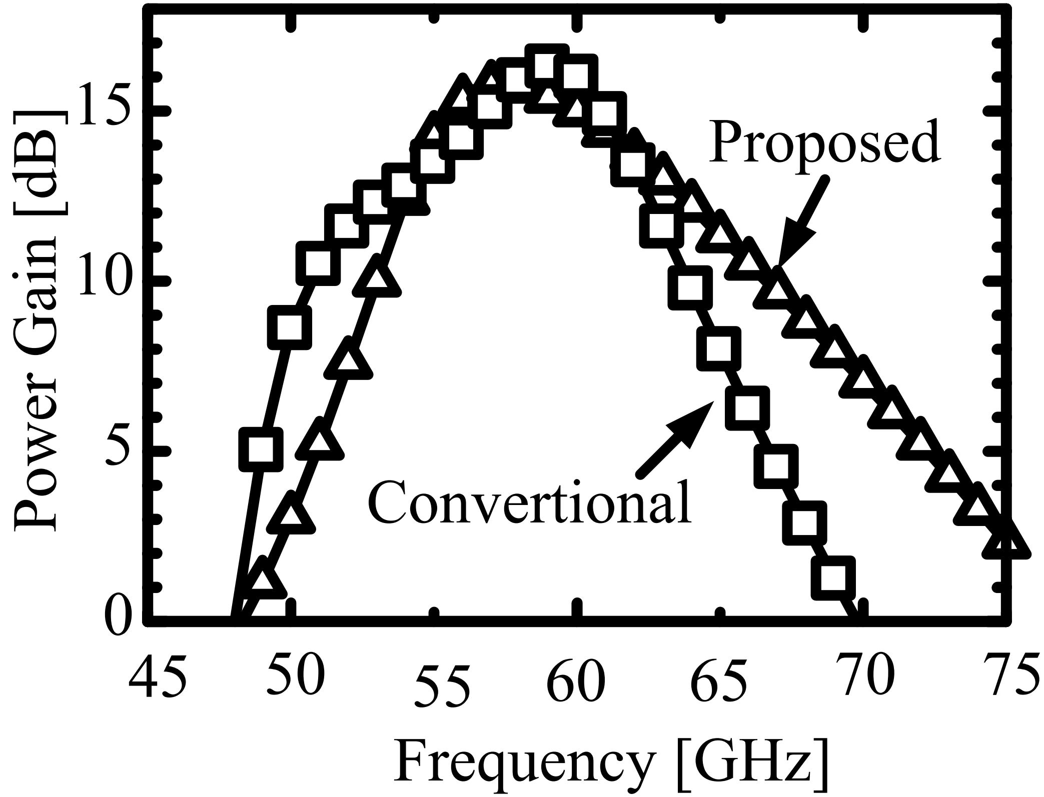

**Conventional**

◆ **7GHz bandwidth in Japan**

| 59GHz~66GHz | Proposed | Conventional |
|---|---|---|
| S11 | <-11.4dB | <-13.3dB |
| S22 | <-5.1dB | <-5.7dB |

# Simulation Results – Power Gain



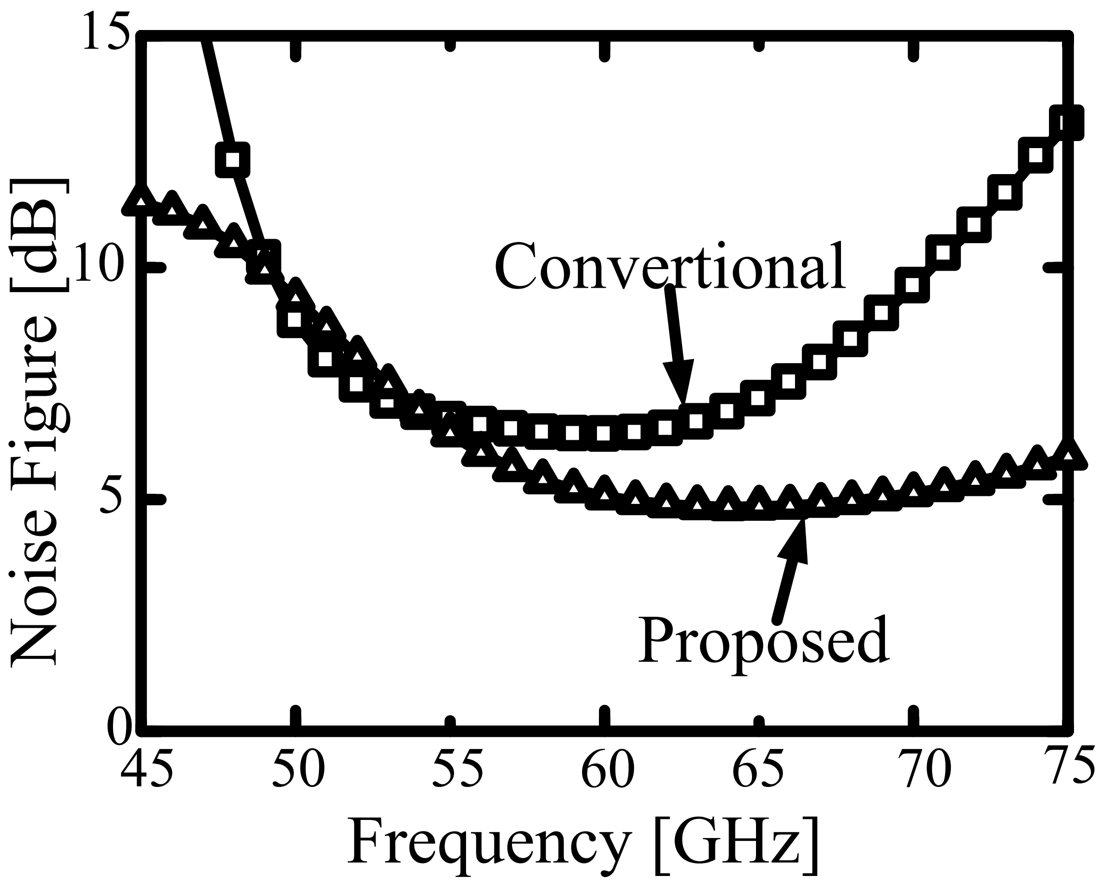



| | Proposed | Conventional |
|---|---|---|
| **Gain** | **15dB** | **16dB** |

# Simulation Results -- NF








| | Proposed | Conventional |
|---|---|---|
| NF | 5dB | 6.4dB |

# Performance Comparison



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| | Simulation | | Measurement | | | | |
|---|---|---|---|---|---|---|---|
| | Proposed | Conv. | [1] | [2] | [3] | [4] | [5] |
| Technology | 90nm CMOS | 90nm CMOS | 90nm CMOS | 90nm CMOS | 90nm CMOS | 90nm CMOS | 65nm CMOS |
| Topology | dual-CS | cascode | CS | cascode | cascode | CS | cascode |
| Gain [dB] | **15** | **16** | 15 | 14.6 | 15.5 | 12.2 | 22.3 (diff.) |
| NF [dB] | **5.0** | **6.4** | 4.4 | 5.5 (sim) | 6.5 | 6 (sim) | 6.1 |
| Power [mW] | **22** | **19** | 3.9 | 24 | 86 | 10.5 | 35 |

**Reference:**

**[1] Emanuel Cohen, et al., RFIC, pp. 61-64, 2008. [2] Terry Yao, et al., IEEE JSCC, vol. 42, no. 5, pp. 1044-1057, 2007. [3] Stefano Pellerano, et al., ESSCIRC, pp. 352-355, 2007. [4] Babak Heydari, et al., IEEE JSCC, vol. 42, no. 12, pp. 2893-2903, 2007. [5] Christopher Weyers, et al., ISSCC, pp. 192-192, 2008.**

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# Conclusions



- A three-stage LNA employing a dual noise-matching topology
- Noise matching optimized by using source degeneration
- A 5dB NF realized by dual noise matching technique
- Comparing with the conventional
  - ☑ 1.4dB NF improvement
  - ✘ 1dB gain decrease
  - ✘ 3mW power consumption increase

# Finally…



**Thank you !**