TOKYO TECH
Pursuing Excellence

Numerical Analysis of Asymmetric Differential Inductors

Masaki Kanemaru, Daisuke Imanishi, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

Matsuzawa & Okada Lab.

Contents

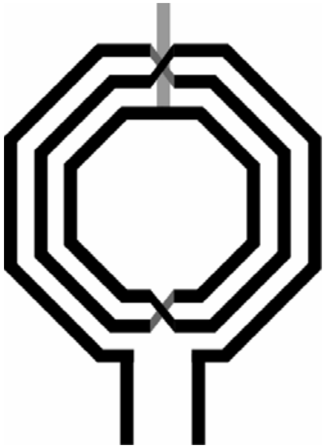
- Background
- Matrix-Decomposition Technique
- Simulation & Measurement Results
- Summary

Background

TOKYO TECH
Pursuing Excellence

Miniaturization of CMOS process
→Difficulty of characterize on-chip inductors
Degradation of circuit performances

●On-chip differential inductor
Used for LC-VCO, differential LNA, Mixer…
Mismatch between left and right halves degrades circuit performances.

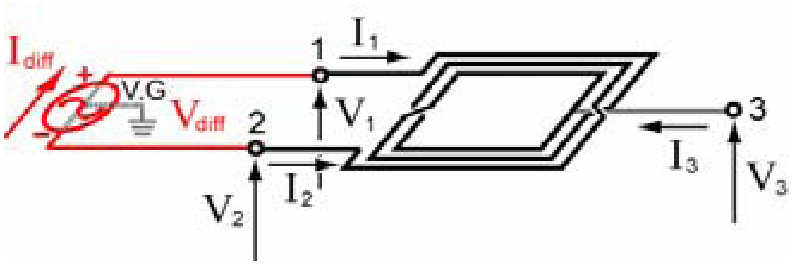


Accurate modeling of on-chip symmetric inductor
→ Extract of asymmetric parameters

Symmetric inductor analysis

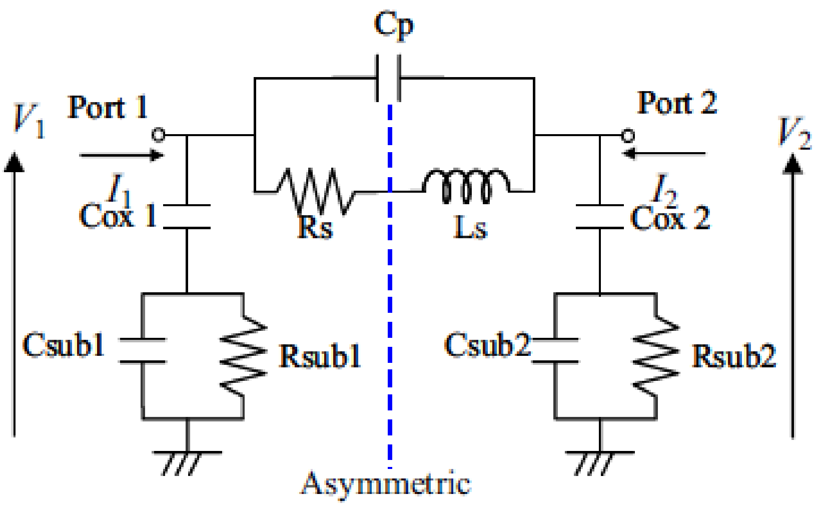
TOKYO TECH Pursuing Excellence

- 3-port symmetric inductor analysis in various operation modes [1]
  - -Circuit parameters are extracted by numerical optimization
  - -Symmetry is assumed in the parameters
- Asymmetric properties are estimated from Y11 and Y22 [2]
  - -The difference is involved in only difference in shunt parasitic components



$$Z_{\mathrm{diff}} = \frac{V_{\mathrm{diff}}}{I_{\mathrm{diff}}} = \frac{2(Y_{23}+Y_{13})}{Y_{23}(Y_{11}-Y_{12})-Y_{13}(Y_{21}-Y_{22})}$$

$$\therefore L_{\mathrm{diff}} = \frac{1}{\omega}\mathrm{Im}(Z_{\mathrm{diff}}) \qquad Q_{\mathrm{diff}} = \frac{\mathrm{Im}(Z_{\mathrm{diff}})}{\mathrm{Re}(Z_{\mathrm{diff}})}$$

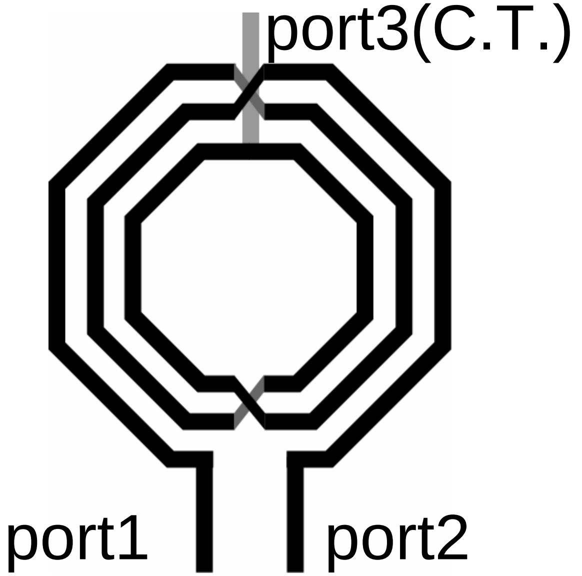


[1] K. Okada, *et al.*, EuMC, Oct. 2007, pp. 520– 523.

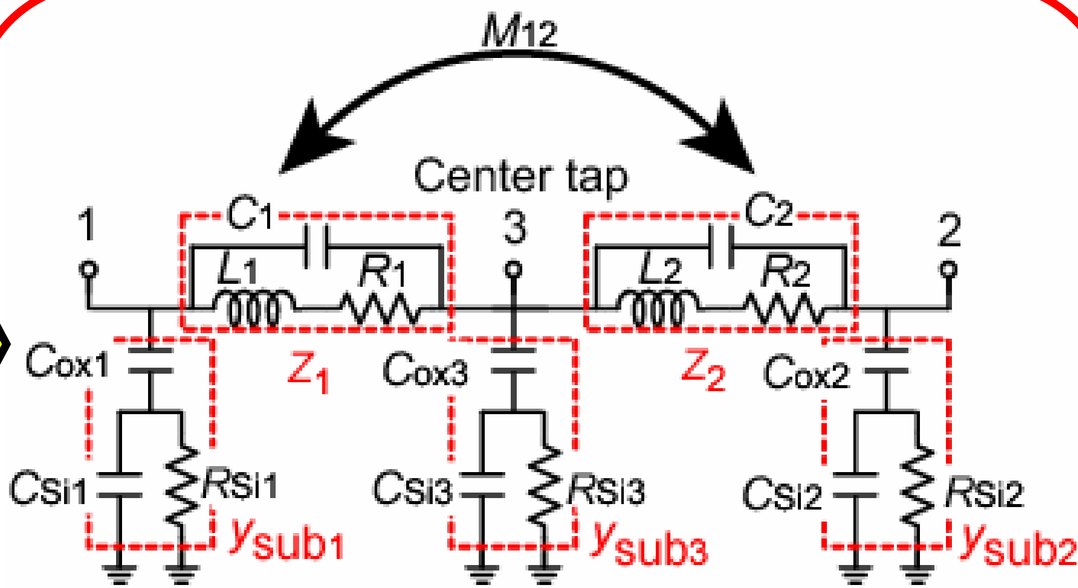
[2] Y. Aoki, *et al.*, EuMC, Oct. 2007, pp. 339–342.

Proposed method

by Matrix-Decomposition Technique



3port S-parameter



Extract π–type equivalent circuit

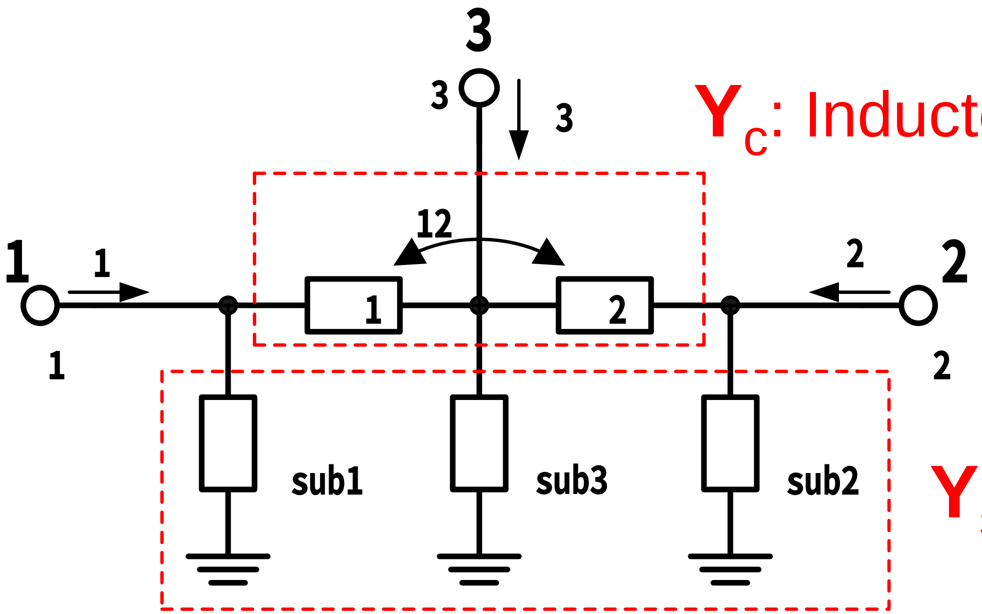
- Physically reliable parameters can be extracted.
- The mismatch can be accurately evaluated.

Contents

- Background
- Matrix-Decomposition Technique
- Simulation & Measurement Results
- Summary

Overview

$$\mathbf{Y}_{\mathrm{meas}} = \mathbf{Y}_{\mathrm{c}} + \mathbf{Y}_{\mathrm{sub}}$$



$\mathbf{Y}_{\mathrm{c}}$: Inductor core

$$\mathbf{i} = \begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} = \mathbf{Y}_{\mathrm{meas}} \begin{pmatrix} v_1 \\ v_2 \\ v_3 \end{pmatrix} = \mathbf{Y}_{\mathrm{meas}} \mathbf{v}$$

$\mathbf{Y}_{\mathrm{sub}}$: Interlayer-dielectric and Si substrate

- All ports have common voltages
  $\mathbf{Y}_{\mathrm{c}}$ can be ignored → $\mathbf{Y}_{\mathrm{sub}}$ is calculated from $\mathbf{Y}_{\mathrm{meas}}$
- $\mathbf{Y}_{\mathrm{c}}$ is calculated from $\mathbf{Y}_{\mathrm{meas}}$ and $\mathbf{Y}_{\mathrm{sub}}$
- $\mathbf{Z}_{\mathrm{core}}$ is derived from $\mathbf{Y}_{\mathrm{c}}$ by converting matrix

Calculation of Y_{sub}

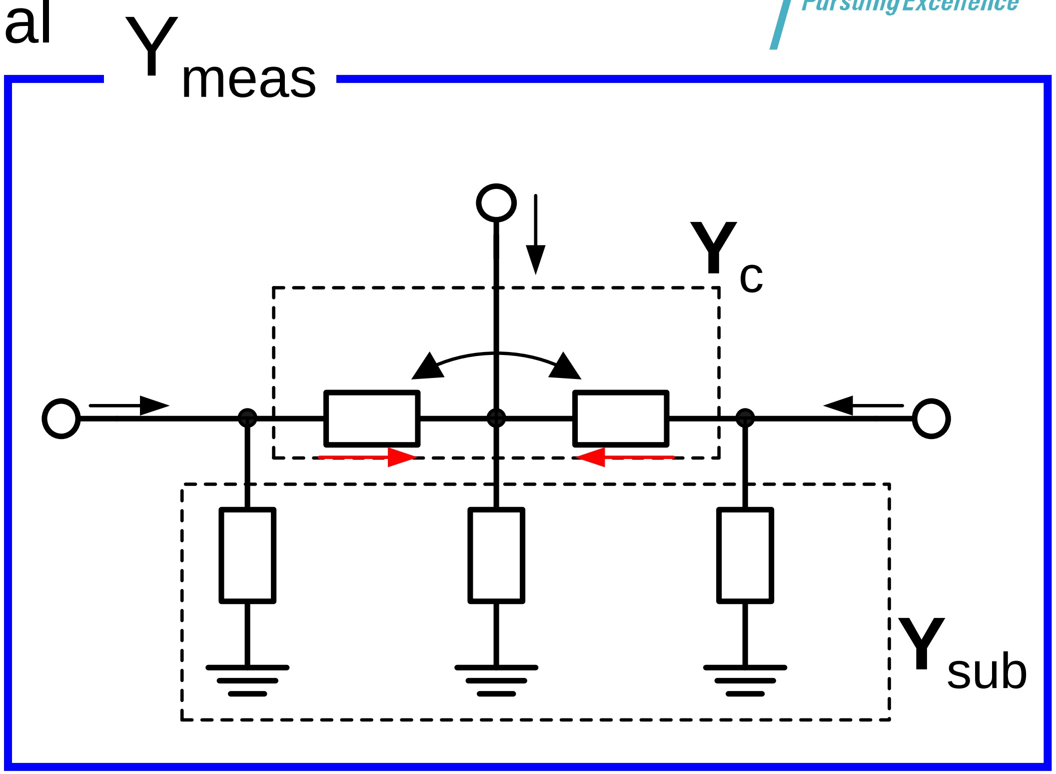
Voltages of each port are equal

→No current flows through z_n

$$\begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} = \mathbf{Y}_{meas} \begin{pmatrix} v_a \\ v_a \\ v_a \end{pmatrix}$$

$$= \mathbf{Y}_c \begin{pmatrix} v_a \\ v_a \\ v_a \end{pmatrix} + \mathbf{Y}_{sub} \begin{pmatrix} v_a \\ v_a \\ v_a \end{pmatrix}$$

$\mathbf{Y}_c \begin{pmatrix} v_a \\ v_a \\ v_a \end{pmatrix} = 0$



$$\mathbf{Y}_{sub} = \begin{pmatrix} y_{sub1} & 0 & 0 \\ 0 & y_{sub2} & 0 \\ 0 & 0 & y_{sub3} \end{pmatrix}$$

$$y_{sub1} = y_{meas11} + y_{meas12} + y_{meas13}$$
$$y_{sub2} = y_{meas21} + y_{meas22} + y_{meas23}$$
$$y_{sub3} = y_{meas31} + y_{meas32} + y_{meas33}$$

Conversion of matrix Y_c to Z_{core}

$\mathbf{Y}_c = \mathbf{Y}_{meas'} - \mathbf{Y}_{sub}$

Define $\mathbf{Z}_{core}$ by 2×2 matrix

$$\mathbf{Z}_{core} = \begin{pmatrix} z_1 & -j\omega M_{12} \\ -j\omega M_{12} & z_2 \end{pmatrix} \qquad \mathbf{v}_z = \mathbf{Z}_{core}\mathbf{i}_z$$

$\mathbf{v}_z = \mathbf{A}\mathbf{v} \quad \mathbf{i}_z = \mathbf{B}\mathbf{i}$

Obtain converting matrix **A** and **B**

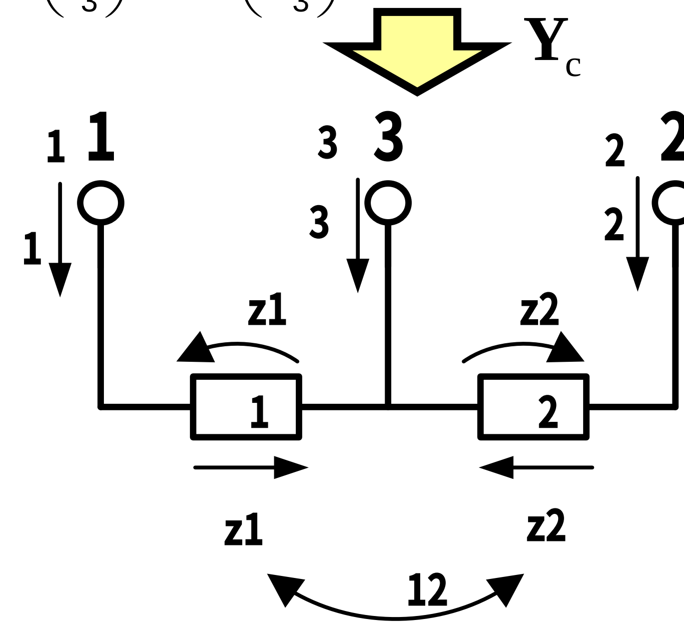
$\mathbf{B}^T$ can be $\mathbf{A}^*$ $\quad \mathbf{A}\mathbf{A}^* = \mathbf{I}$

e.g.) $\mathbf{v}_z = \begin{pmatrix} v_{z1} \\ v_{z2} \end{pmatrix} = \begin{pmatrix} v_1 - v_3 \\ v_2 - v_3 \end{pmatrix} \qquad \mathbf{i}_z = \begin{pmatrix} i_{z1} \\ i_{z2} \end{pmatrix} = \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$

$$\mathbf{A} = \begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{pmatrix} \qquad \mathbf{B} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}$$

Matrix $\mathbf{Y}_c$ is converted into matrix $\mathbf{Z}_{core}$

$$\mathbf{i} = \begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} = \mathbf{Y}_c \begin{pmatrix} v_1 \\ v_2 \\ v_3 \end{pmatrix} = \mathbf{Y}_c \mathbf{v}$$



$$\mathbf{A}\mathbf{v} = \mathbf{Z}_{core}\mathbf{B}\mathbf{i} = \mathbf{Z}_{core}\mathbf{B}\mathbf{Y}_c\mathbf{v}$$

$$\mathbf{A} = \mathbf{Z}_{core}\mathbf{B}\mathbf{Y}_c$$

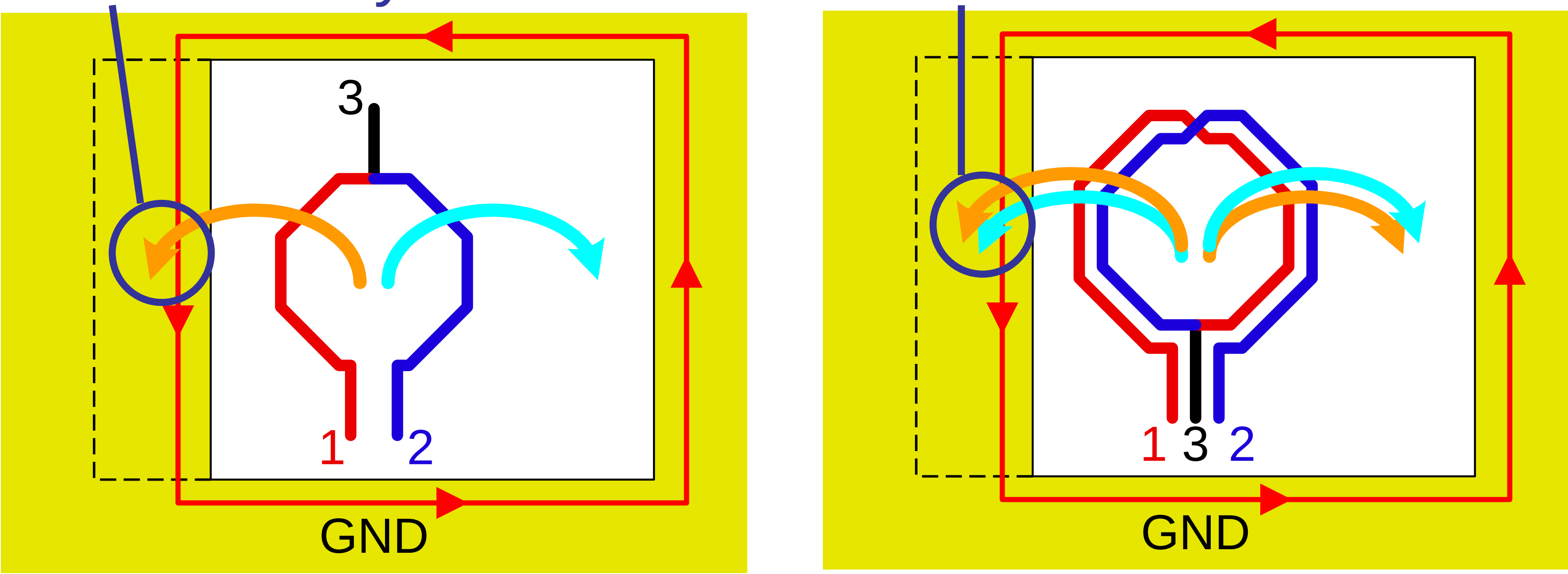
$$\Rightarrow \mathbf{Z}_{core} = (\mathbf{B}\mathbf{Y}_c\mathbf{A}^*)^{-1}$$

Contents

- Background
- Matrix-Decomposition Technique
- Simulation & Measurement Results
- Summary

Mismatch of ground loop

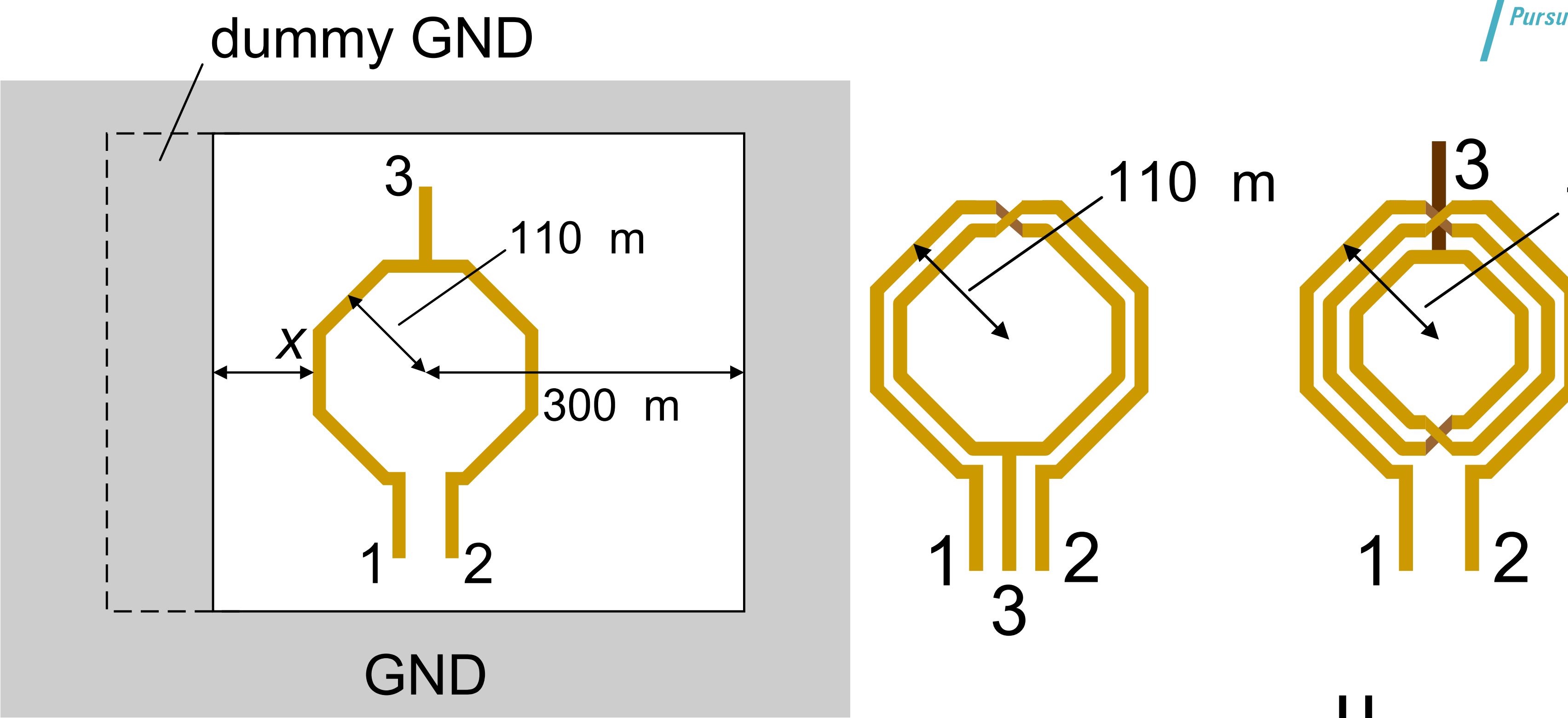
Flux loss: Only half side Flux loss: Both sides



The inductance mismatch depends on the number of turns.

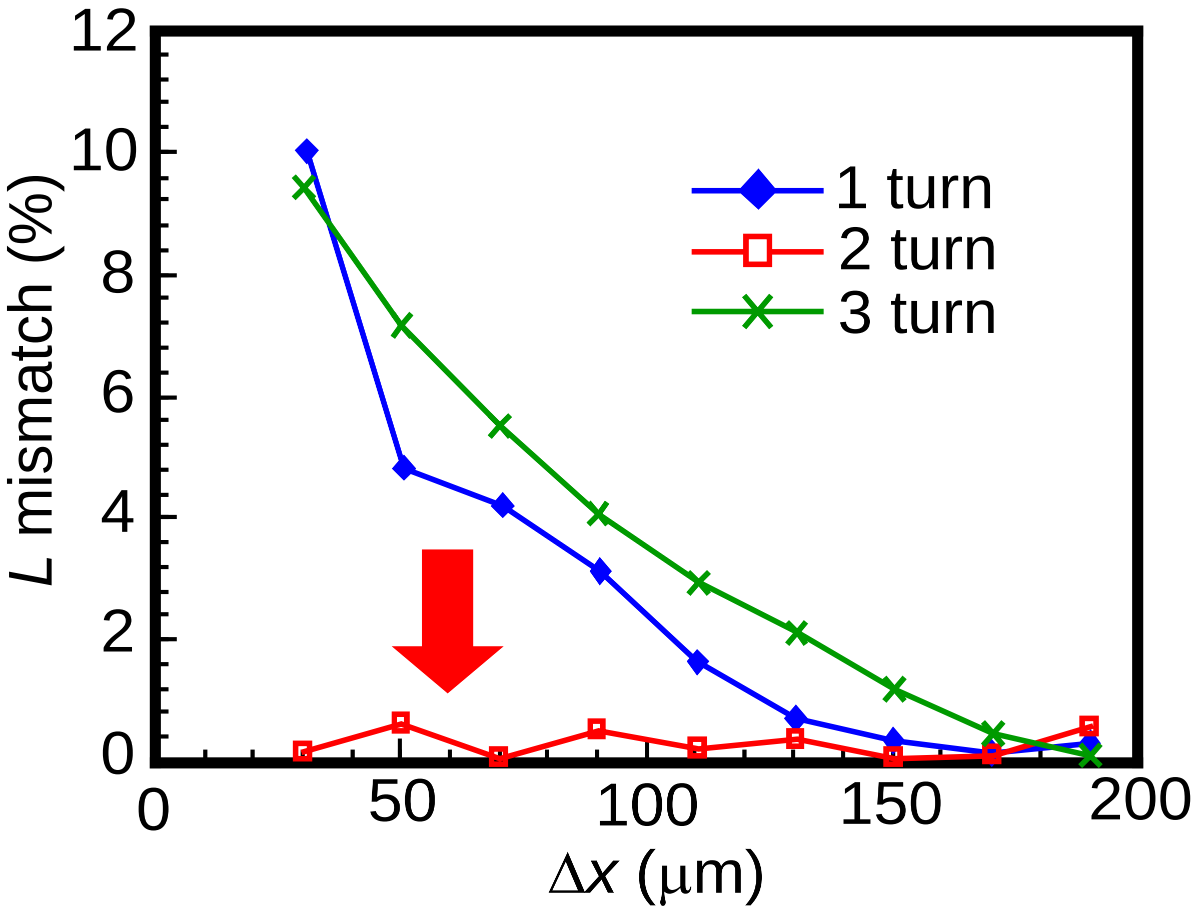
Odd ⇨	Each loss is different ⇨	Mismatch ↑
Even ⇨	Each loss is almost equal ⇨	Mismatch ↓

Simulation model



- Inductance mismatches are evaluated by the proposed method.
- The mismatches are plotted as a function of Δ*x*.

Simulation Result

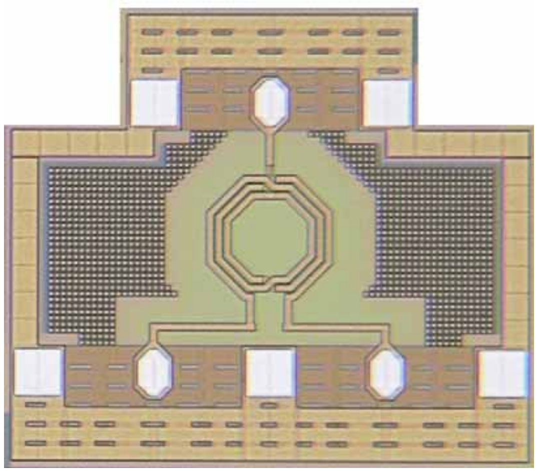


- The mismatch of 2-turn is smaller than 1- and 3-turn
- Increasing Δx, mismatch decreases

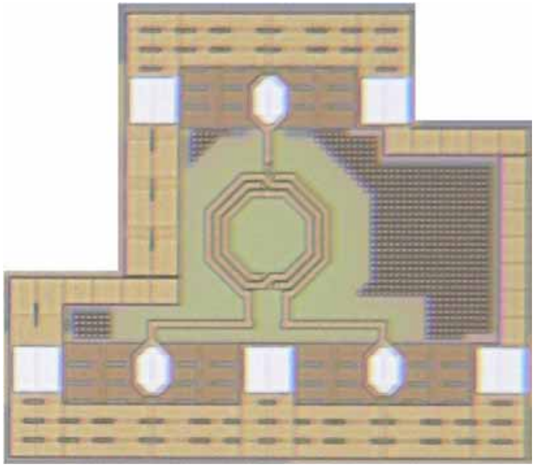
Measurement

0.18 μm Si-CMOS

Line width：9μm, Line space:2μm
Inner diameter:100μm, Turn:3



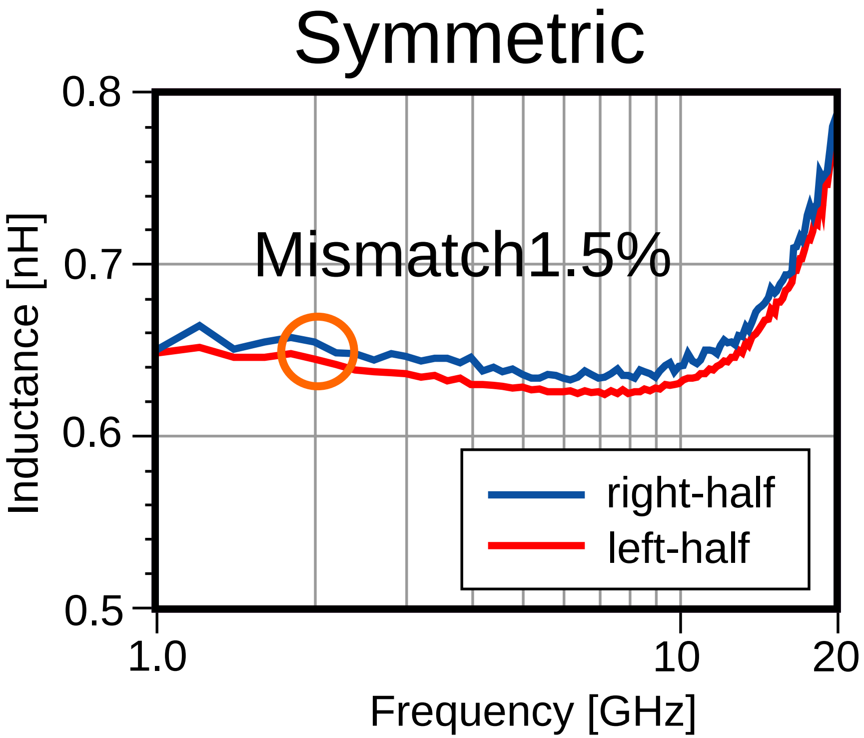
Symmetric

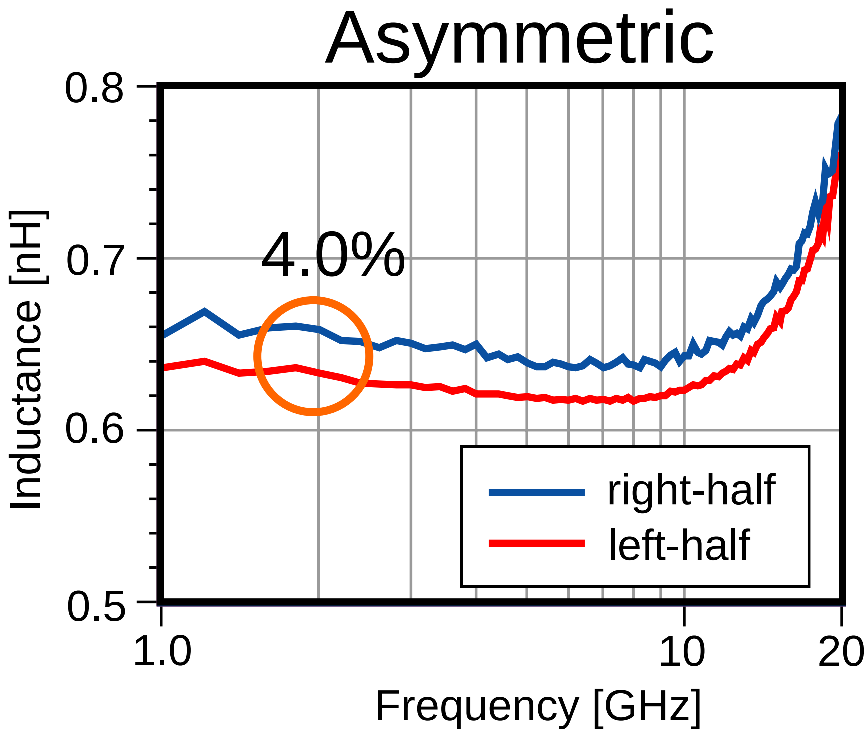


Asymmetric

VNA : 4port 10MHz-67GHz
E8361A+N4421BH67(Agilent)
Probe : I67-D-GSGSG-150 (Cascade)
I67-GSG-150 (Cascade)

Measurement Result





- Influence of asymmetric ground loop is extracted
- Other reasons to cause asymmetry exist

Contents

- Background
- Matrix-Decomposition Technique
- Simulation & Measurement Results
- Summary

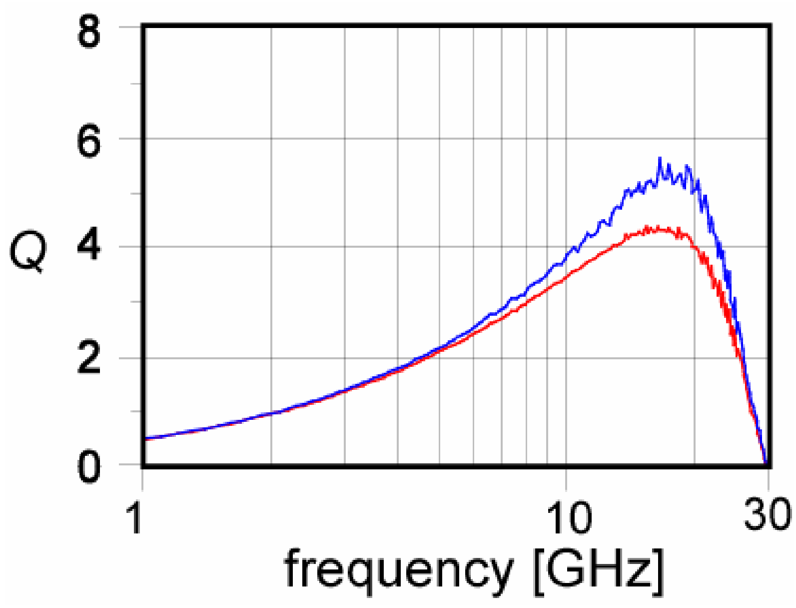
The numerical analysis using the matrix-decomposition technique is proposed

- Physically reliable parameter can be extracted
- The mismatch can be accurately evaluated

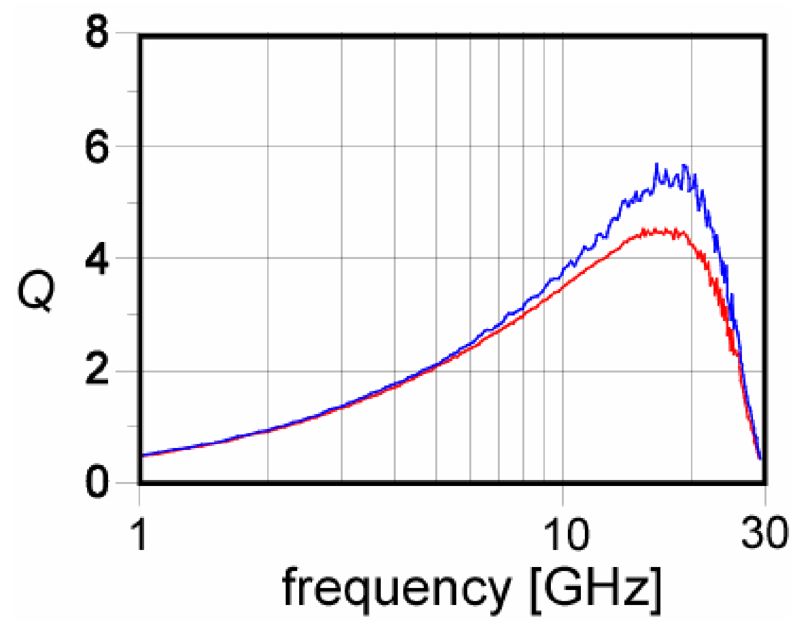
Proposed method is applied to 1-, 2-, and 3-turn differential inductors

Influence of asymmetric ground loop can be accurately extracted

Q factor

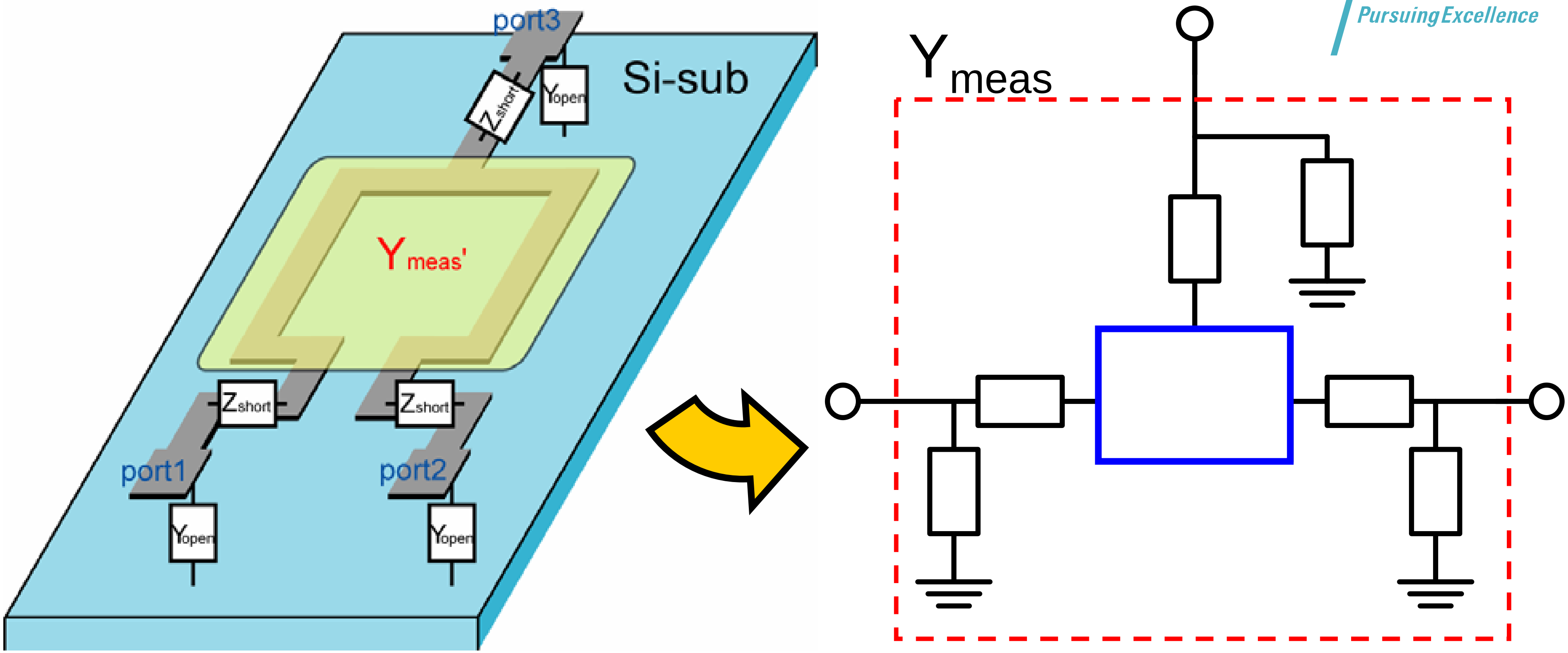


Symmetric



Asymmetric

Extract $Y_{meas'}$



- Z_{short} and Y_{open} are removed by Open-Short de-embedding

$$\mathbf{Z}_{meas'} = (\mathbf{Y}_{meas} - \mathbf{Y}_{open})^{-1} - (\mathbf{Z}_{short} - \mathbf{Y}_{open})^{-1}$$

$$\mathbf{Y}_{meas'} = \mathbf{Z}_{meas'}^{-1}$$