カレントスティーリングDACの動的特性の調査

Recent studies on the dynamic behavior of current-steering DACs

東京工業大学　大学院
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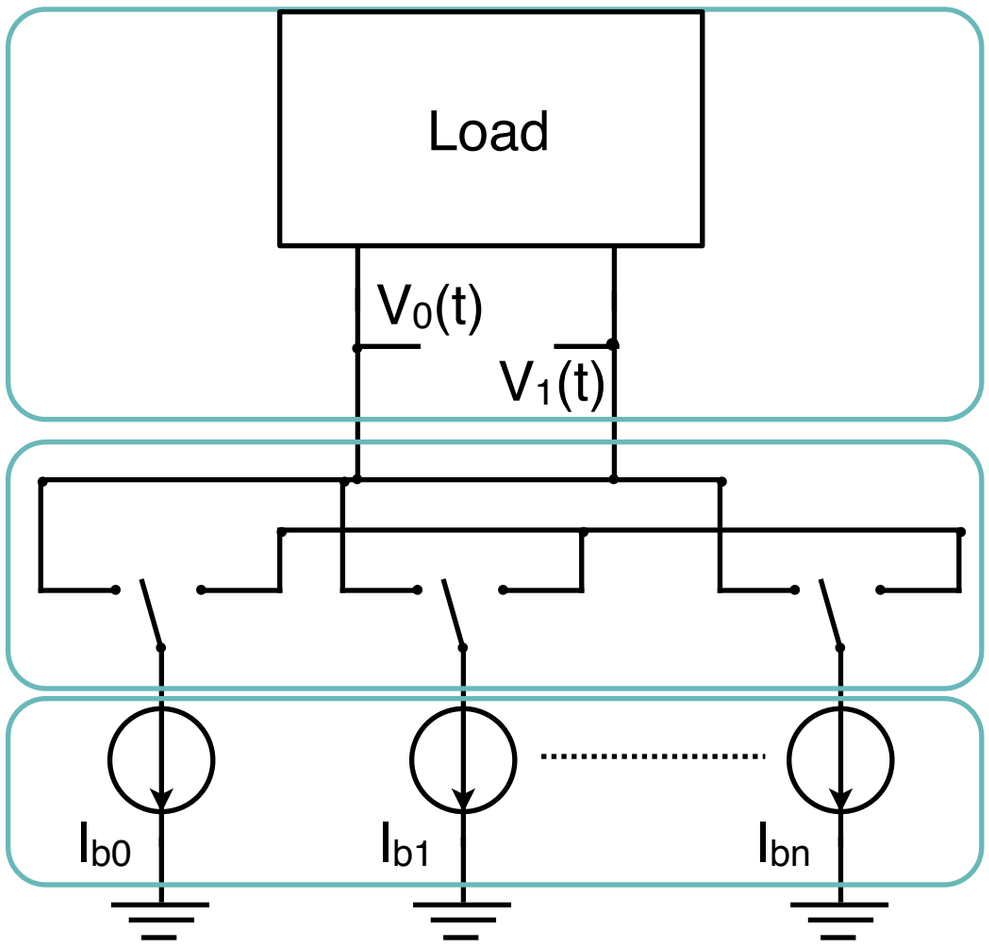
Matthias Frey and Akira Matsuzawa

Motivation, Background

- What is a current-steering DAC?

ideal:

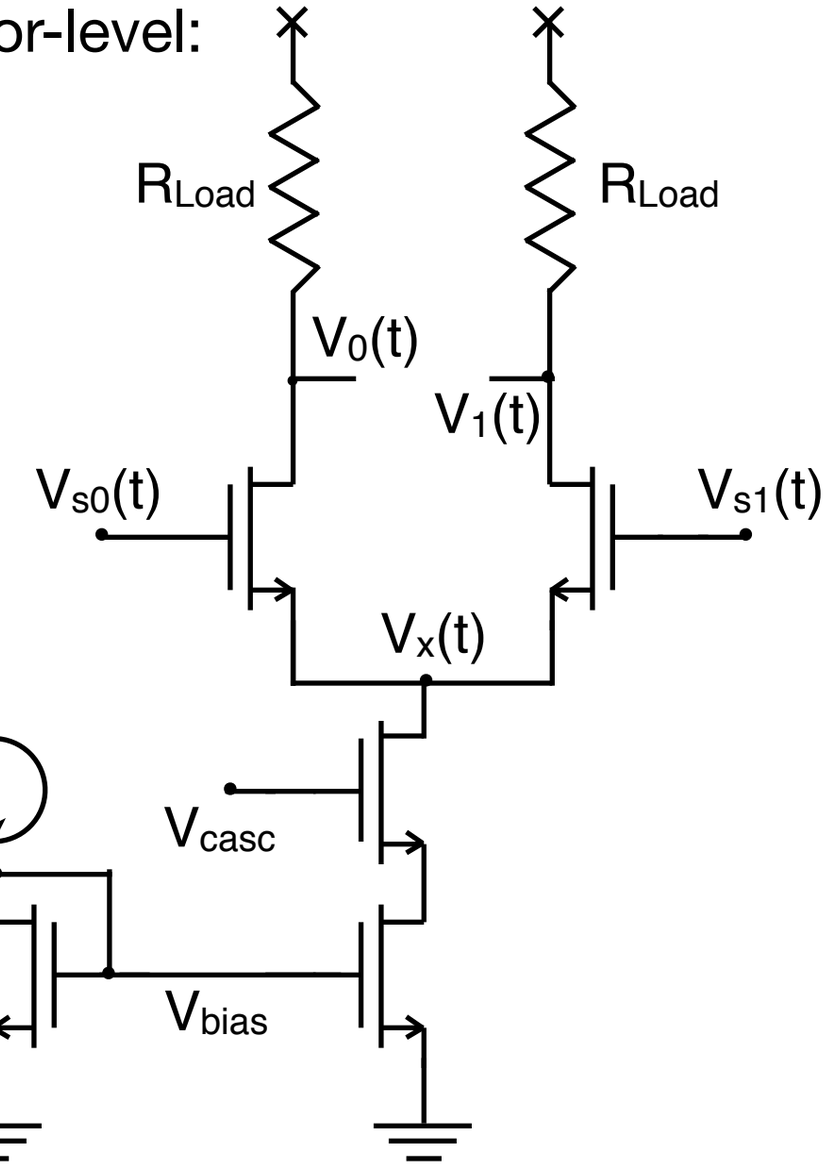


resistive load for current-to-voltage conversion

switches

scaled current sources

transistor-level:

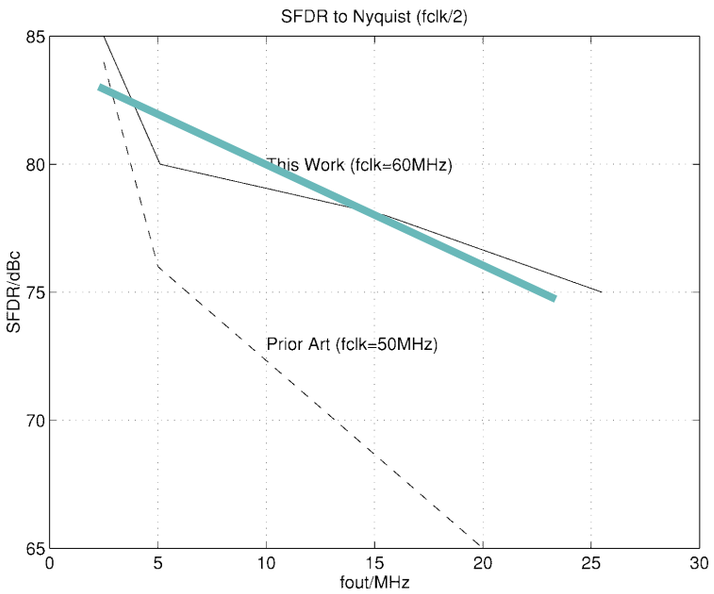


Motivation

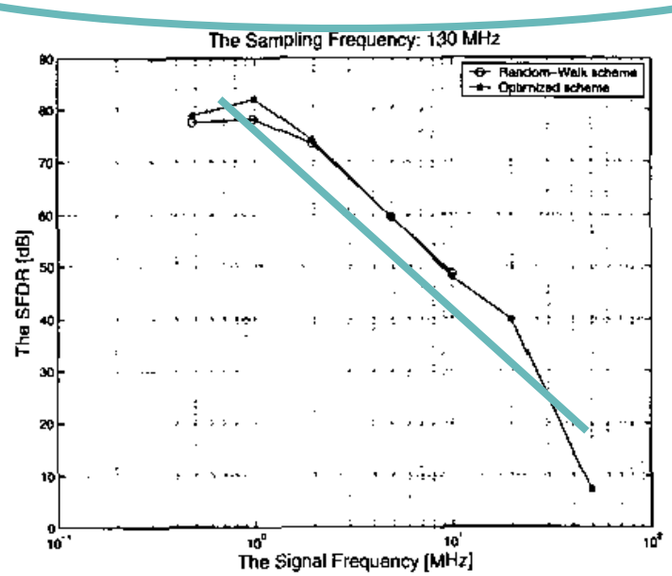
- Why should we care about dynamic properties?
  ...and not only about INL/ DNL?

SFDR vs. Signal Frequency

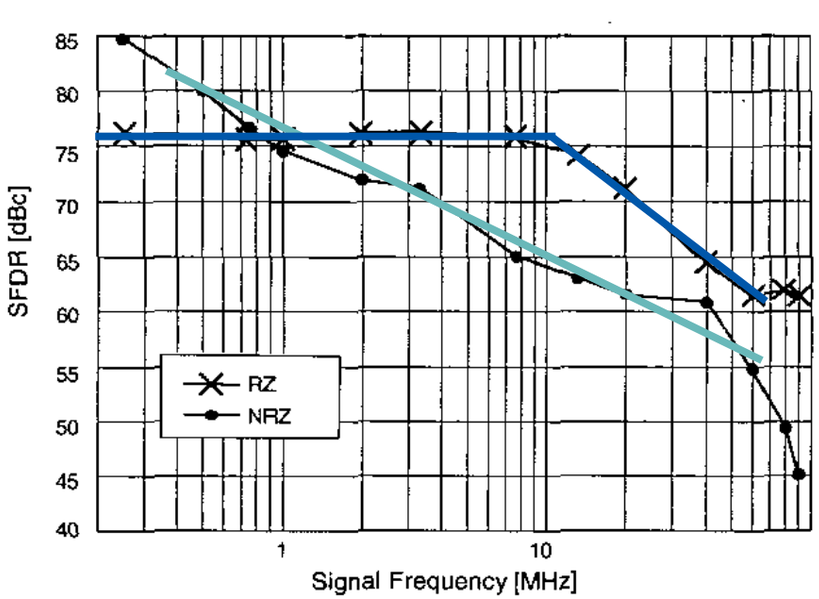
...later!



from:
Bugeja et al., "*14-b, 100-MS/s CMOS DAC for spectral performance*",
JSSC 1999



from:
T. Chen, et al., "*A 14-bit 130-MHz CMOS Current-Steering DAC with adjustable INL*",
ESSCC 2004



from:
Q. Huang, "*Low Voltage and Low Power Aspects of Data Converter Design*",
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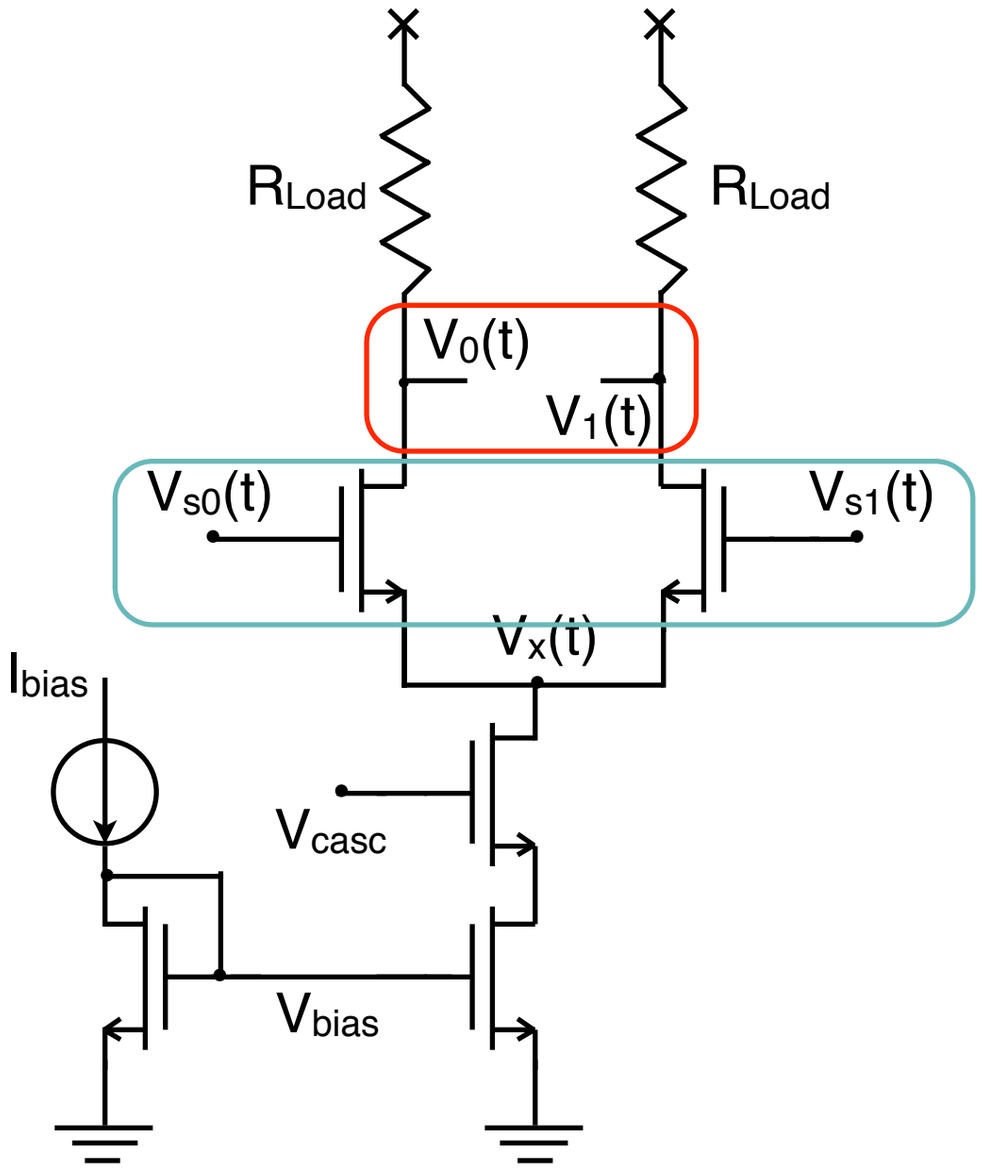
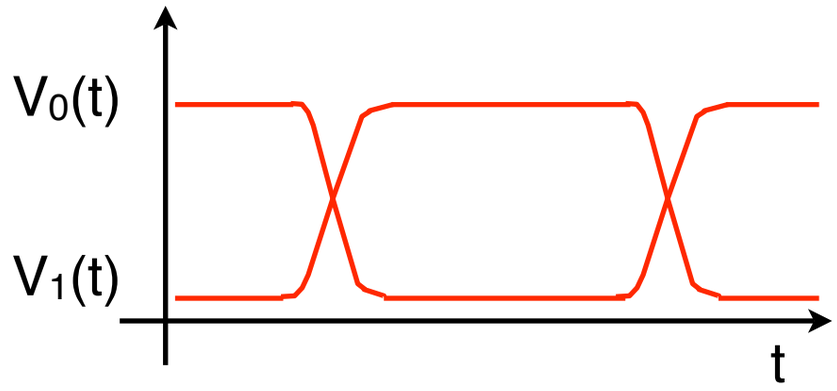
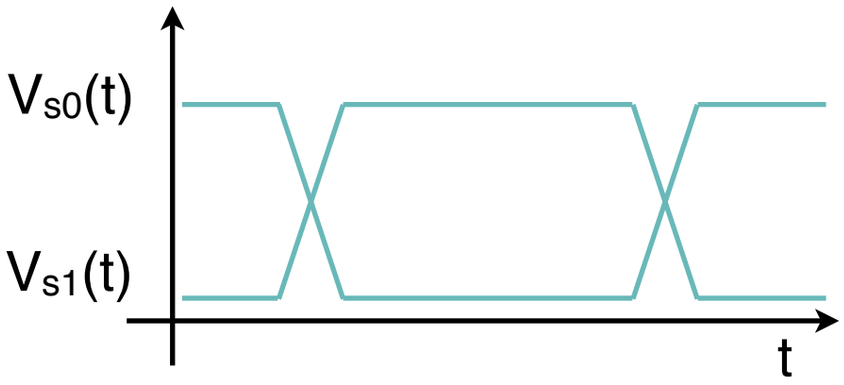
Motivation

- Switching in Current Steering DACs:



ideally:





Motivation

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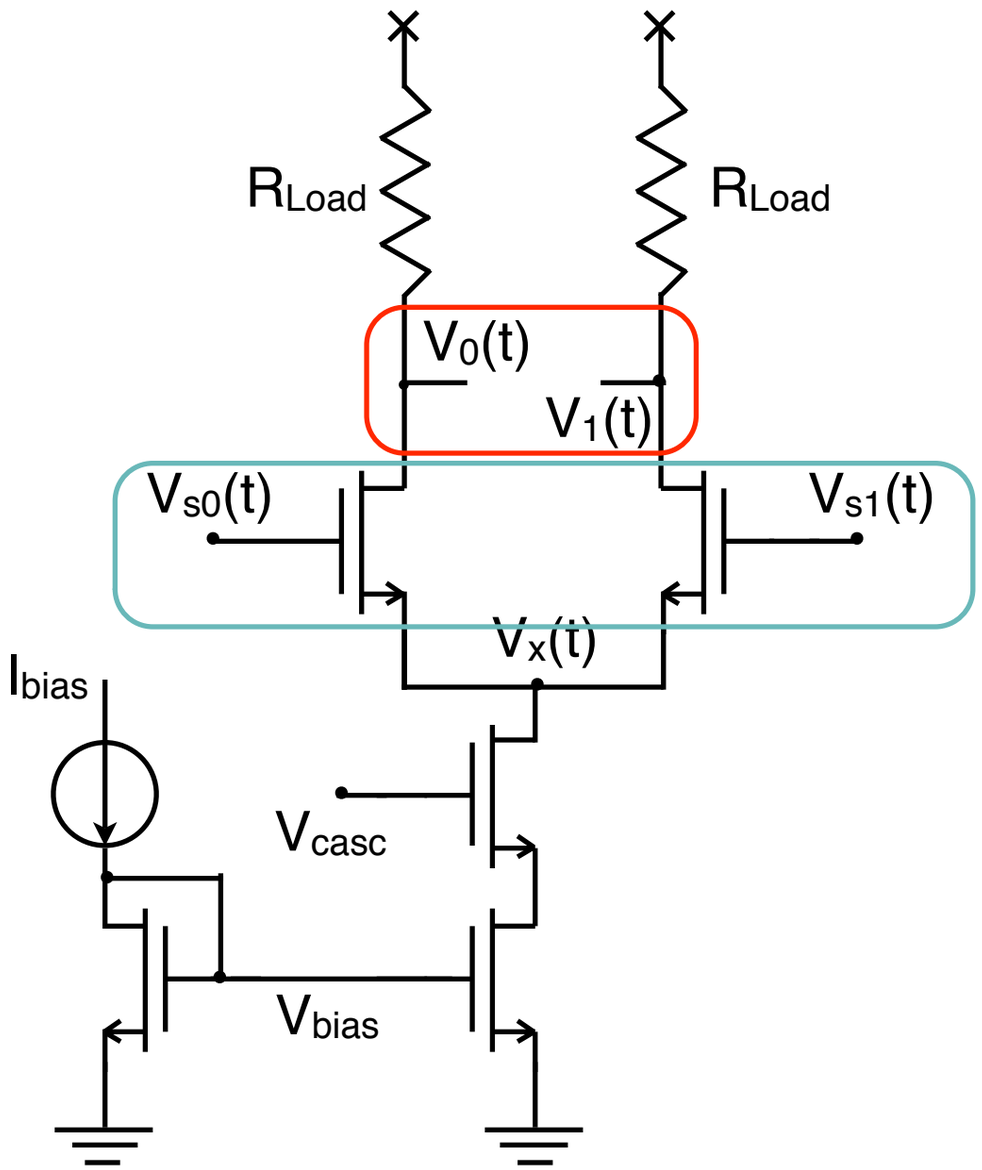
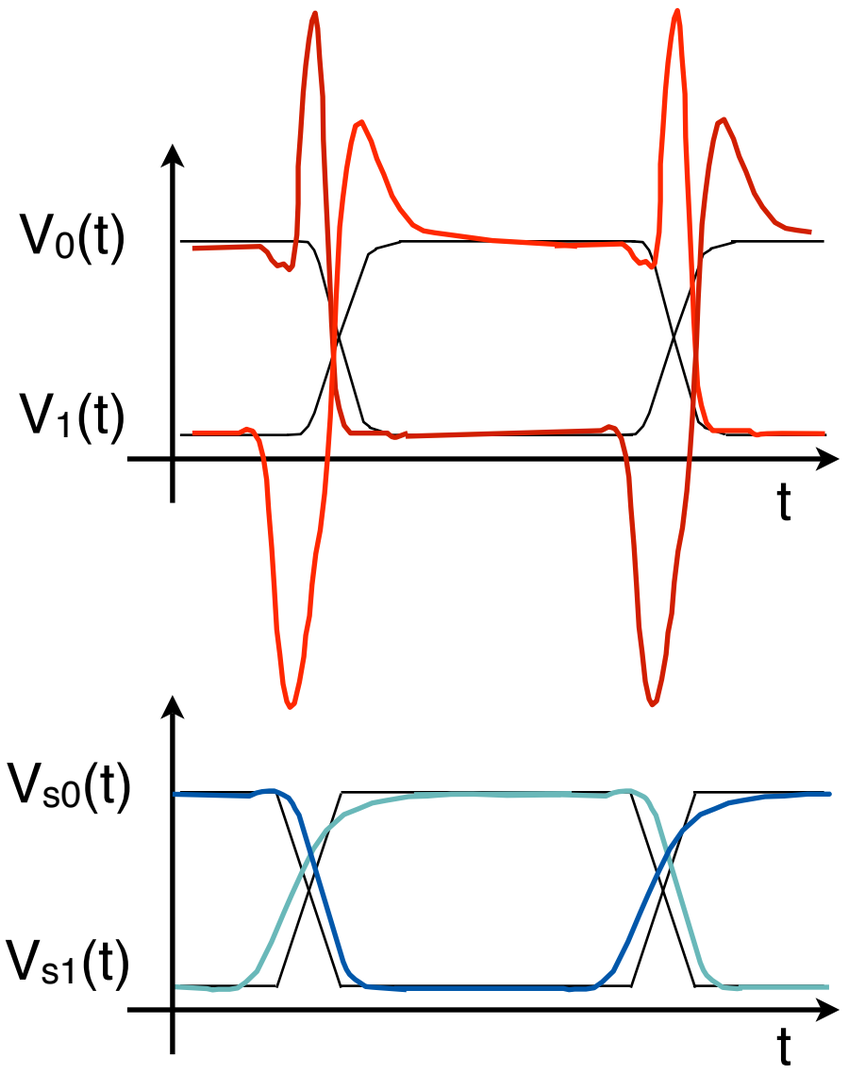


realistic:



Part I: Origin of reduced SFDR

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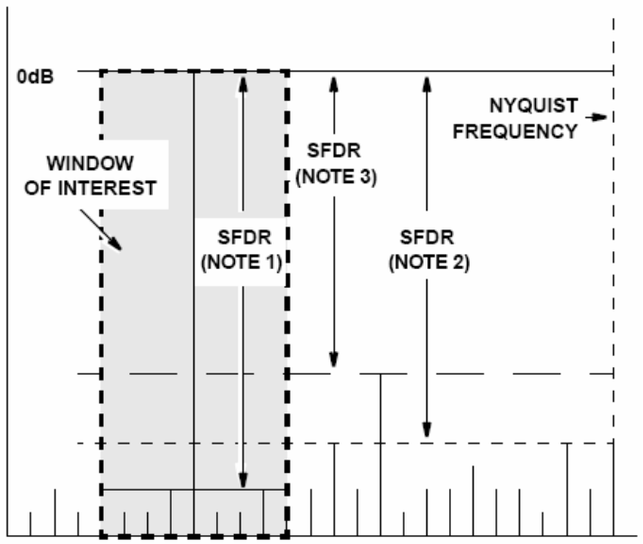
- Switching Delay Differences:
  - Output-Dependent Delay Difference
  - Cell-Dependent Delay Difference

- Errors Introduced while Switching:
  - Switching Crossover
  - Charge Feed-through

- Resampling Circuits
  - Non-Return-to-Zero vs. Return-to-Zero
  - Dual Return-to-Zero Circuit

Preliminaries: One Definition

- SFDR: **S**purious **F**ree **D**ynamic **R**ange



from: E. Balestrieri, et al., "Some critical notes on DAC frequency domain specifications", IMEKO, 2006.

  - many definitions of SFDR exist!
  - many definitions of Spur exist, e.g., "non-harmonic", "any non-signal component"
  - various frequency bands of interest
  - SFDR is generally a function of input-signal frequency and amplitude, and sampling frequency

Switching Delay Differences

- Cell-Dependent Delay Differences:
  - delay differences between current-sources is one of the main differences for bad SFDR.
  - delay determined by position of the current-cell in the layout
  - model discussed:
    - linearly-distributed delays are considered
    - maximum delay difference: d_{max}

discussed in:
T. Chen and G. Gielen,
"*The analysis and improvement of a current-steering DAC's dynamic range-I: The cell-dependent delay differences*", Jan. 2006.

Switching Delay Differences

- Cell-Dependent Delay Differences: Main results:
  - "worst case scenario": $f_0 \leq \frac{2}{\pi d_{\max} 10^{(6.02N+1.76)/20}}$

    e.g.: 10 bits DAC, d_{max} = 100 ps

    ⇒ max. signal frequency: f_0 < 5 MHz

  - The distribution of the delay values has the greatest impact on the SFDR, rather than the values itself.

    ⇒ switching sequence needs to be optimized

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Switching Delay Differences

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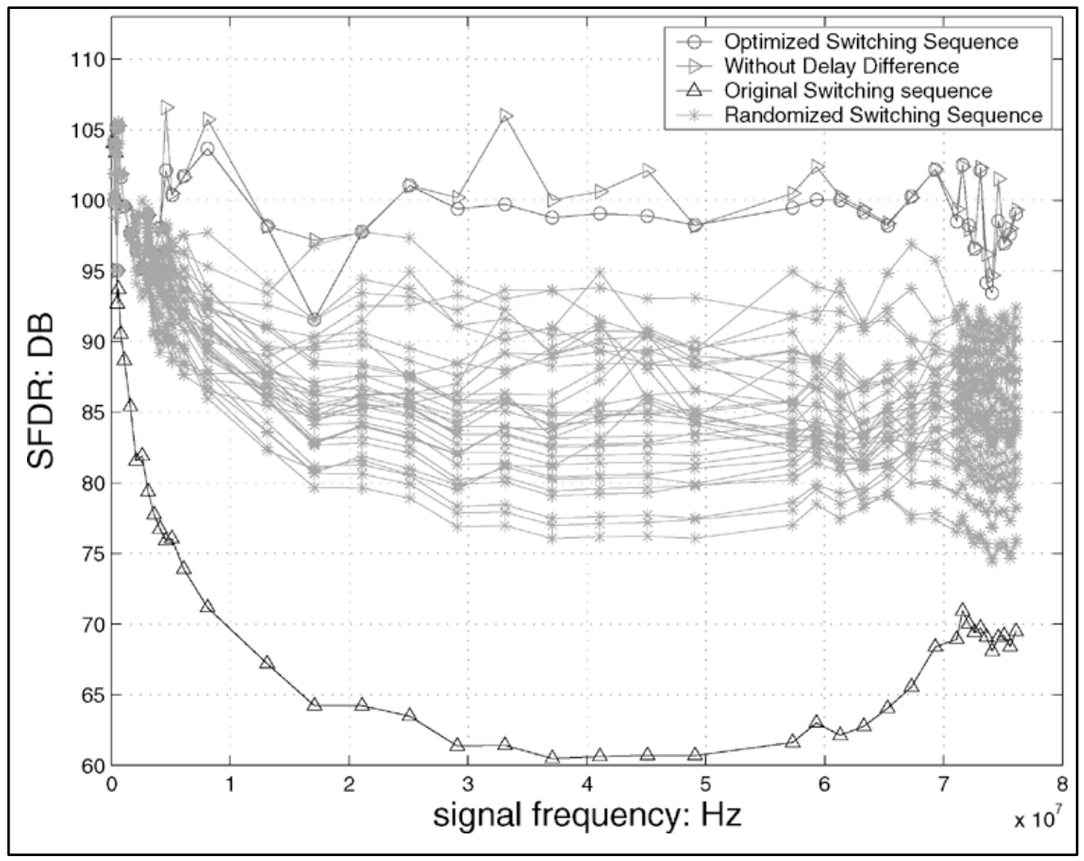

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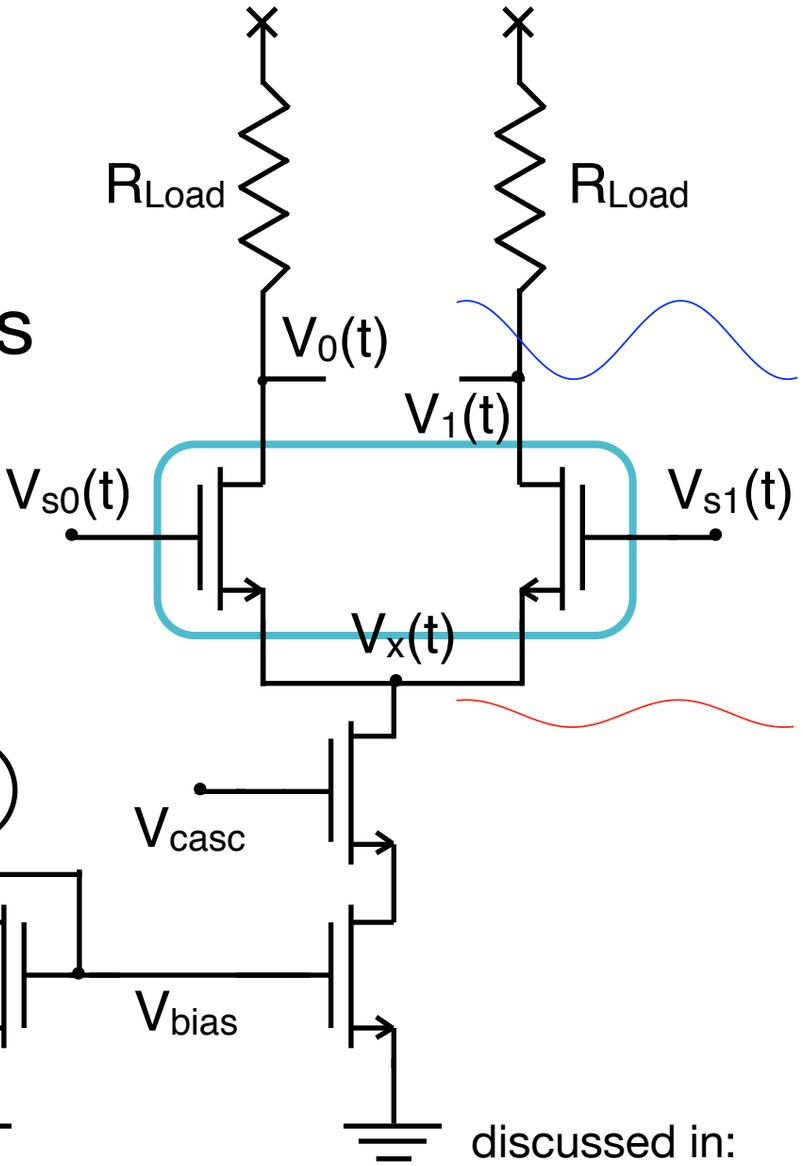
Switching Delay Differences

- Output-Dependent Delay Differences:
  - Origin:
    - A transistor switches at $V_{gs} = V_{th}$
    - Because of the Switch-transistor's limited ($g_m \cdot r_0$):
      $\mathbf{V_x(t)} = f(\mathbf{V_0(t)}, \mathbf{V_1(t)}, V_{s0}(t), V_{s1}(t))$



- $V_x(t) \approx V_0 / (1 + g_m r_0)$

  g_m, r_0: transconductance and output resistance of the switch transistor

discussed in:
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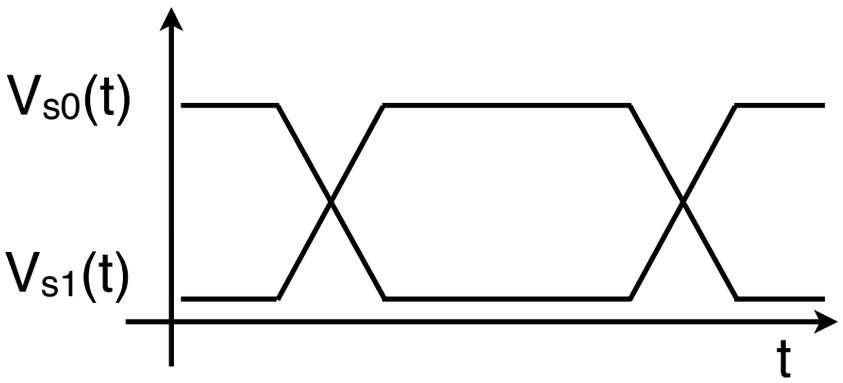
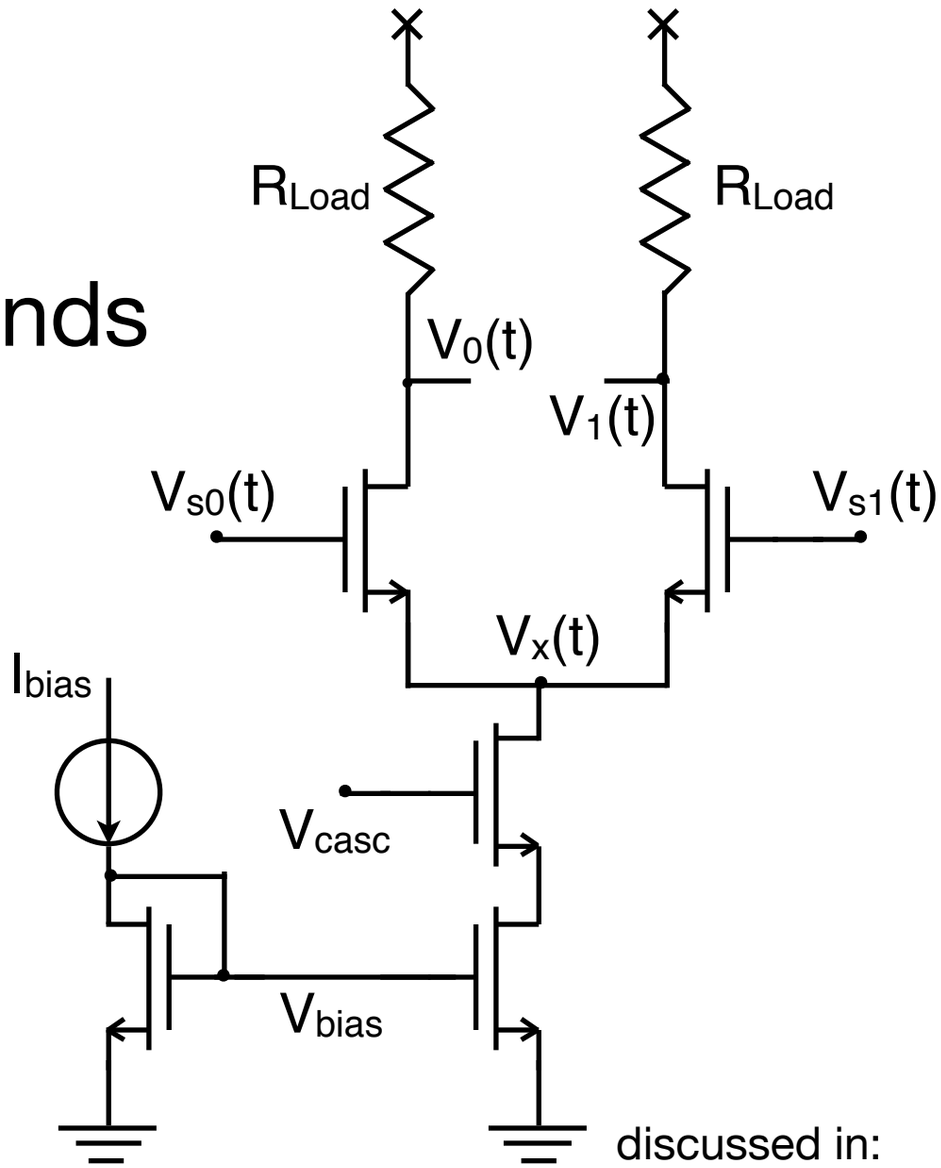
Switching Delay Differences

- Output-Dependent Delay Differences:
  - As the clock-signals $V_{si}(t)$ have a finite slope and
  - the source voltage $V_x(t)$ depends on the output voltage, $V_i(t)$,

  $\Rightarrow$ the switch-delay depends on the output voltage.





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Switching Delay Differences

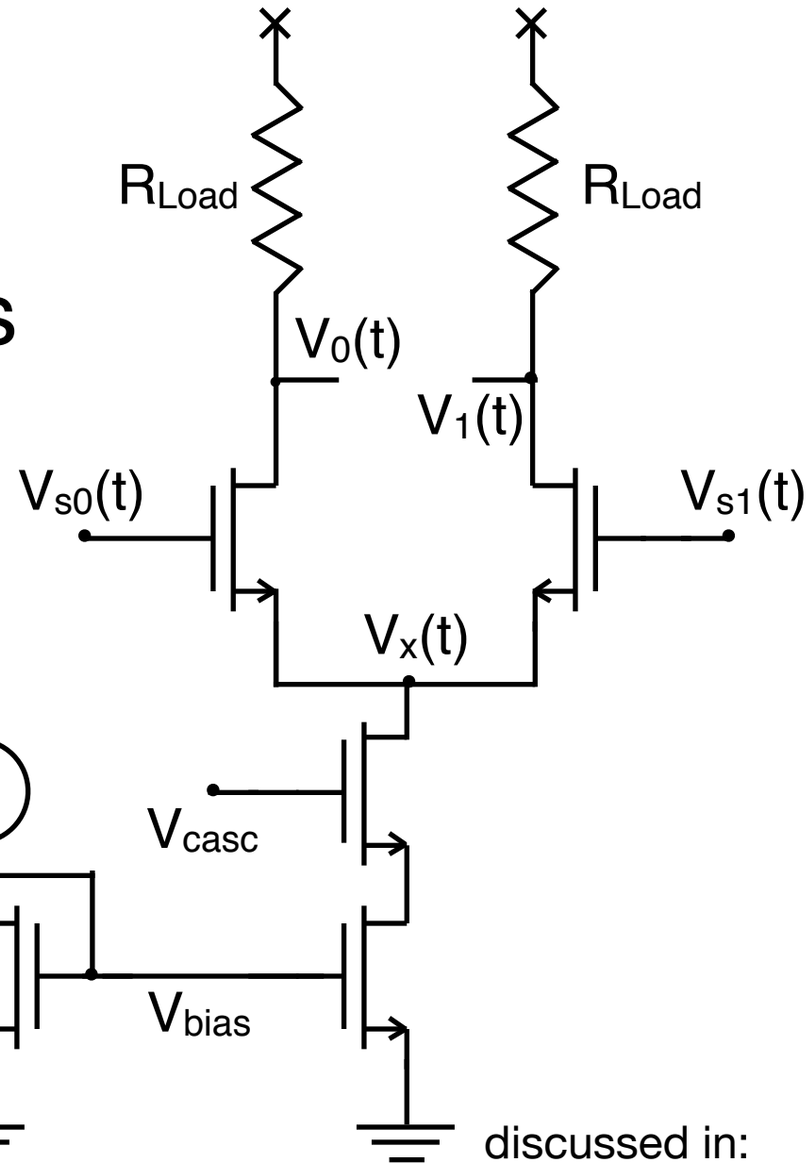
ferences:

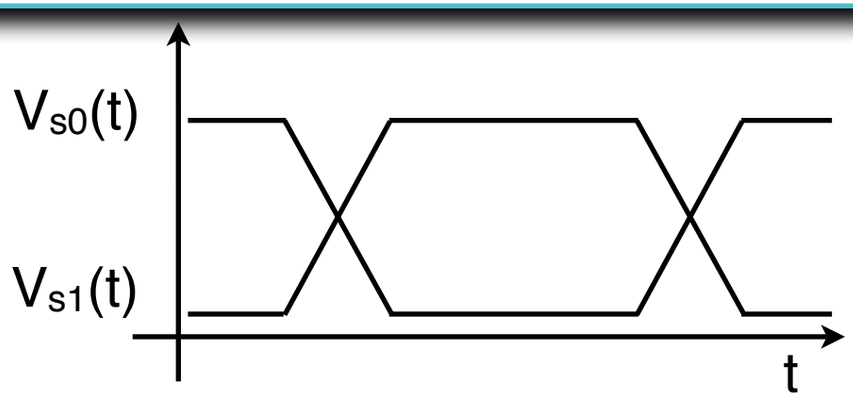
Practical Example:

- max. output voltage swing: 0.5 V
- $g_m r_0 \approx 10$
- max. source voltage (V_x) variation: ≈ 0.05 V
- rising speed of clock: 1.25 V/ns

⇒ resulting delay difference: 40 ps

ds





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Switching Delay Differences

- Output-Dependent Delay Differences:
  - Effects on the SFDR:

single-ended output:

$$\mathrm{SFDR} = \frac{4}{\omega_0 d_{\max}} \sqrt{\frac{1+4\omega_0^2\tau^2}{1+\omega_0^2\tau^2}}$$

$$\mathrm{SFDR} \approx \frac{4}{\omega_0 d_{\max}}$$

SFDR decreases with:
- increasing d_{max}
- increasing signal frequency ω_0

differential output:

$$\mathrm{SFDR} = \frac{32\tau}{\omega_0 d_{\max}^2} \sqrt{\frac{1+9\omega_0^2\tau^2}{1+\omega_0^2\tau^2}}$$

$$\mathrm{SFDR} \approx \frac{32\tau}{\omega_0 d_{\max}^2}$$

SFDR decreases with:
- increasing d_{max}
- increasing signal frequency ω_0
- decreasing time constant τ

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Switching Delay Differences

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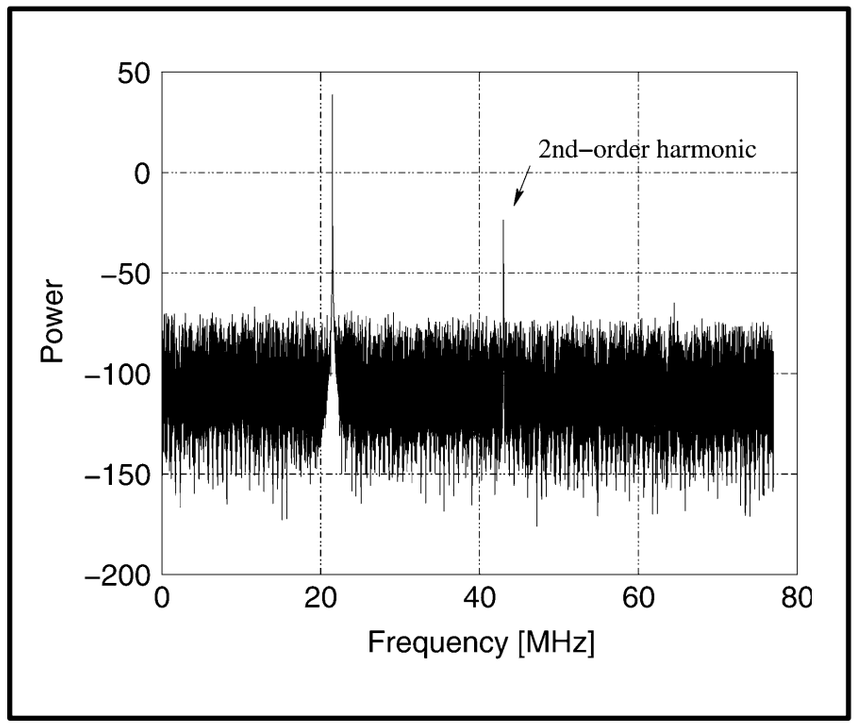
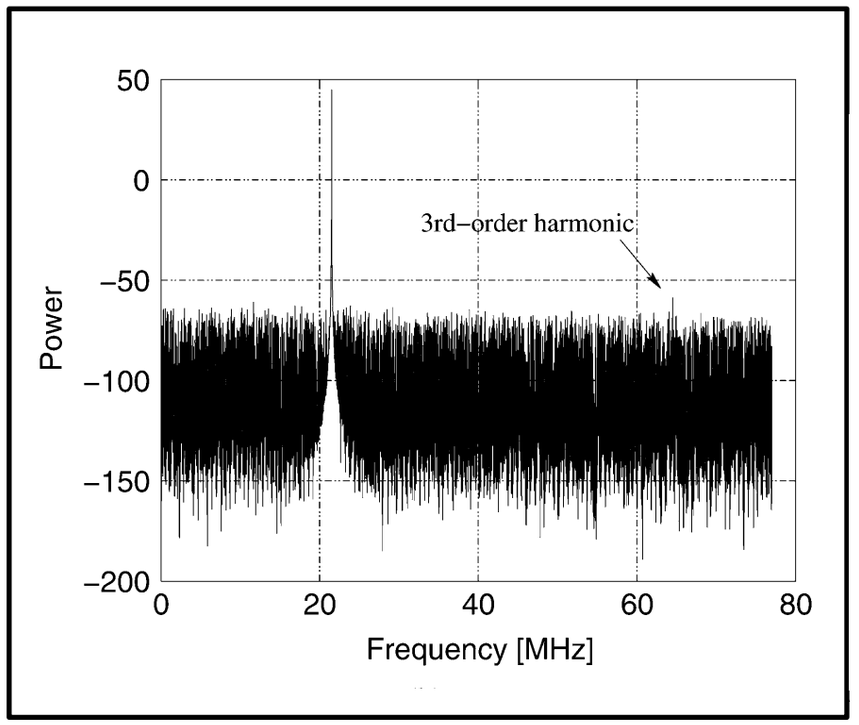
  - Effects on the SFDR:

single-ended output:



differential output:



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Switching Delay Differences

- Output-Dependent Delay Differences:
  - Measures against it:
    - increase ($g_m \cdot r_0$) of switches
      - add a cascode stage for switch (if voltage headroom permits)
      - scale the switches to increase $g_m \cdot r_0$
    - accelerate switching speed
    - add an RZ stage

discussed in:
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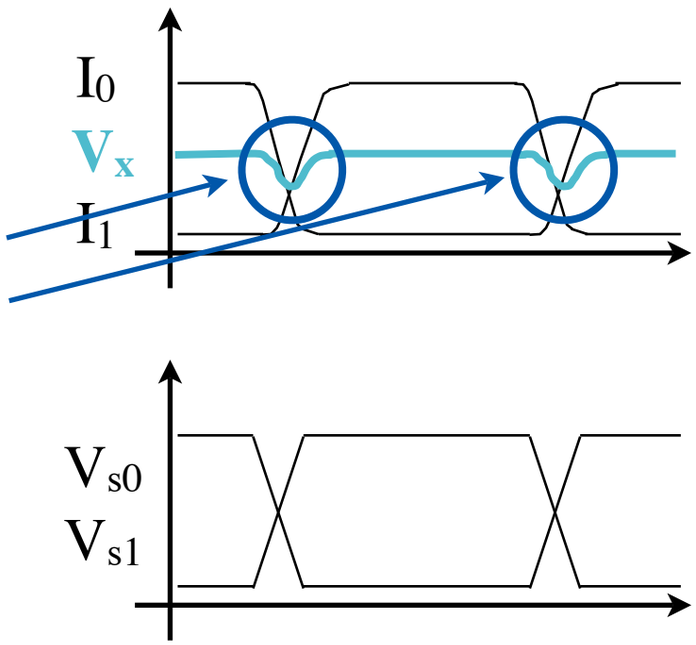
Switching Current Sources

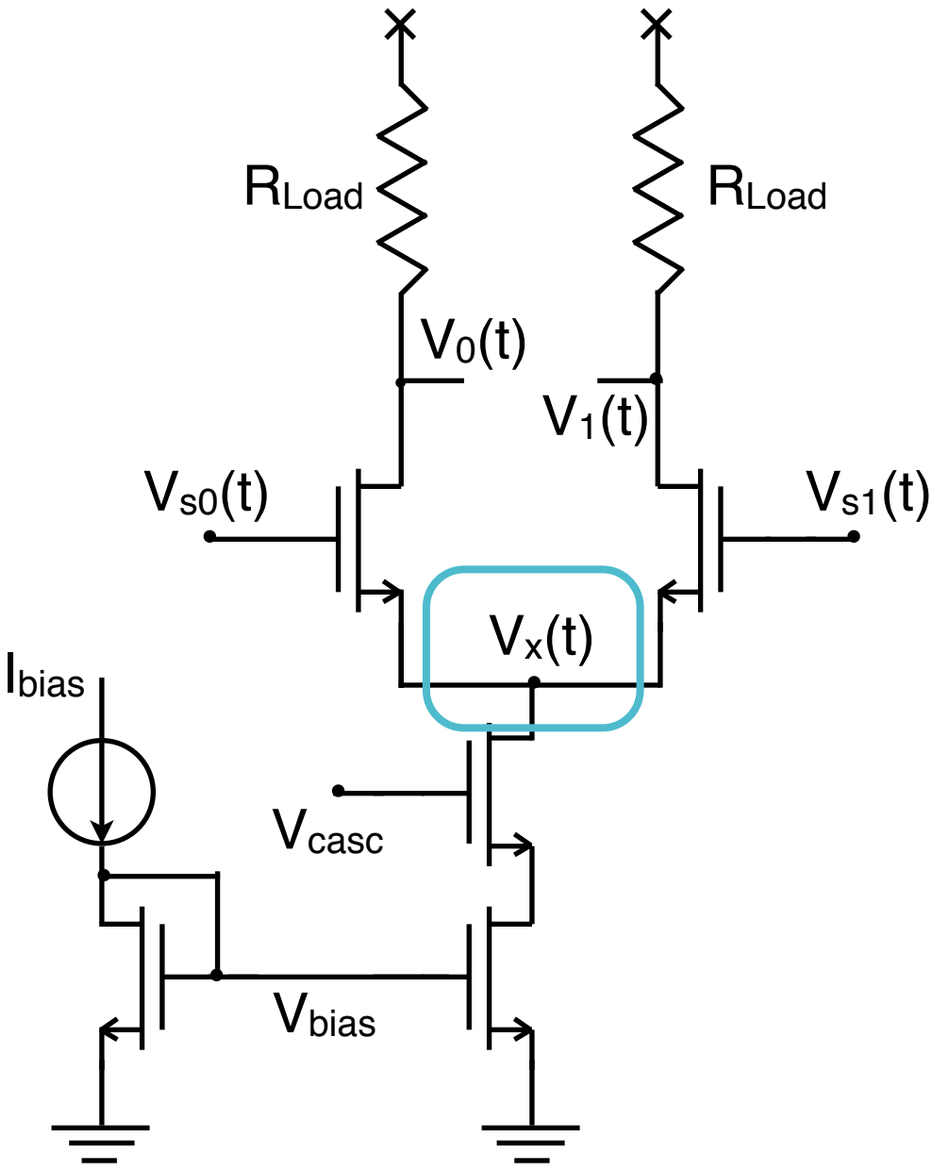
- Errors introduced while Switching:
  - "turning on"-transistor reaches different regions of operation at different times than its complementary "turning off" transistor.

short time where both differential current-switches are off

➡ abrupt discharge with steep transient

➡ voltage V_x drops





Switching Current Sources

- Charge feed-through:
  - common problem for all SC- and SI-circuits
  - first order proportional to
    - switch-capacitance (switch-size)
    - switch-driving signal slope
    - switch-driving signal swing
  - ideal switching scheme (for min. feed-through):
    - small switch
    - slow switch-driving signal
    - small switch-driving signal swing

Switching Current Sources

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- How to improve switching behavior
  - ideal switching scheme:
  - for min. feed-through:
    - small switch
    - slow switch-driving signal
    - small switch-driving signal swing
  - for small output-dep. delay differences:
    - increase size of switches for large ($g_m \cdot r_0$)
  - for short crossover time:
    - fast switching to minimize switching time

Switching Current Sources

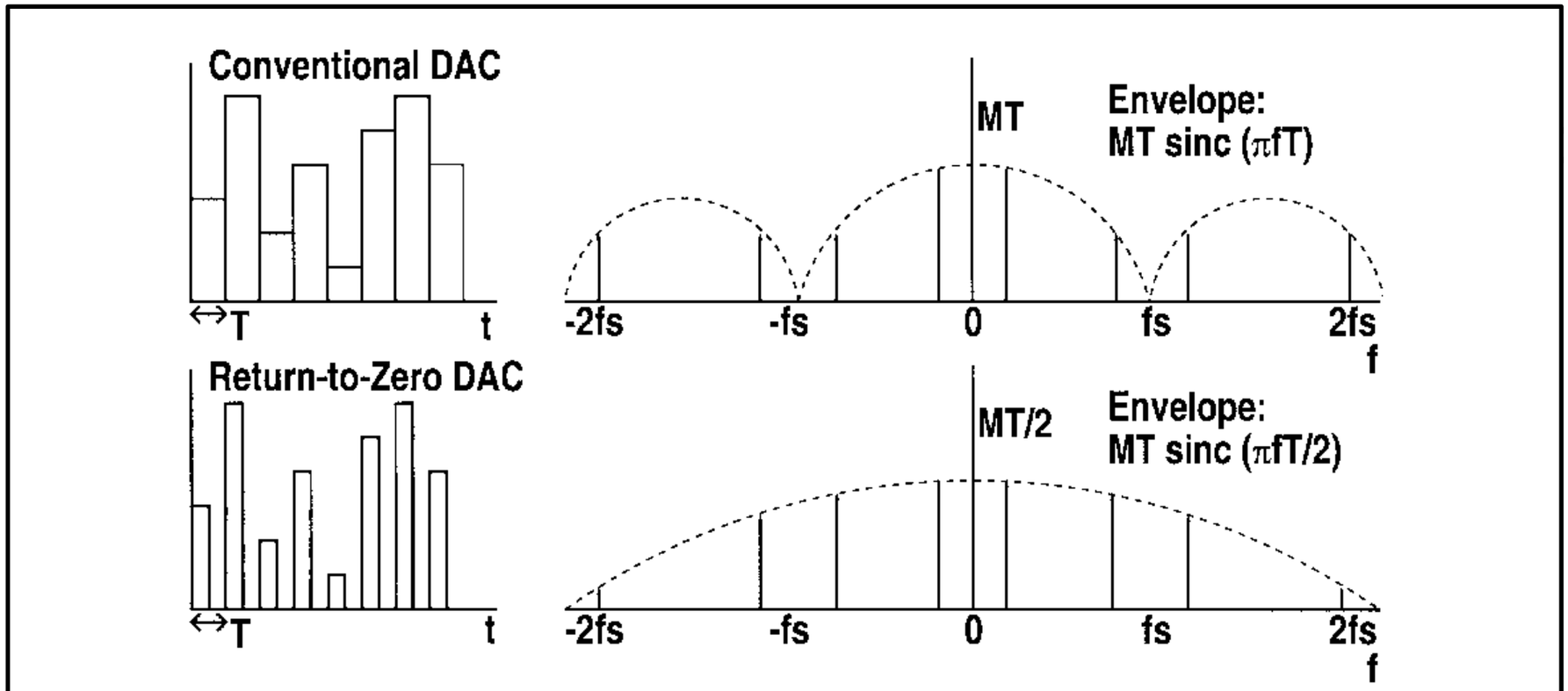
- How to improve switching behavior
  - ideal switching scheme:
  - for min. feed-thro
  -
  - f crossover time:
    - fast switching to minimize switching time

Switch Optimization:

- find ideal trade-off for switch-size (use cascode if head-room permits)
- slow switching signal, but with small signal-swing

NRZ vs. RZ, dual RZ

- NRZ vs. RZ, dual RZ:
  - RZ, return-to-zero circuit:
    - each pulse returns to zero for a portion of the clock period



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    - solves inter-symbol interference problem
    - halves the output signal power, extra circuitry power
    - reduces SFDR for low frequency input signals

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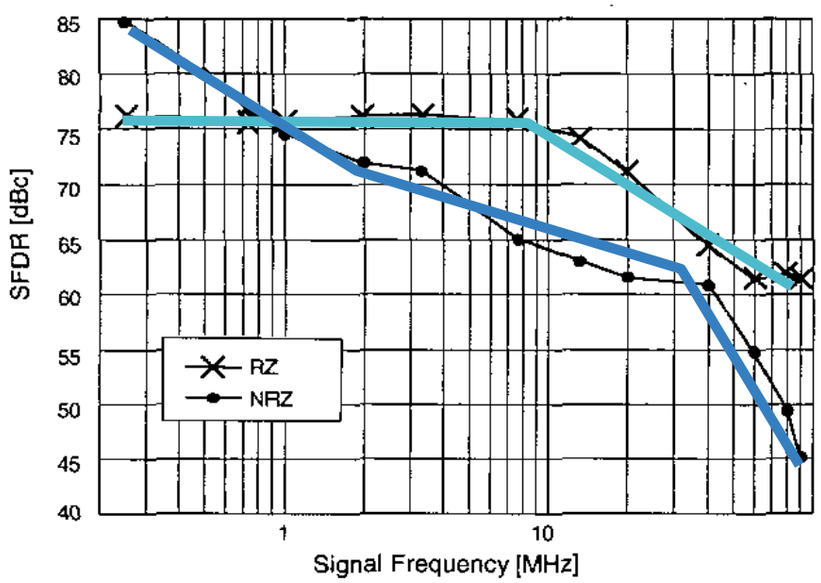

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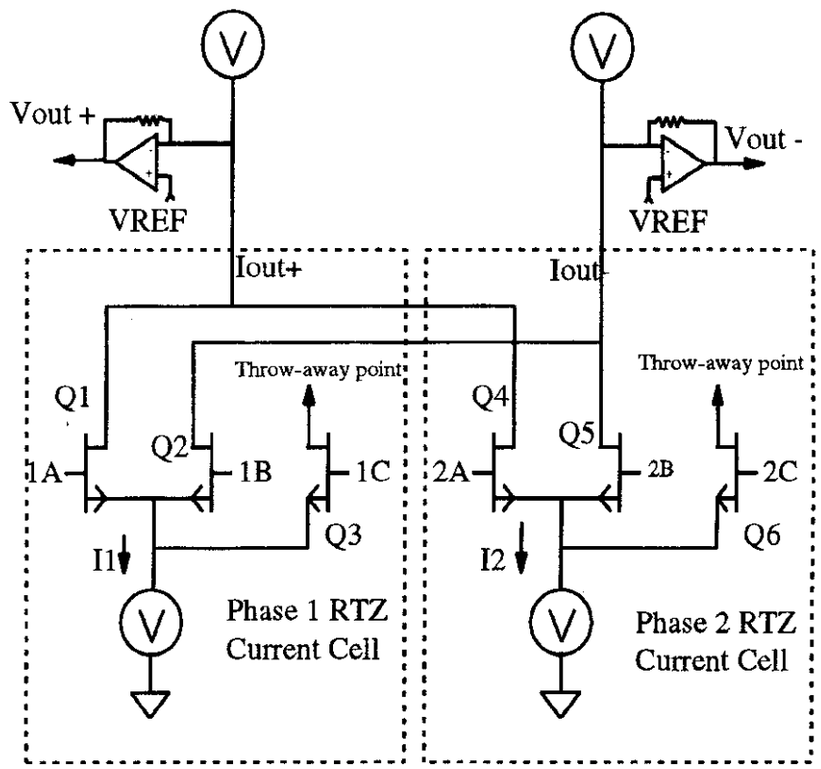

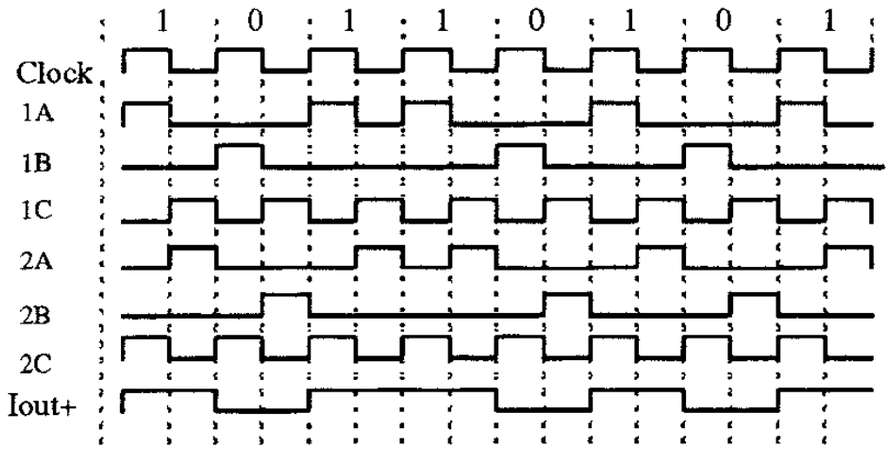

from:
R. Adams, et al., "*A 113 dB SNR oversampling DAC with segmented noise-shaped scrambling*", ISSCC 1998.

NRZ vs. RZ, dual RZ

- Dual RZ:
  - RZ, return-to-zero circuit:
    - combines two shifted RZ-pulses to a single pulse
    - solves inter-symbol interference problem
    - large circuit overhead

Part II: Modeling of DACs

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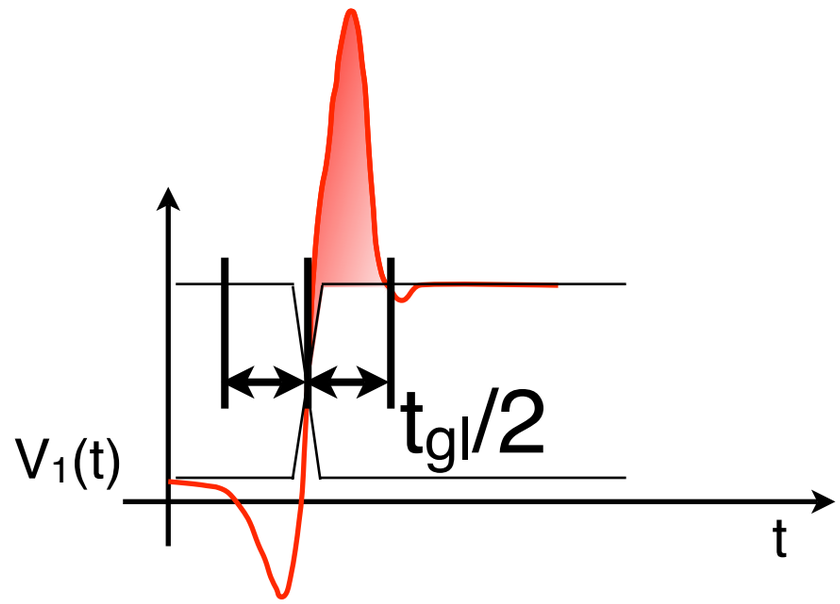
- Simple Mathematical Model of a Current-Steering DAC's Output
  - Code-Transition
  - Output-Dependent Delay Difference
  - The Simulink Model

- Future Work
  - Check whether the Model is precise enough
  - Build a Feedback Loop to Correct Non-Idealities

Preliminaries: Two Definitions

- Glitch “Energy”, E_{gl}:
  - sometimes called “Glitch Area”
  - not an energy, but voltage integrated over time
  - Unit: often $[pV \cdot s]$
  - many different definitions “my” definition:

- Glitch Time, t_{gl}:
  - “time during which the glitch occurs”



Simple Mathematical Model of a CS-DAC

- Current-Source Switching:
  - Code-Transition modeled by
    - shifted “tanh”-function
      +
    - exponentially-damped sinusoid as glitch

$$i_{\text{out}} = A_{\text{gl}} \sin\left(\frac{2\pi}{t_{\text{gl}}}(t-t_0)\right)\exp\left(-\text{sign}(t-t_0)\frac{2\pi}{t_{\text{gl}}}(t-t_0)\right) + \frac{\text{level}_{i+1}-\text{level}_i}{2}\tanh\left(\frac{2\pi}{t_{\text{gl}}}(t-t_0)\right) + \frac{\text{level}_{i+1}+\text{level}_i}{2}$$

discussed in:
J. Vandenbussche et al.,
“*Systematic Design of High-Accuracy Current-Steering D/A Converter Macrocells for Integrated VLSI Systems*”, TCAS-II, March 2001.

Simple Mathematical Model of a CS-DAC

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$$\frac{E_{\text{gl}}}{2R_{\text{load}}}nr_{\text{switched}} = A_{\text{gl}}\sin\left(\frac{2\pi}{5}\right)\exp\left(-\frac{2\pi}{5}\right) + \frac{1}{2}\frac{\text{level}_{i+1}-\text{level}_i}{2}\left(\tanh\left(\frac{2\pi}{5}\right)-1\right)\frac{t_{\text{gl}}}{4}$$

  - Parameters:
    - Glitch Energy, E_{gl} → Glitch Amplitude A_{gl}
    - Glitch Time, t_{gl}
    - number of switches (involved in the code-transition)

discussed in:
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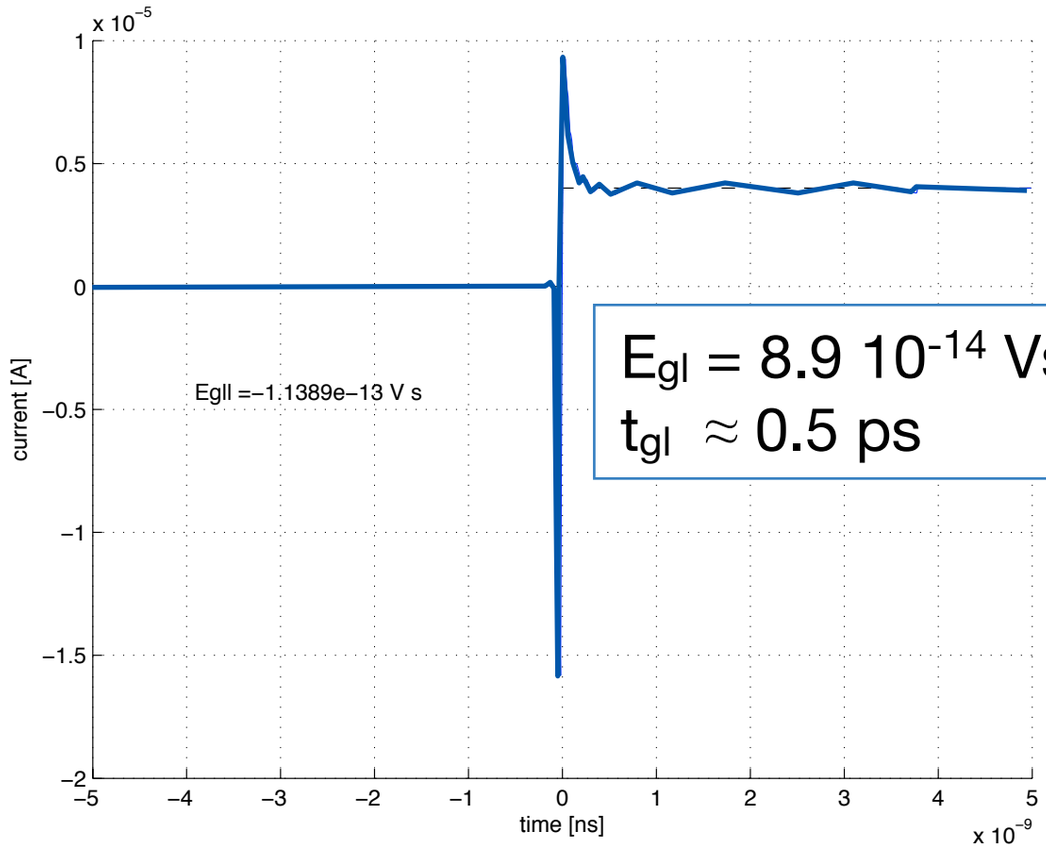
Simple Mathematical Model of a CS-DAC

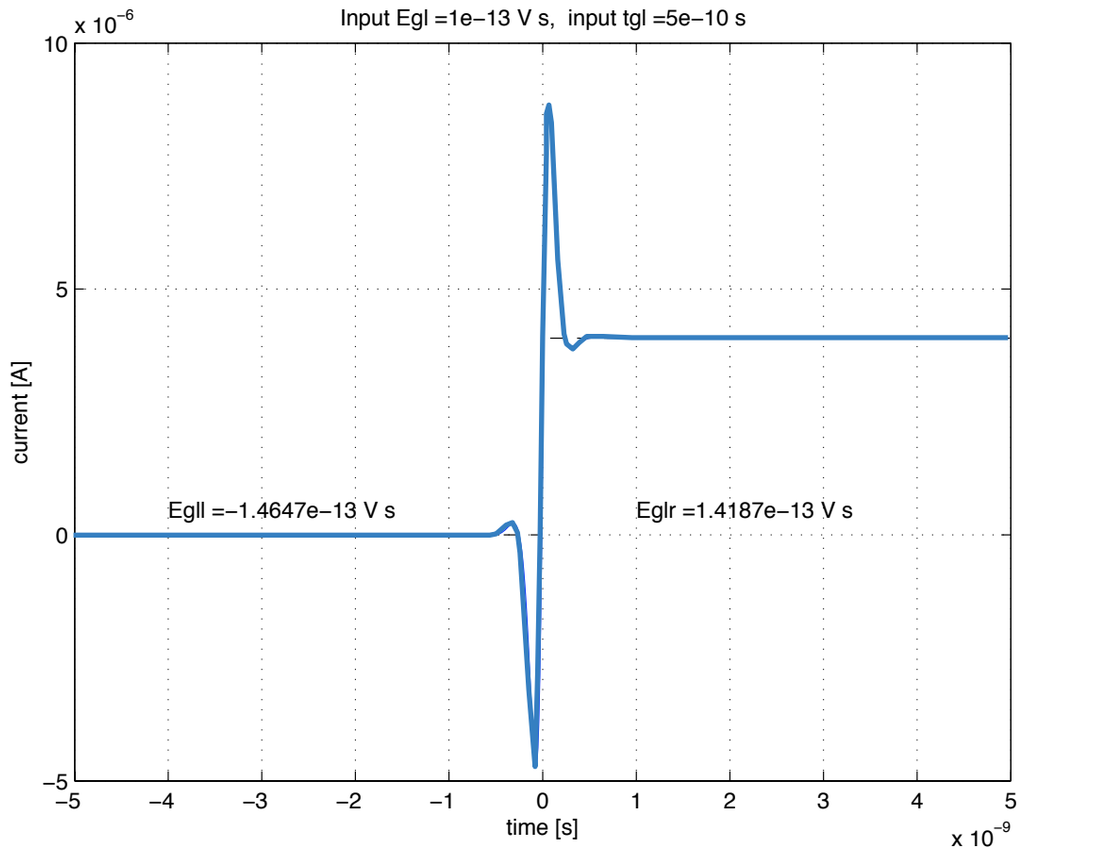
- From Transistor-Level to High-Level

1) Transistor-Level Simulation in Cadence:



$E_{gl} = 8.9\ 10^{-14}$ Vs
$t_{gl} \approx 0.5$ ps

3) High-Level Simulation with Extracted Parameters:



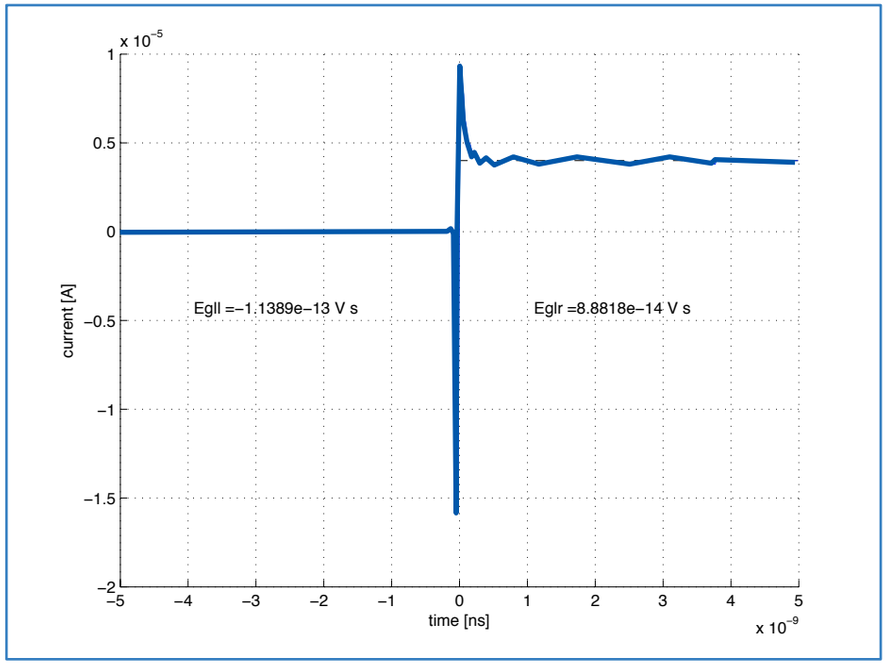
2) Extract Parameters E_{gl}, t_{gl}

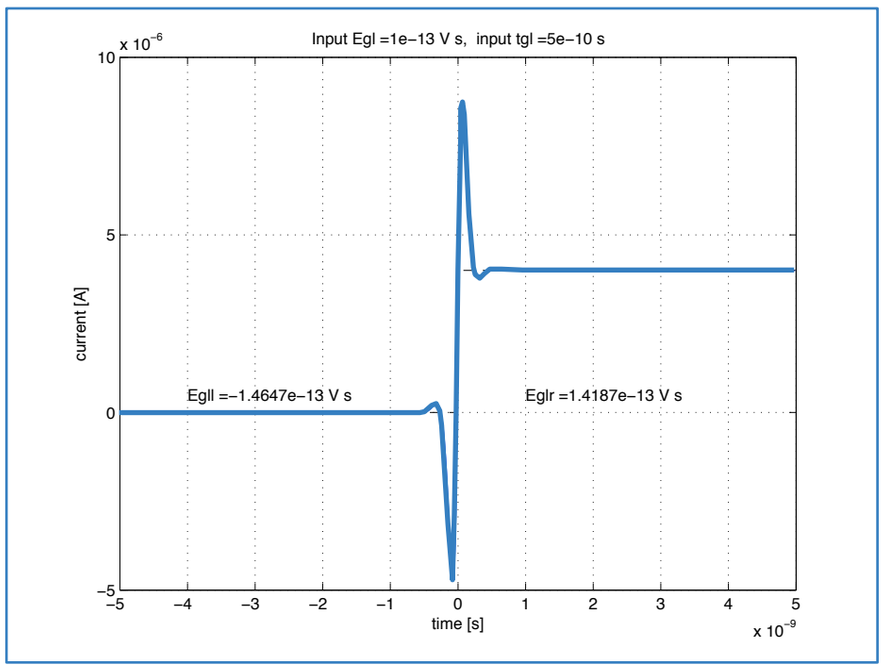
Simple Mathematical Model of a CS-DAC

- From Transistor-Level to High-Level
- Is the model precise enough?

  – Glitches are more symmetric in the mathematical model than in Cadence

  – With the same glitch-time, t_{gl}, the high-level simulation has a smaller bandwidth.





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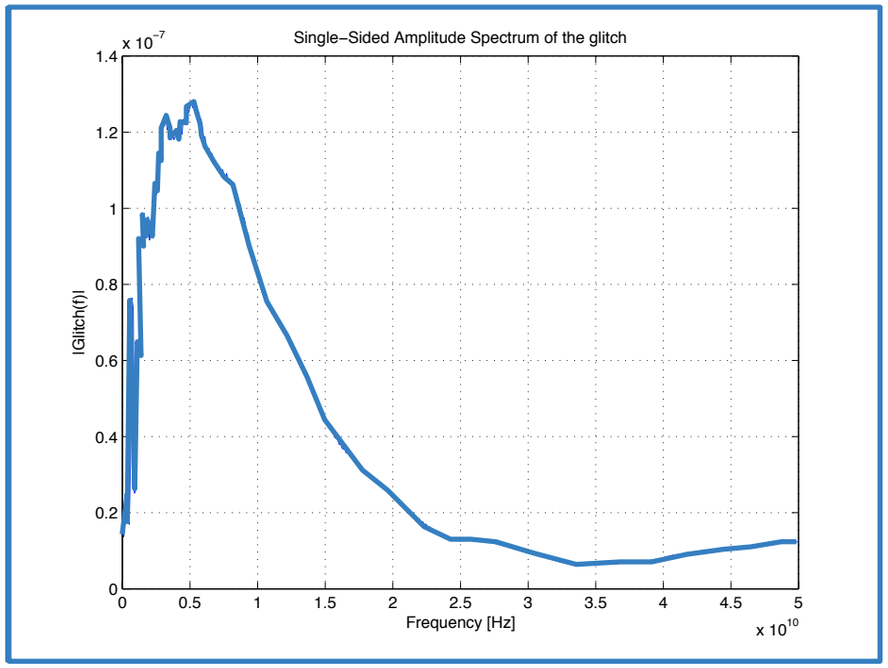
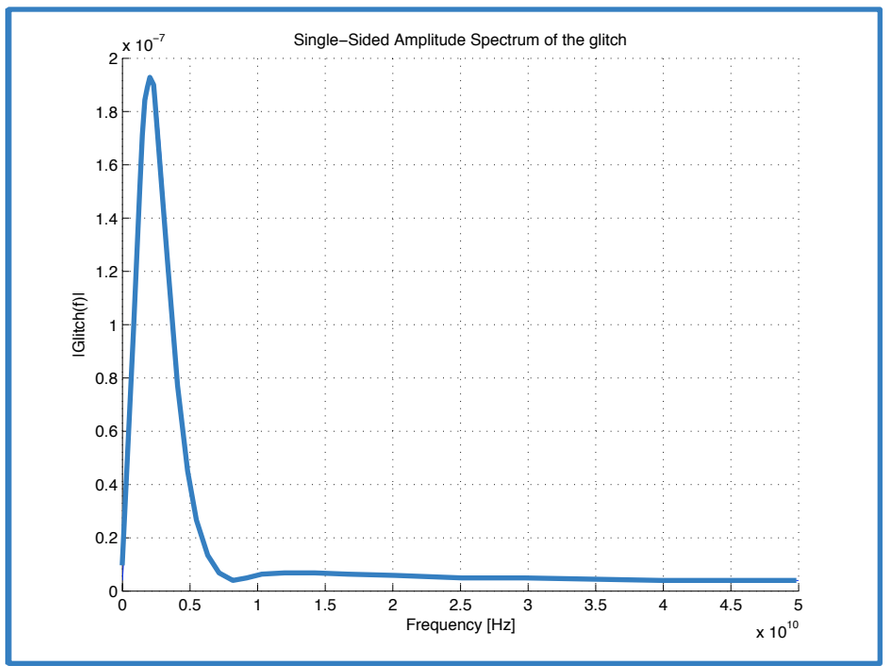
  - With the same glitch-time, t_{gl}, the high-level simulation has a smaller bandwidth.



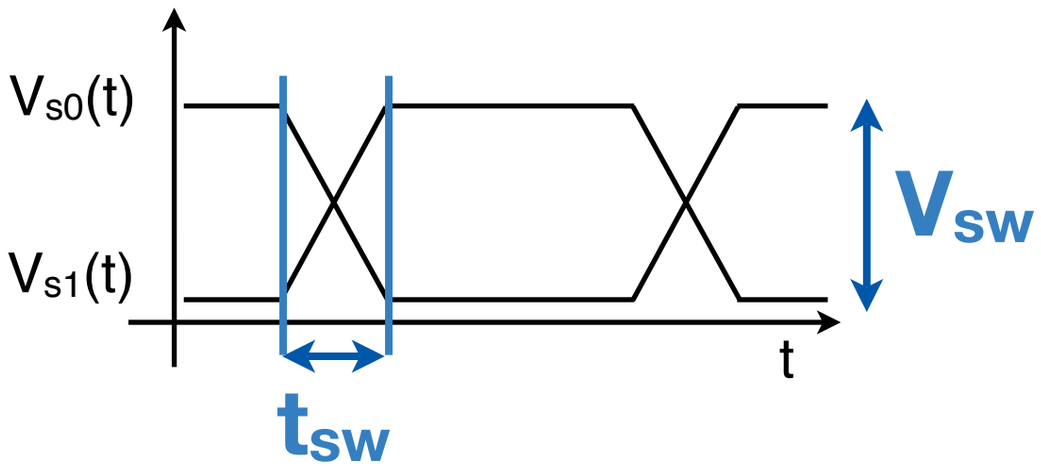


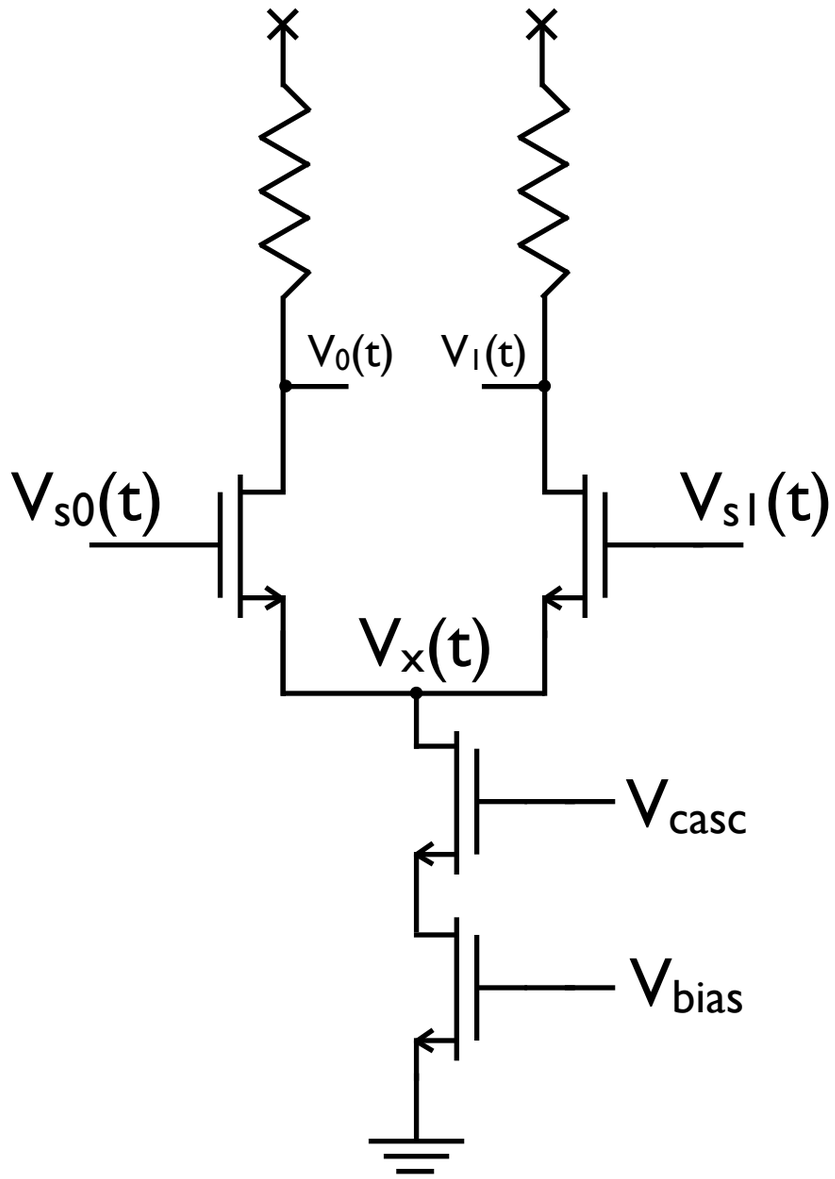
Simple Mathematical Model of a CS-DAC

- Output-Dependent Delay Difference

$$V_{\mathrm{x}}(t) = \frac{V_0(t)}{1 + g_m r_0}$$

$$t_{\mathrm{delay}} = \frac{t_{sw}}{V_{sw}(V_{\mathrm{th}} + V_{\mathrm{x}}(t))}$$

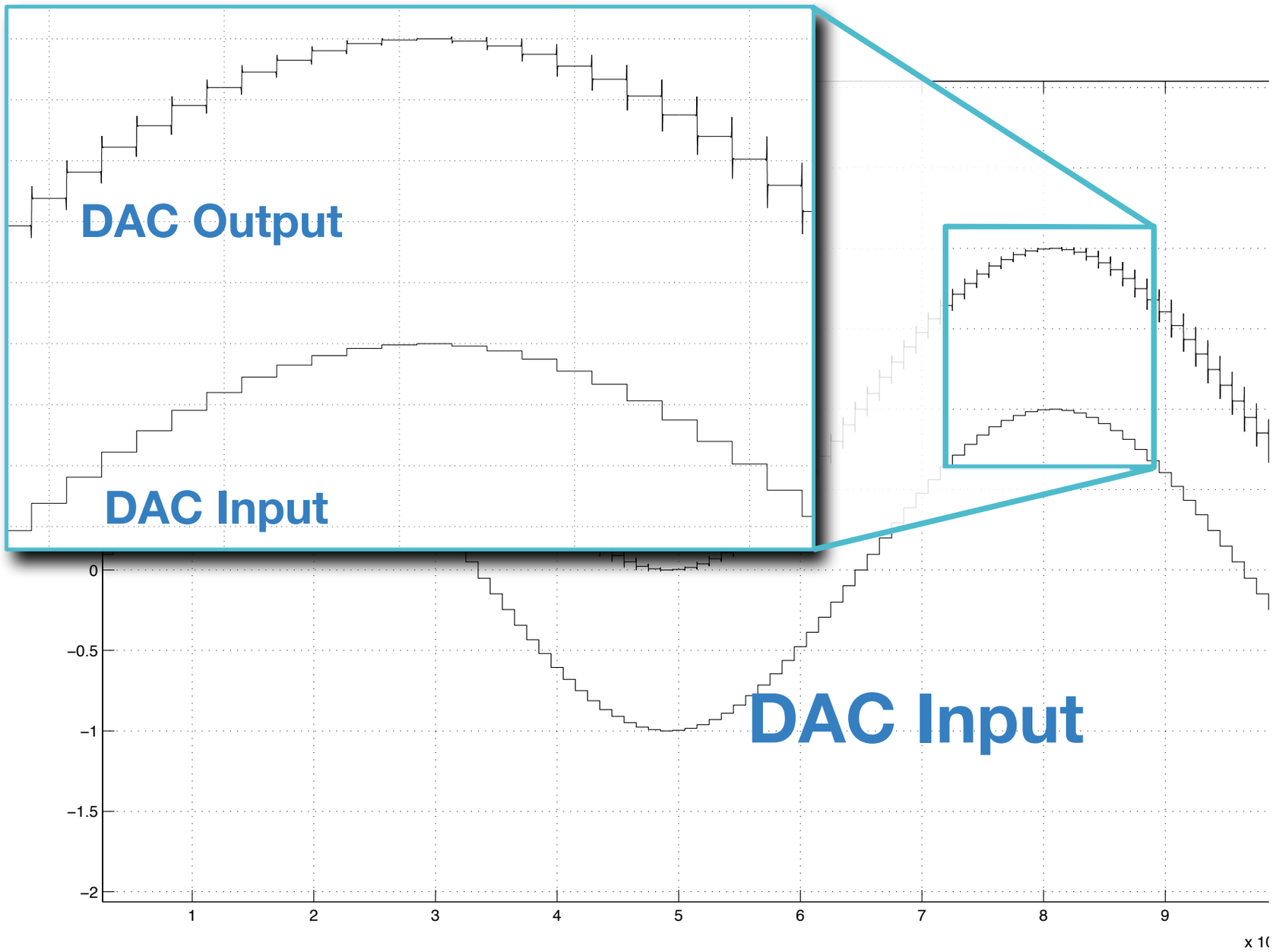




$$t_{\mathrm{delay}} = \frac{t_{sw}}{V_{sw}\left(V_{\mathrm{th}} + \frac{V_0(t)}{1+g_m r_0}\right)}$$

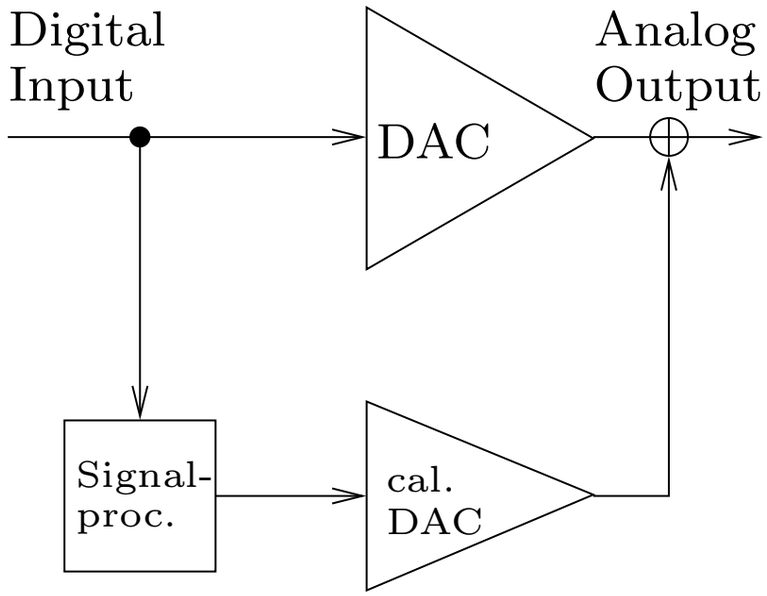
Simulink Model of a CS-DAC

- Output of the Simulink Model:

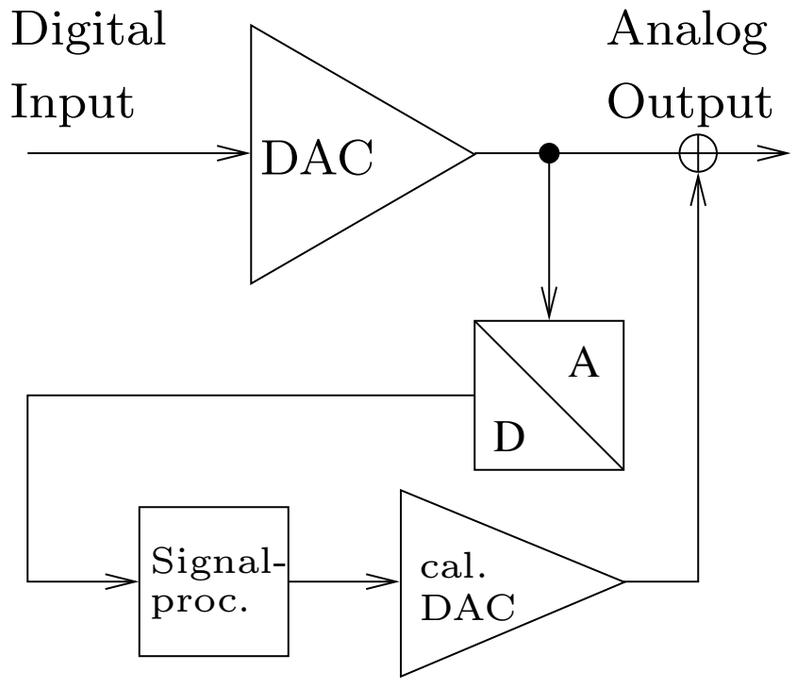


Future Work

- Check if Model's Precision is enough
- Design Feedback Loop to Correct Non-Idealities of DAC-Settling



(a) Feedforward with a seperate calibration DAC.



(b) Feedback with a separate calibration DAC.

Conclusions

- The settling behavior of a current-steering DAC was discussed.
- Various reasons for SFDR degradation in current-steering DACs was presented.
- Hints for the design of the switches in current-steering DACs were given.

- A simple mathematical model of a current-steering DAC was presented.

Thank you!

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Thank you for your interest!

for questions & comments:
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