カレントスティーリングDACの動的特性の調査

Recent studies on the dynamic behavior of current-steering DACs

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In recent years, the interest in high-speed and high-resolution current-steering digital-to-analog converters (DACs) has greatly increased. Even though many medium-resolution DACs (of around 8–10 bits) for higher sampling frequencies exist, most of these DACs show poor performance for input signal frequencies approaching the Nyquist frequency [1], as can, e.g., be seen in Fig. 1. Therefore, it seemse to be essential to study the dynamic behavior of DACs. It has been found that the cell-dependent delay differences [3], and the output-dependent delay differences [4] greatly limit the SFDR of high-speed DACs.

Our ongoing research focuses on building a high-level model of the DAC's dynamic behavior and subsequently designing a digital calibration circuit that dynamically adjusts the input to the DAC to compensate for non-ideal dynamics.

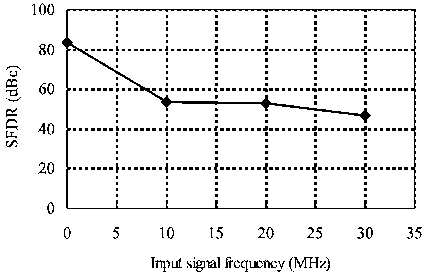

Fig. 1: SFDR versus input signal frequency, $f_{samp} = 100$ MHz (taken from [2]).

References:

[1] K. Doris, A. van Roermund, and D. Leenaerts, "*Wide-bandwidth high dynamic range D/A converters*", Springer, The Netherlands, 2006.

[2] Y. Ikeda, M. Frey, and A. Matsuzawa, "*A 14-bit 100-MS/s digitally calibrated binary-weighted current-steering CMOS DAC without calibration ADC*", to be published at ASSCC 2007, South Korea, 2007.

[3] T. Chen and G. Gielen, "*The analysis and improvement of a current-steering DAC's dynamic SFDR—I: The cell-dependent delay differences*", TCAS-I, vol. 53, no. 1, January 2006.

[4] T. Chen and G. Gielen, "*The analysis and improvement of a current-steering DAC's dynamic SFDR—II: The output-dependent delay differences*", TCAS-I, vol. 54, no. 2, February 2007.