The effects of Switch Resistances on Pipelined ADC Performances and the Optimization for the Settling Time.

Hiroki Endo, Masaya Miyahara, Akira Matsuzawa
Tokyo Institute of Technology, Japan

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Motivation

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- Switch resistance in submicron CMOS can't be neglected.
- The influence of the switch resistance on the settling time needs to be considered.

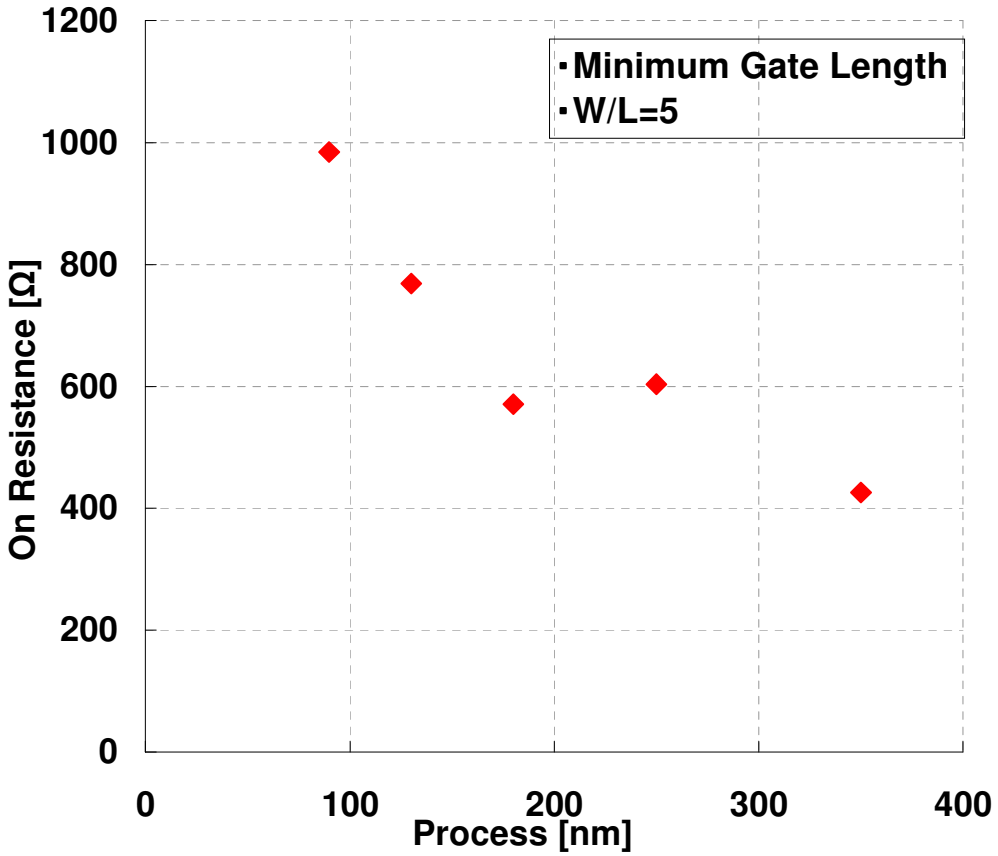

Fig.1 NMOS Switch Resistance

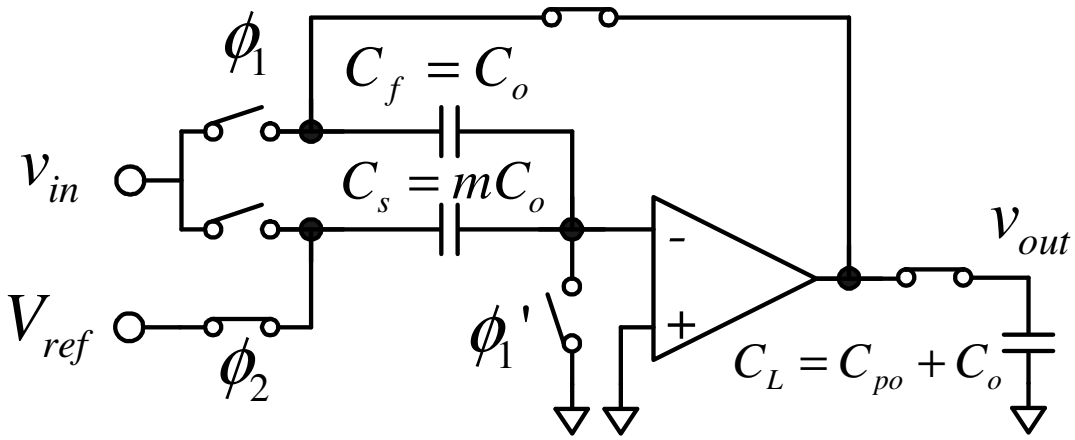

Fig.2 The MDAC configuration of pipelined ADC

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The Effects of Switch Optimization

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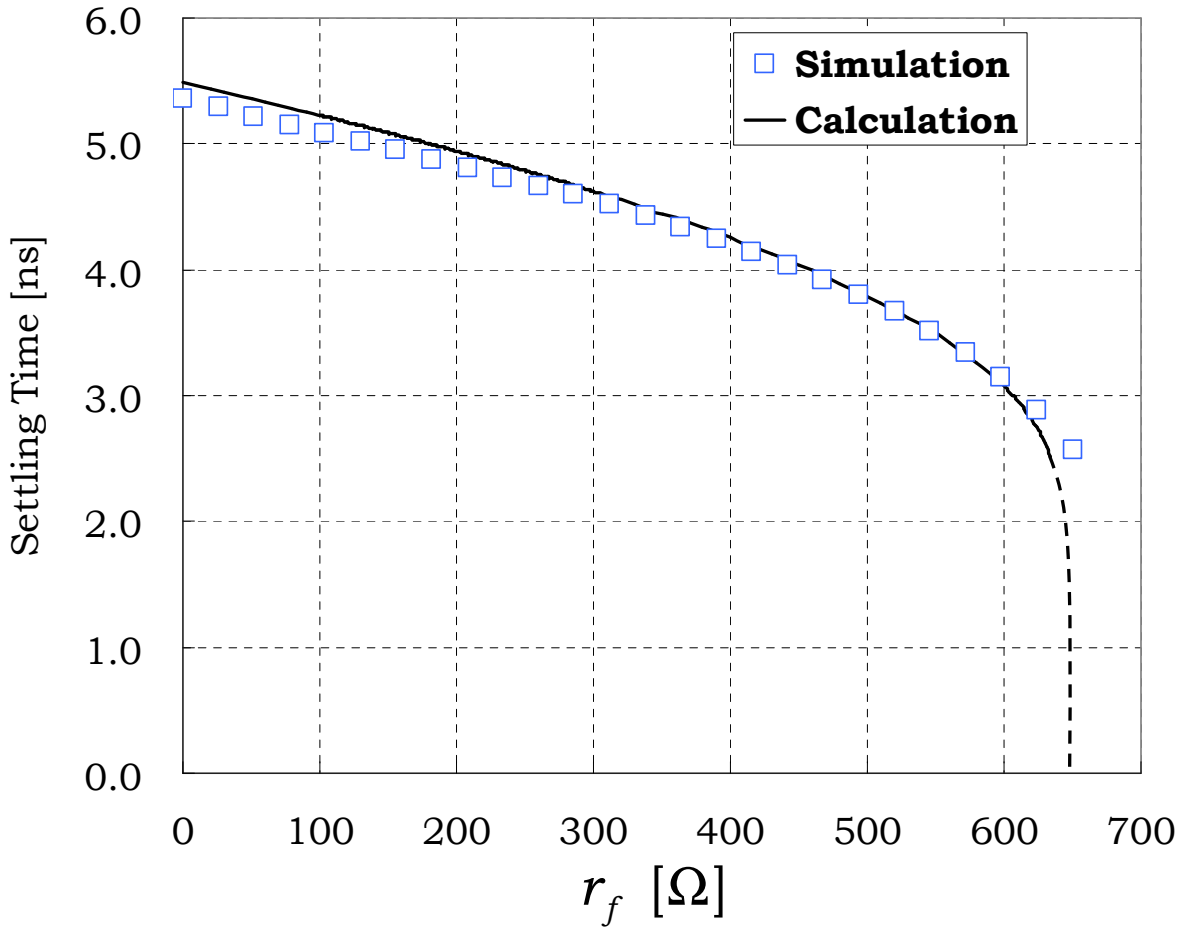
- This equation shows optimum feedback switch resistance.
- Using this equation, the settling time has been improved by 50%.

$$r_{f\_opt} = mr_s + \frac{(m+1)}{g_m}$$

r_{f_opt} : optimum feedback switch resistance
r_s : sampling switch resistance
g_m : transconductance of opamp
m : number of sampling capacitor



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