R1-15 The Effects of Switch Resistances on Pipelined ADC Performances and the Optimization for the Settling Time.

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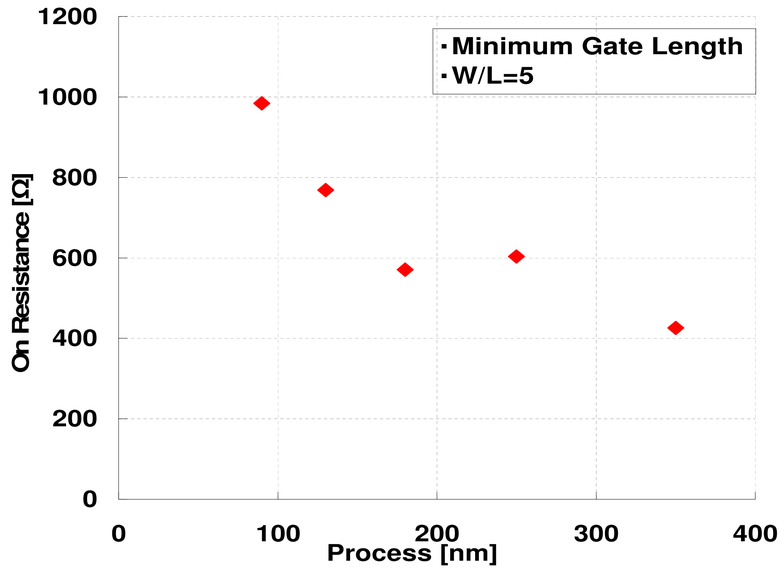
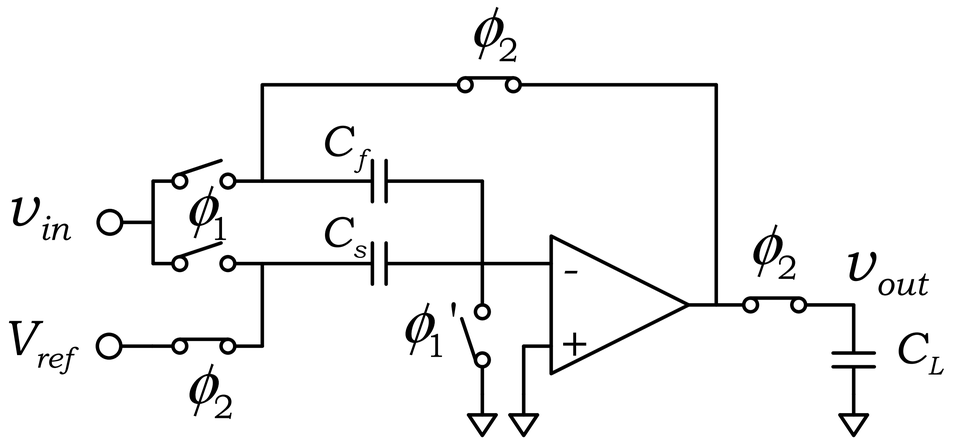
1. Background

Switch resistance can't be neglected to design switched capacitor circuit in sub-micron CMOS.

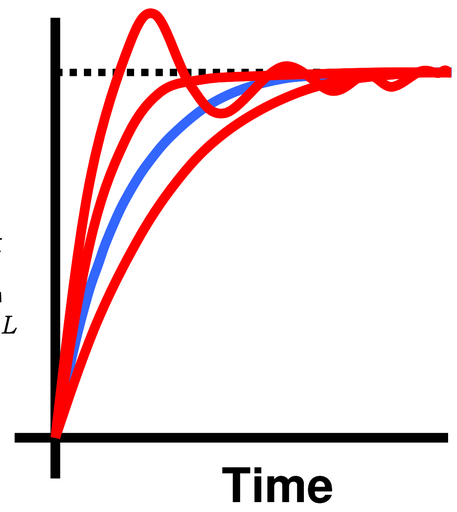


2. Purpose

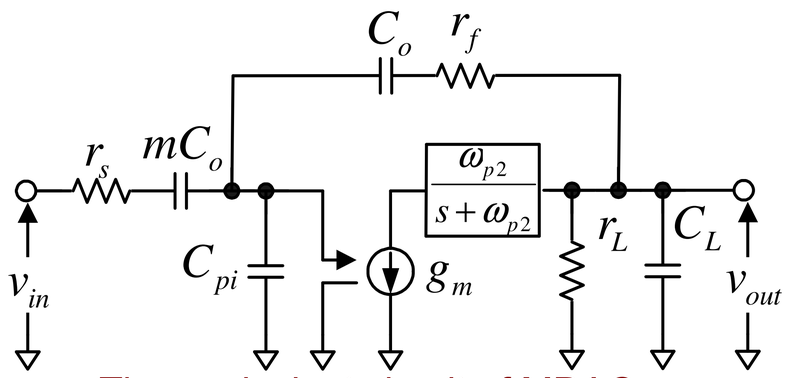
1. Explain the influence of the switch resistance on the settling time of MDAC.
2. Derive optimum condition of the switch resistance.
3. Consider optimum MDAC configuration.



Multiplying Digital to Analog Converter



3. Pole-Zero Cancellation



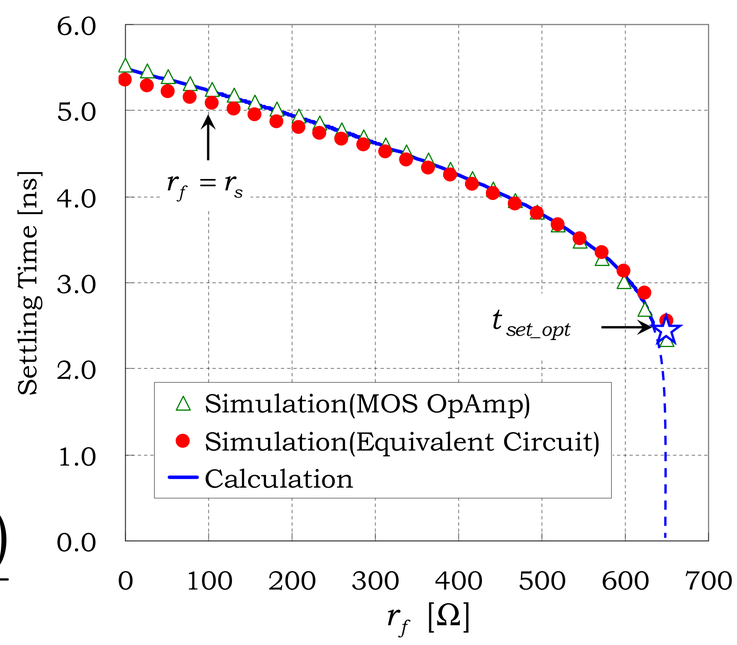
The equivalent circuit of MDAC

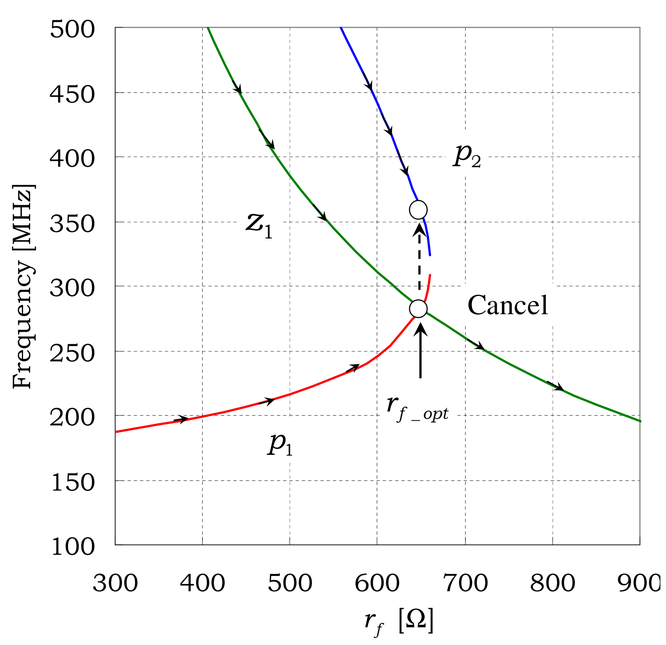
$$v_{out} = -mV_{in}\left[1-\frac{1}{2}(1+\gamma)e^{-(\alpha-\beta)t} - \frac{1}{2}(1-\gamma)e^{-(\alpha+\beta)t}\right]$$

reject this term

$$r_{f\_opt} = mr_s + \frac{(m+1)}{g_m}$$

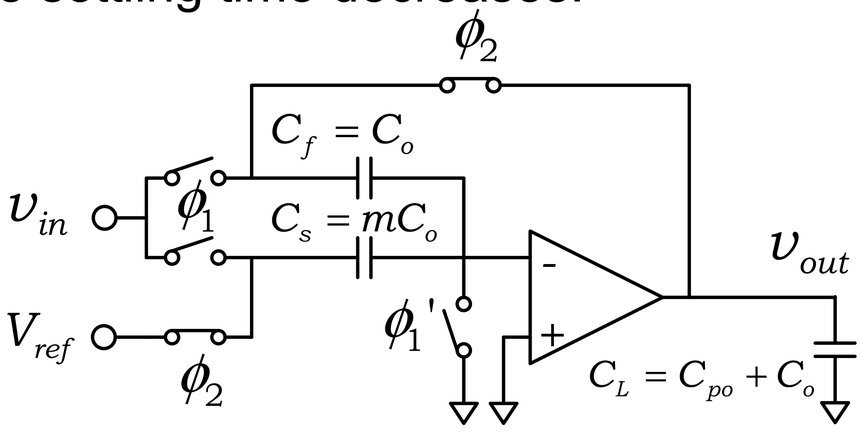
By using the switch resistance optimization, the settling time of the MDAC has been improved by 50%.

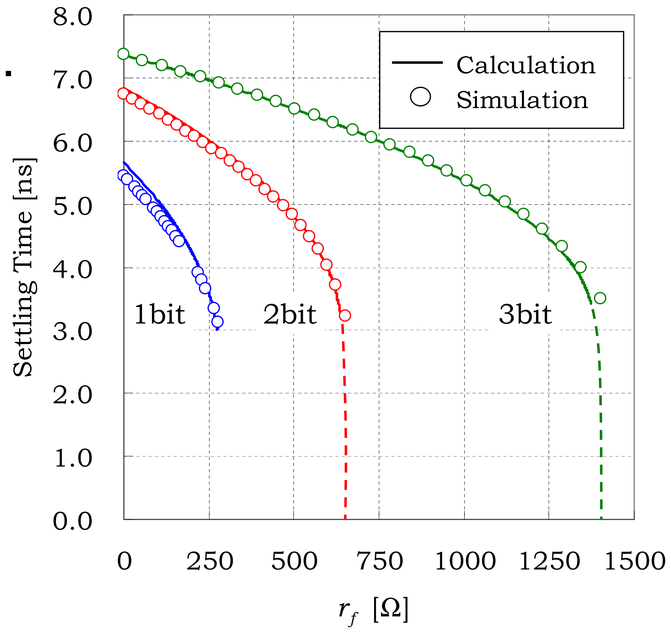


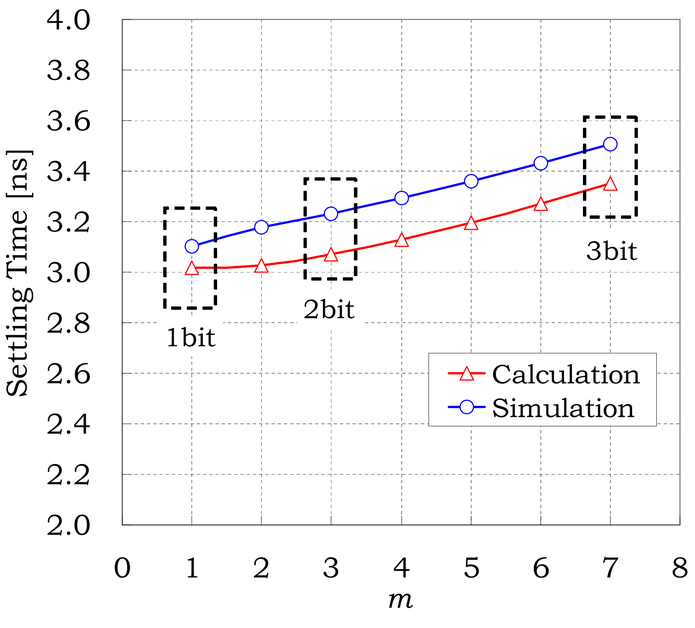


4. Multi-Bit Structure

The multi-bit structure might be able to make better use of the switch resistance optimization.
Because the sensitivity of switch resistance to the settling time decreases.







5. Summary

1. To optimize the MDAC in a pipelined ADC, the influence of the switch resistances on the settling time is investigated.
2. The settling time of the MDAC has been improved by 50% in the maximum by using pole-zero cancellation.