R1-14   ΣΔ-Modulator with High Nearby Interferers Suppression by Transmission Zeroes
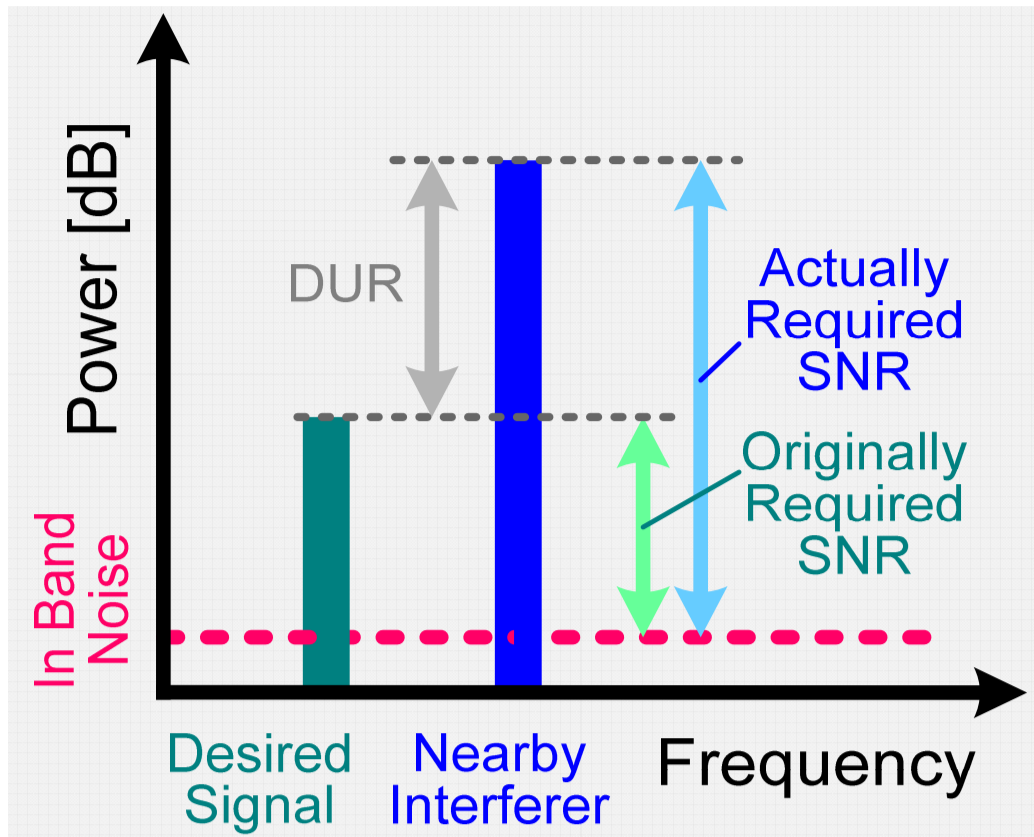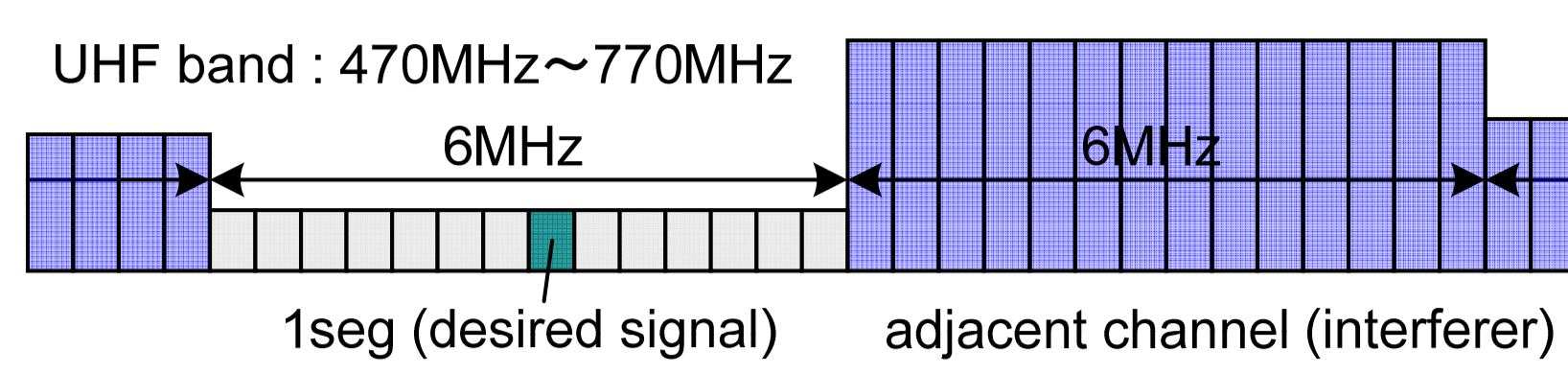
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1. Background

Higher resolution ADC is required because of large nearby interferer.


Simplified frequency chart of "1seg" TV signal

UHF band : 470MHz〜770MHz
6MHz   6MHz

1seg (desired signal)   adjacent channel (interferer)

① ADC → Digital Filter → DSP   High resolution is required for ADC.

② Filter → ADC → DSP   Power consumption of the prefilter is large.

③ Filtering ADC → DSP   This work

2. Filtering STF of normal Sigma-Delta Modulators
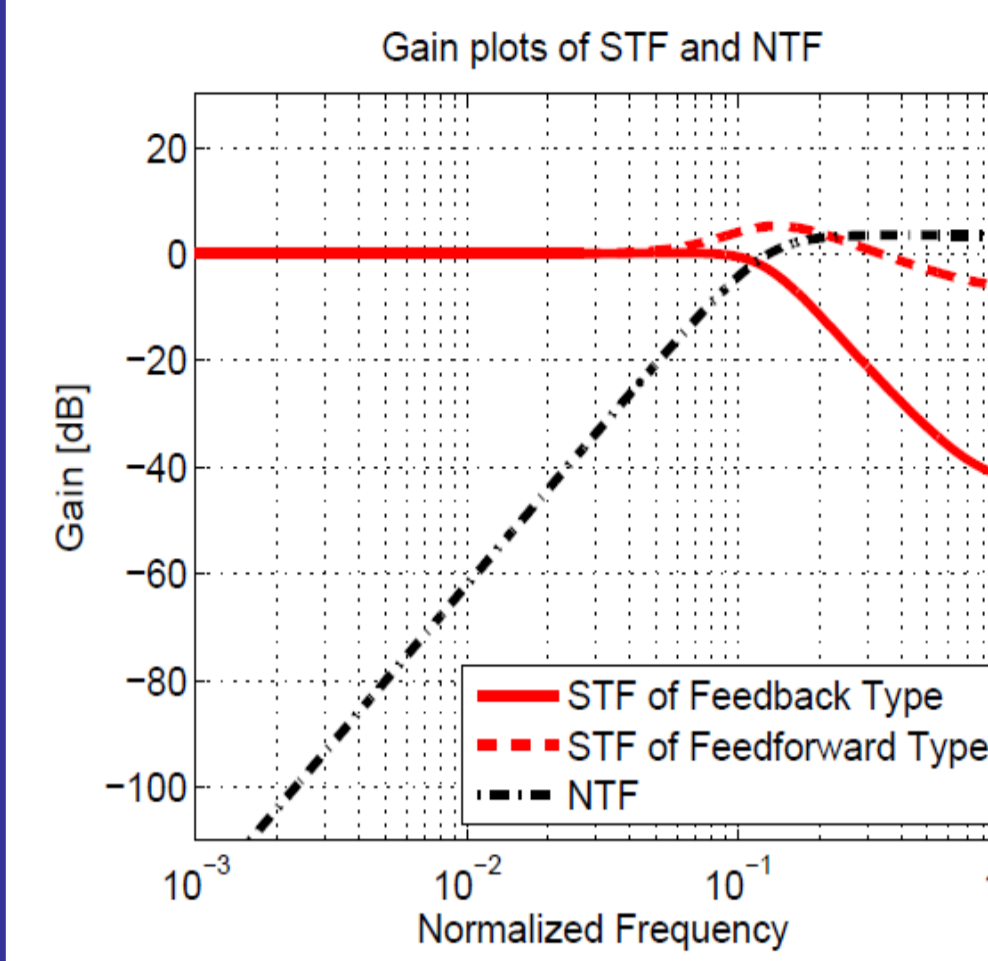
Signal Transfer Functions of normal ΣΔ-Modulators are originally low-pass filter.

However, sufficient nearby interferer suppression can not be achieved because of their wide pass-band.

Gain plots of STF and NTF
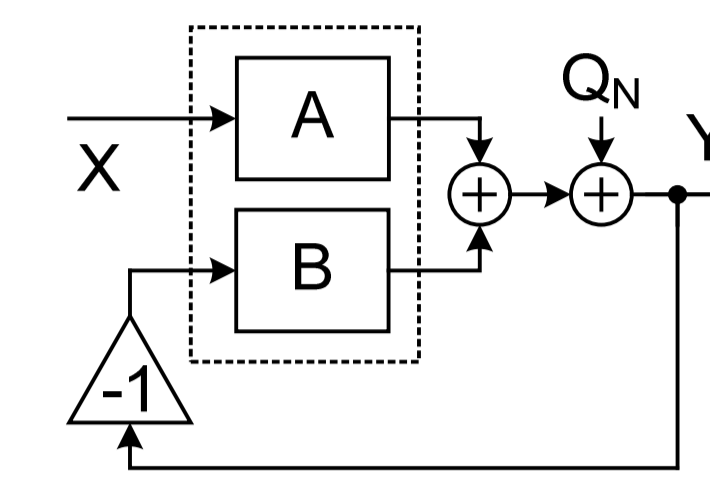
$$A = \frac{A_{num}}{A_{den}}, \quad B = \frac{B_{num}}{B_{den}}$$

$$Y = \underbrace{\frac{A_{num} \cdot B_{den}}{A_{den} \cdot B_{den} + B_{num}}}_{STF} X + \underbrace{\frac{B_{den}}{B_{den} + B_{num}}}_{NTF} Q_N$$

3. Filter Design for Notched STF

Proposed STF improvement method introduces transmission zeroes to form notched STF.

It can be realized by direct feedforward paths from the input to each integrator and quantizer.


Gain plots of STF and NTF

Poles and Zeros of STF and NTF

× NTF Poles
○ NTF Zeros
+ STF Poles
□ STF Zeros
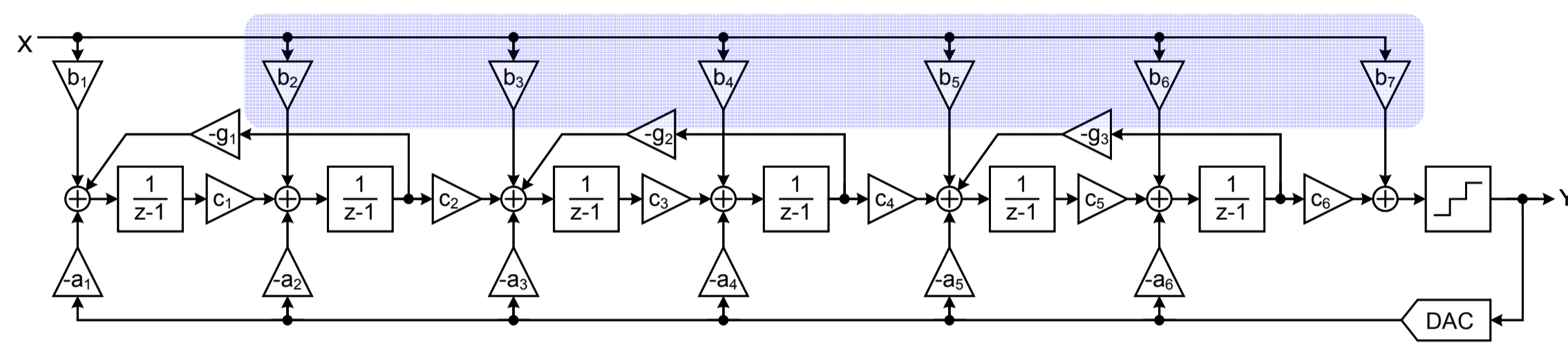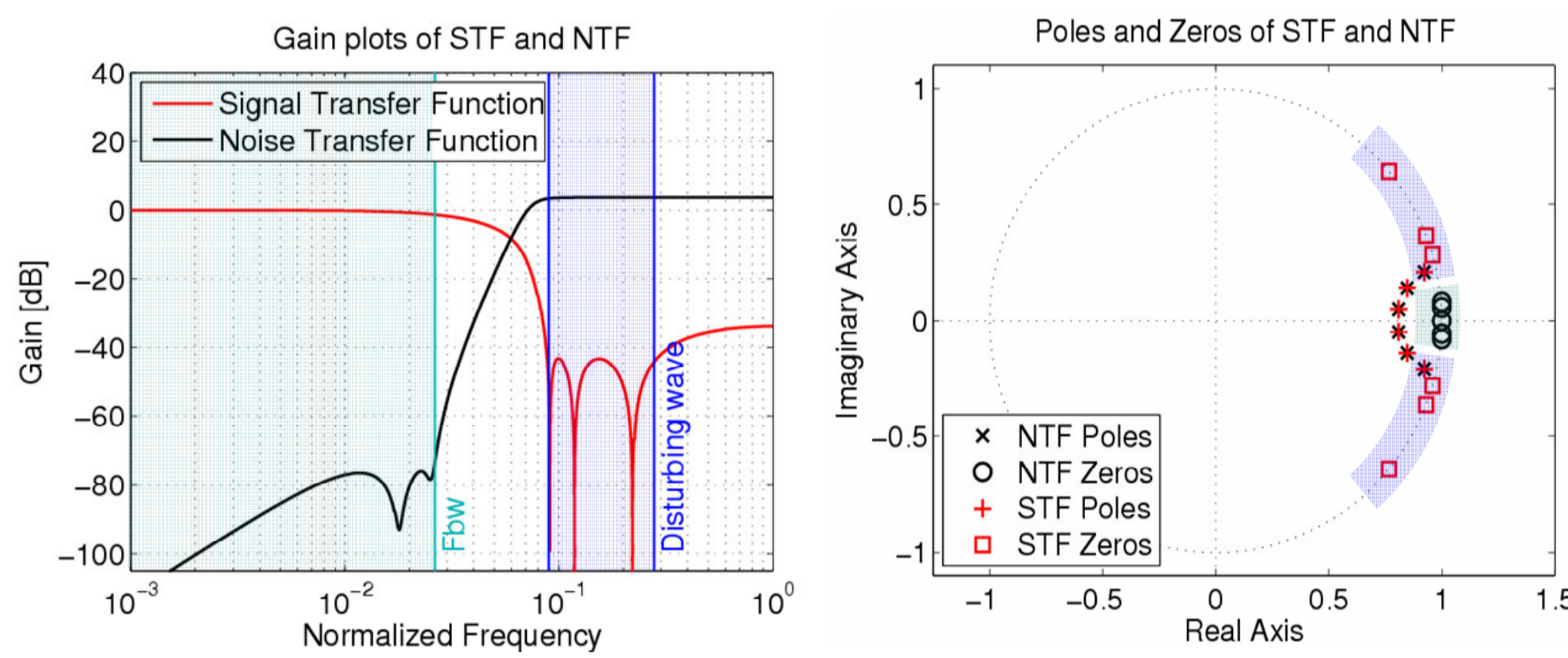
4. Circuit Design

The kT/C noise of the switched capacitor summing integrator (after the multiplication with coefficients)

$$\left\{ \sum_i \left(\sqrt{\frac{kT}{C_{si}}} \times C_{si} \right) \right\} / C_f = \sqrt{\frac{kT \cdot \sum_i C_{si}}{C_f^2}}.$$

kT/C noise and power consumption are minimized by maximally sharing the sampling capacitors between feedback paths and the other paths.
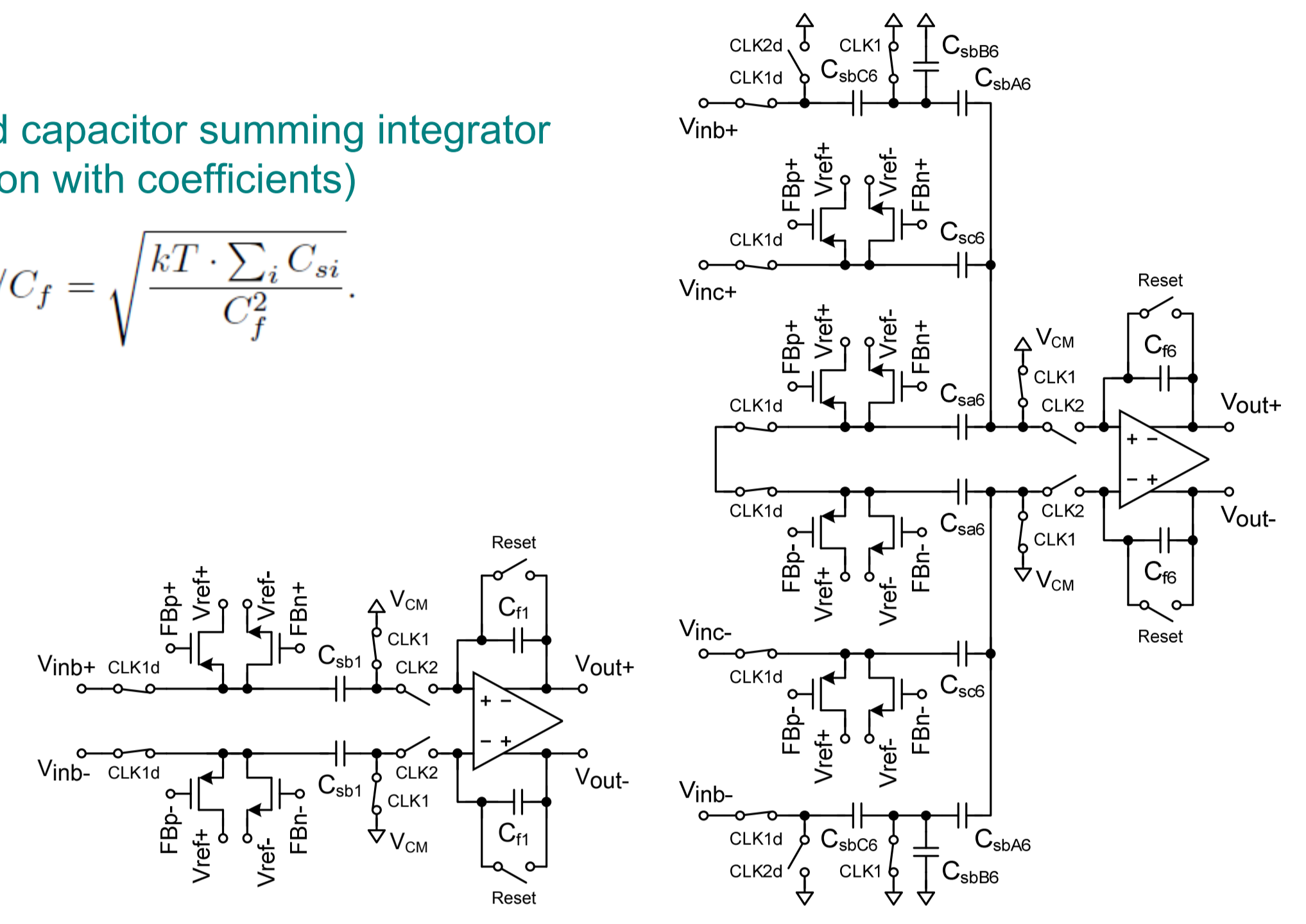
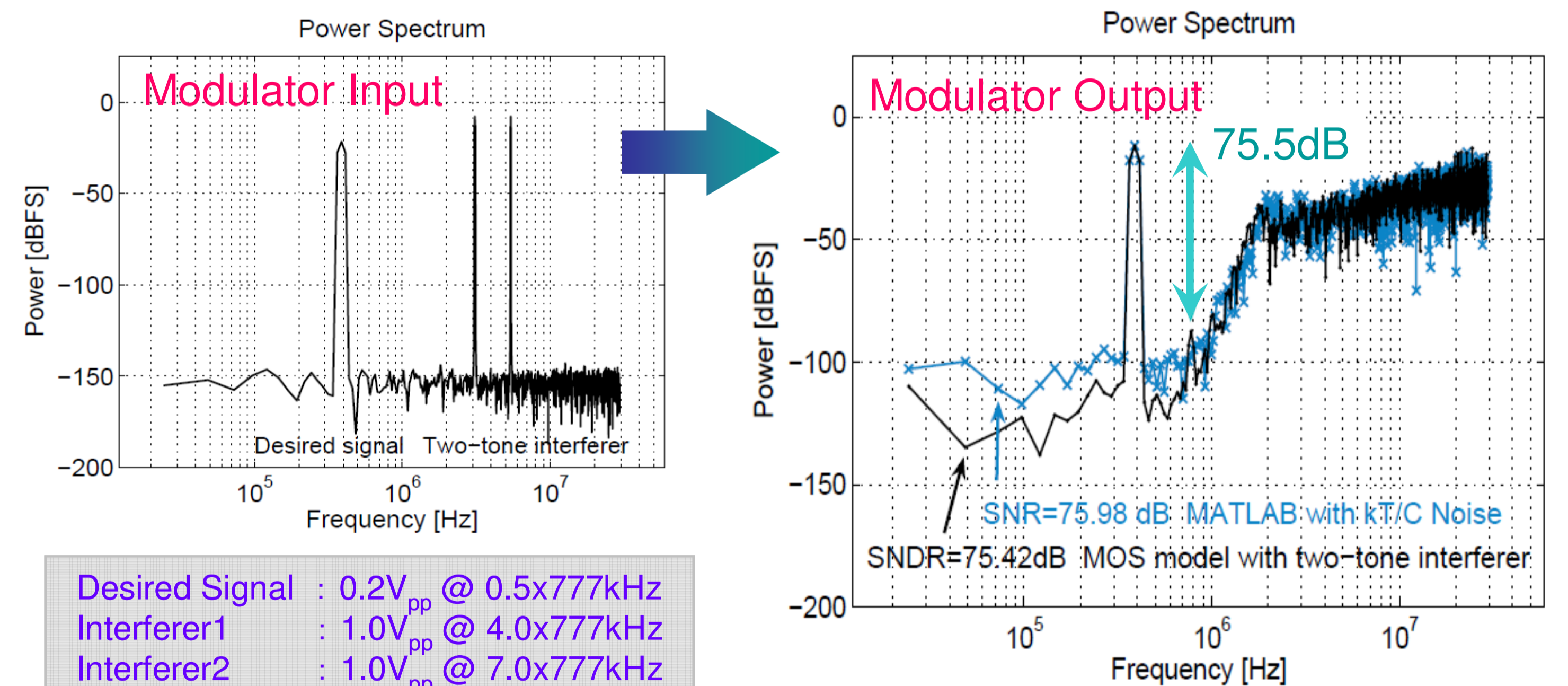1st summing Integrator   6th summing Integrator

5. Simulation Results

System Level simulation

Allowable interferer input level of notched STF is effectively increased.
(5th-order example)

Normal STF   Notched STF

Interferer Level (freq.=BWx4)   Desired Signal Level (freq.=BWx0.5)
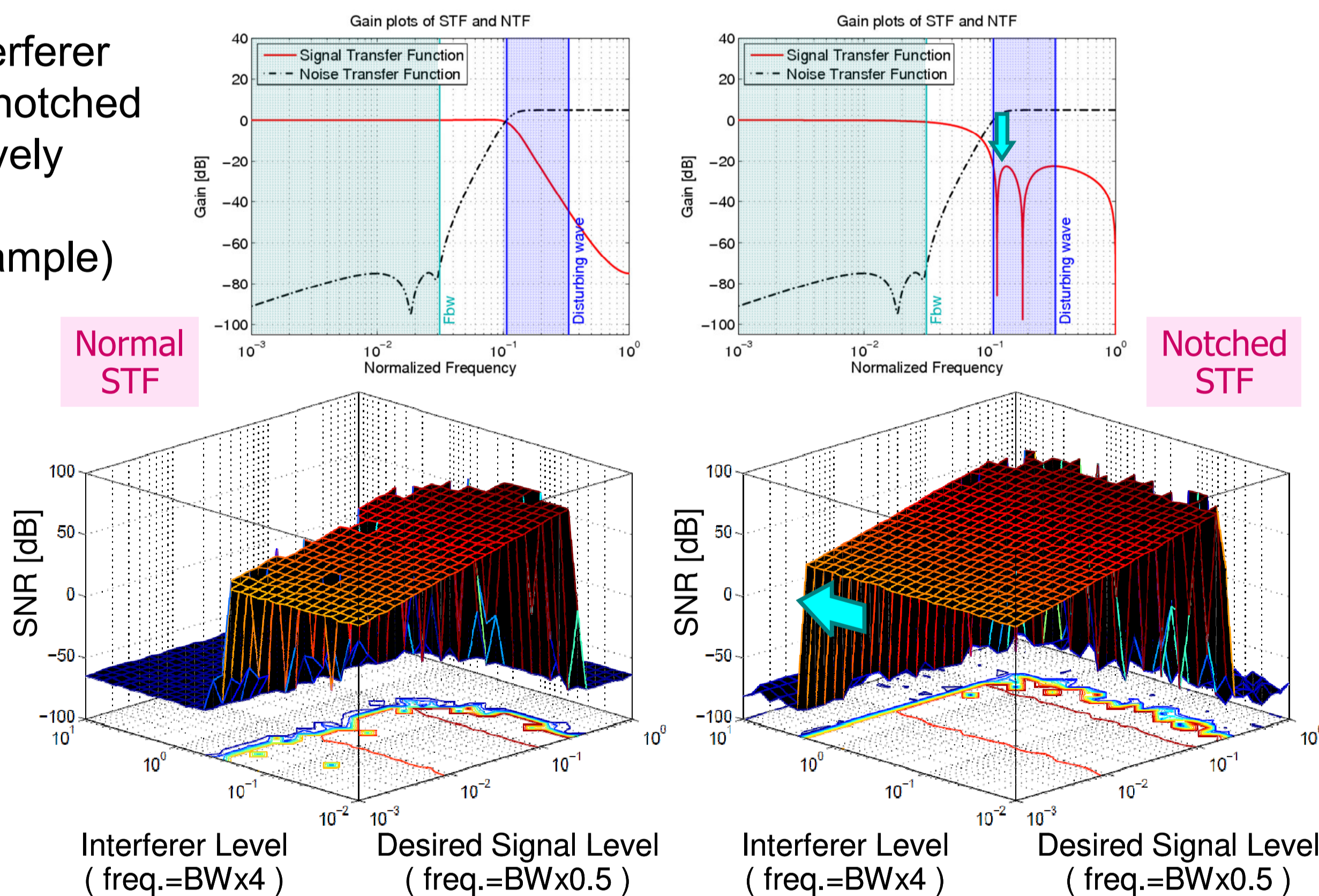
CMOS Level simulation

The effect of interferer suppression can be confirmed.

The IM3 from two-tone interferers is -75dB.
This is almost the same level as that of normal STF designed for comparison.

Power Spectrum — Modulator Input

Power Spectrum — Modulator Output   75.5dB

SNR=75.98 dB :MATLAB with kT/C Noise
SNDR=75.42dB :MOS model with two−tone interferer

Desired Signal : 0.2V_{pp} @ 0.5x777kHz
Interferer1 : 1.0V_{pp} @ 4.0x777kHz
Interferer2 : 1.0V_{pp} @ 7.0x777kHz

6. Influence of Noise

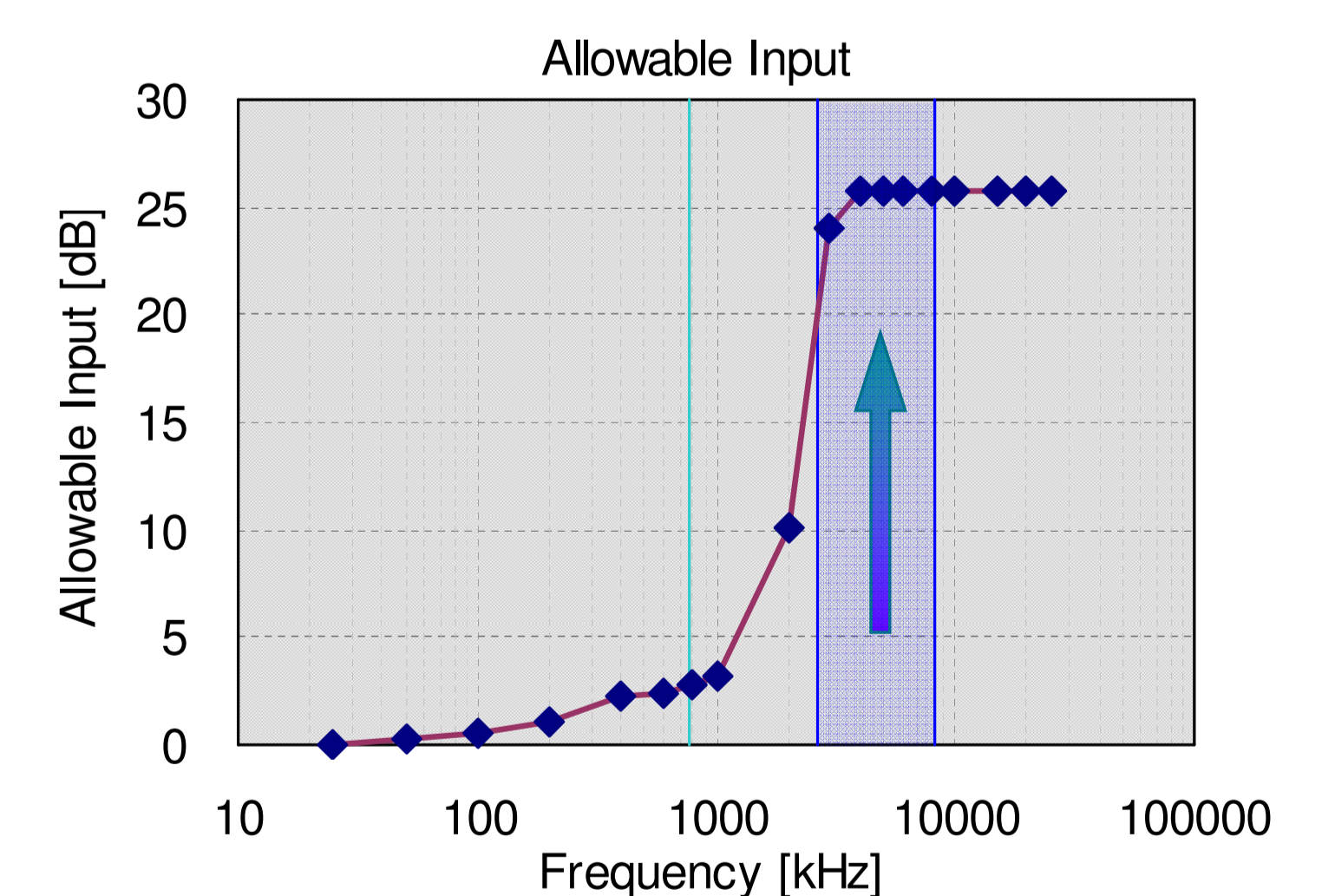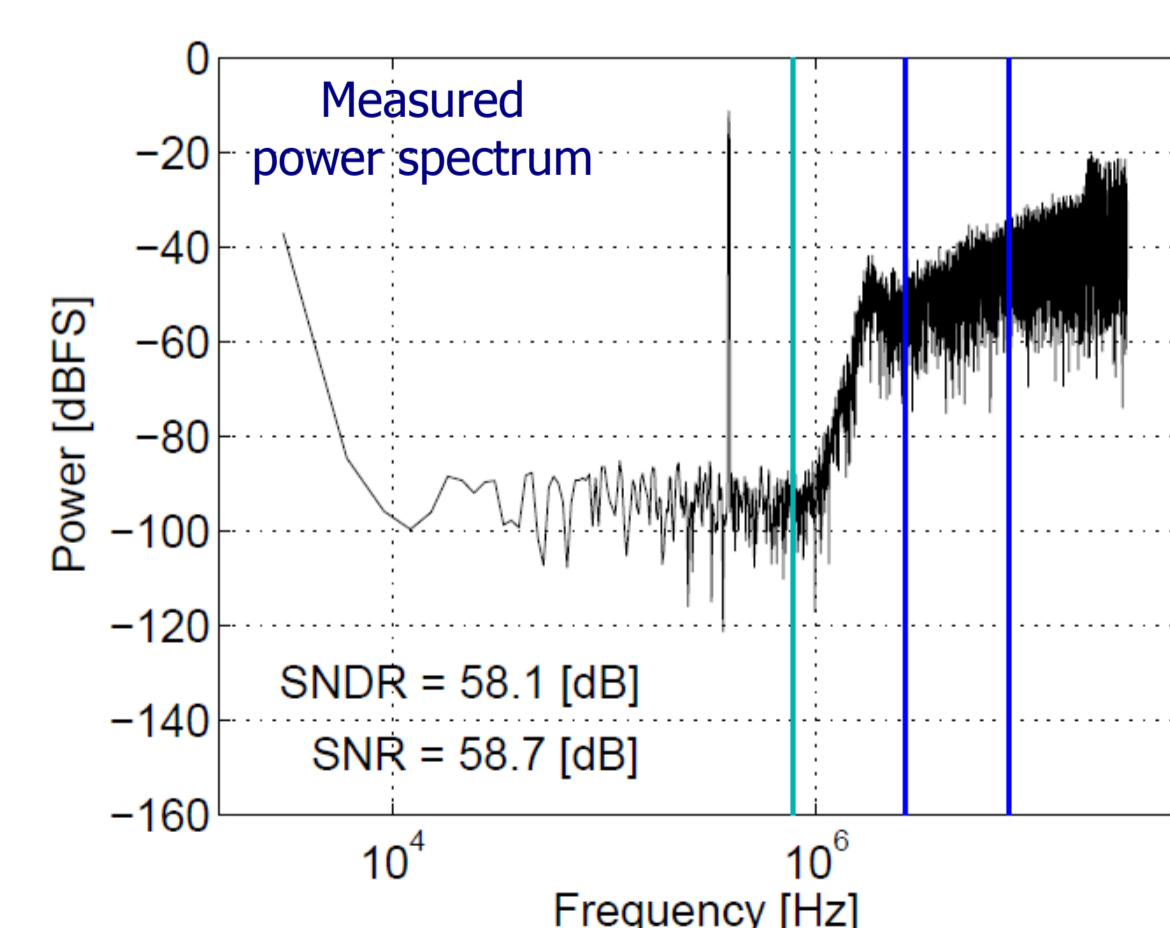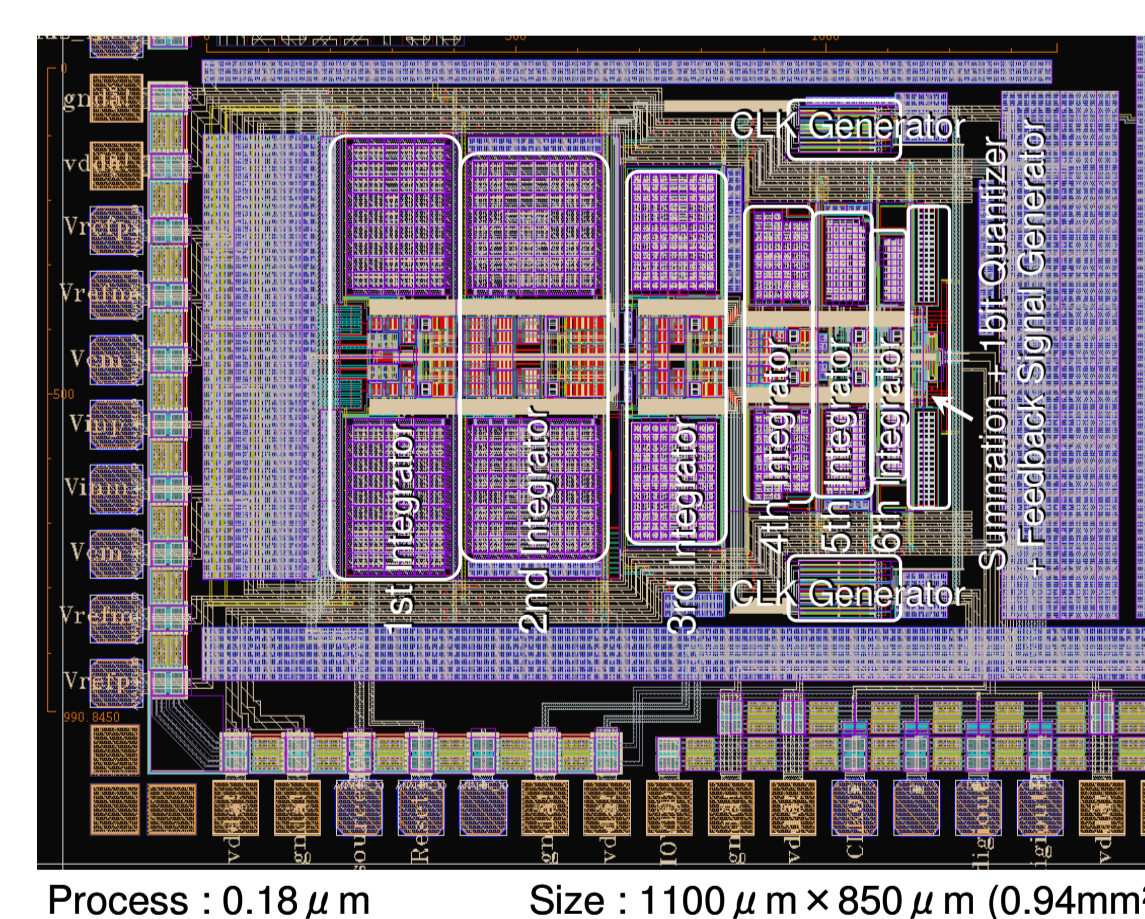In thermal noise dominated ΣΔ-Modulators, the effect of DR increase is lowered because of limited input signal amplitude and noise.

Vref should be lowered because the previous circuit output swing is limited.
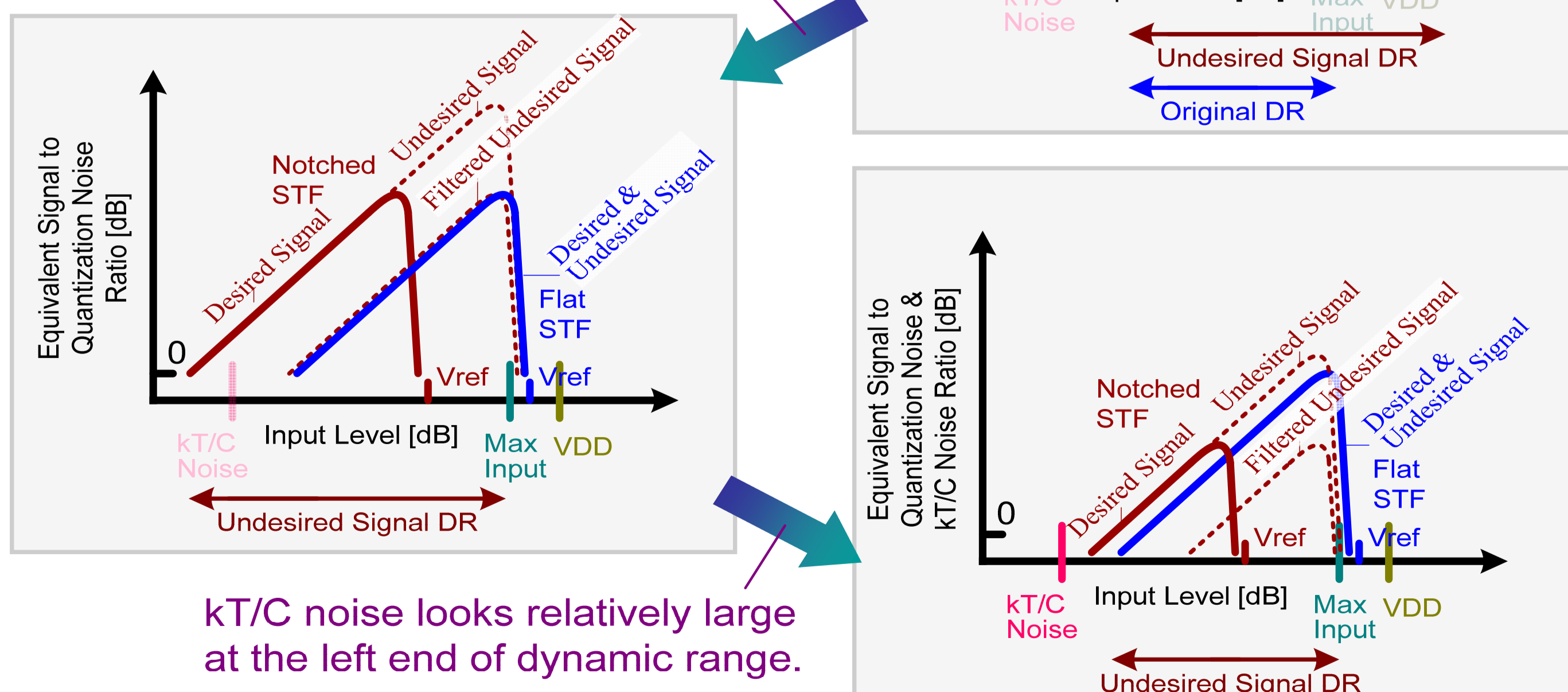
kT/C noise looks relatively large at the left end of dynamic range.

7. Measurement Results

Process : 0.18μm   Size : 1100μm × 850μm (0.94mm²)

Allowable Input

Measured power spectrum

SNDR = 58.1 [dB]
SNR = 58.7 [dB]

PERFORMANCE OF DESIGNED ΣΔ-MODULATOR.

Input Sampling Frequency	59.0625 MHz
Band Width	777 kHz
Interferer Frequency Range	2.65 MHz - 8.22 MHz
Interferer Suppression	20 dB+
Supply Voltage	1.8 V
CMOS Process	0.18 μm
Peak SNR (Designed)	70 dB+
Peak SNR (Measured)	59 dB
Power Consumption	45.5 mW
Core Size	0.94 mm²

8. Summary

1. Feedforward signal passes from input to each integrator can form zeroes in STF to suppress the nearby interferers strongly.
2. In thermal noise dominated ΣΔ-Modulator, the effect of DR increase is lowered because of limited input signal amplitude and noise.
3. A prototype 777-kHz BW DT 6th-order ΣΔ-Modulator has been designed and implemented in 0.18um CMOS technology.
4. This architecture is practically effective to keep the modulator stable even when strong nearby interferers attack the receiver.