

Digital-Centric RF CMOS Technology

Akira Matsuzawa

Tokyo Institute of Technology, S3-27, 2-12-1, O-okayama, Meguroku, Tokyo, 152-8552, Japan.

ABSTRACT — Analog-centric RFCMOS technology has played important role to give the motivation to change the technology from conventional discrete device technology or bipolar IC technology to CMOS technology. However it has many issues such as poor performance, weak in PVT fluctuations, and cost increase with technology scaling. The most important advantage of CMOS technology to legacy RF technology must be the feature that CMOS can use more high performance digital circuits with cheapest cost. In fact, analog-centric RF-CMOS technology has failed the FM/AM tuner applications and the digital-centric CMOS technology is becoming attractive for many users. It has many advantages; such as high performance, no adjustment points, high productivity, and low cost.

Therefore digital-centric RF CMOS technology must be right way and digital-RF technology that uses digital technology to RF circuits directly has emerged, however it is not matured and further investigations are expected.

Index Terms — CMOS, RF, analog, digital, tuner, PLL, sampling, mixer, wireless.

I. INTRODUCTION

RF CMOS technology has an idea to integrate every needed components, circuits, and functions for realizing wireless systems to increase the performance and to decrease power consumption and cost [1]. It is however not easy to integrate analog and RF circuits with highly-scaled CMOS technology [2].

This paper reviews the current status of FA/AM tuner ICs in which CMOS technology has not been used sufficiently and will reveal the advantage of the digital-centric RF CMOS technology compared to conventional analog-centric technology. Furthermore digital RF technology that uses digital technology to RF circuits will be reviewed to point out the features and issues on this technology.

II. Analog-centric RF CMOS technology

An application of CMOS technology to FM/AM tuners sounds easy compared to wireless network systems and cellular phone systems, however the most toughest area in reality. Low frequency requires so large inductors and capacitors that the integration on a chip is not reasonable and results in requiring many external components. AM signal is suffered by $1/f$ noise directly, furthermore higher sensitivity and higher durability

against the unwanted signals are requested compared to the wireless network systems and the cellular phone systems.

Figure 1 and figure 2 show current FM/AM tuner board and block diagram, respectively. Many external components and many adjustment points are needed, for example; in this case, three ICs, 187 external components, and 12 adjustment points are needed.



Fig. 1. Current FM/AM tuner board.

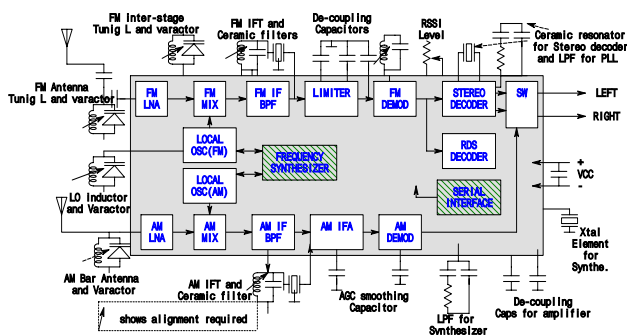


Fig. 2. Block diagram of current FM/AM tuner.

Table 1. Analog-centric technology and issues.

Parts	Methods for on-chip	Problems
AM/FM IF BPF	1. Low IF (a few hundred KHz) 2. Gm-C BPF with auto alignment, SCF	1. poor selectivity(-45dB), 2. SCF Switch noise 3. Center frequency shift by DC offset 4. Poor image rejection ratio (25 to 35dB)
FM Demodulator	Pulse count FM detector	Poor THD (0.5%)
Stereo Decoder	Multi-vibrator VCO, SCF filter	Large variation of free-run frequency Still need external LPF for PLL
RSSI Level adj.	Signal detector with DC compensation	Can't cover all process corner
Varactor	MOS varactor	Too much sharp C-V curve, distorted signal
AGC smoother	Time division charge and discharge	Needs large capacitor for low audio frequency
Capacitors	Stages Direct connection, use small value coupling capacitor	High impedance required, Difficult for low frequency

The first trial to apply CMOS technology to this FM/AM tuner started to integrate the functions of these

external components on a chip by using analog-centric technology.

Table 1 shows the used circuit technologies and caused problems. Low IF architecture has been chosen to address 1/f noise and DC offset issues. Active filters; such as gm-C filter and switched capacitor filter were used for channel select filters and poly-phase filter was used to reject image signal. Pulse count method and multi-vibrator circuit were used for FM demodulation and reconstruction of stereo sound, respectively.



Fig. 3. FM/AM tuner board using analog-centric CMOS IC.

Figure 3 shows FM/AM tuner board using analog-centric CMOS IC. The performance was not attractive. The selectivity and image rejection ratio were only -45 dB and 30 dB, respectively. Furthermore performance was seriously affected by PVT fluctuations and productivity was not sufficient. The number of external components was 69 and the number of adjustment points was 11. Thus both performance and cost are not attractive to users in spite of use of advanced CMOS technology.

III. Digital-centric RF CMOS technology

This fail of IC development promoted to change the technology from analog-centric IC technology to digital-centric IC technology. Use of analog technology should be minimized and use of digital technology should be maximized.

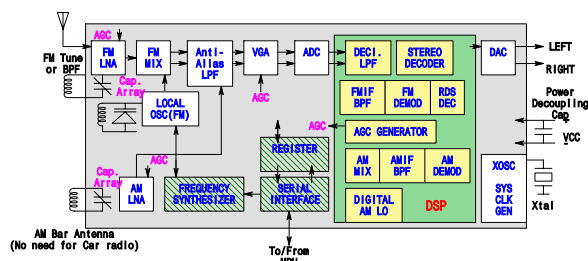


Fig. 4. Block diagram of digital-centric CMOS LSI for FM/AM tuner.

Figure 4 shows a block diagram of digital-centric RF CMOS IC for FM/AM tuner.

Low IF architecture was used for FM signal. The digital filter was used for the channel select filter and attained high selectivity of 65 dB. AM modulation signal is directly converted to digital signal and demodulated by multiplication of negative carrier frequency as shown in (1) in digital domain.

$$[1 + S(t)]\exp(j\omega t) \times \exp(-j\omega t) = [1 + S(t)] \quad (1)$$

FM signal can be demodulated by time derivation of phase component as shown in (2) (3).

$$R(t)\exp\left(j\left(\Delta\omega t + K_d \int m(\tau)d\tau\right)\right) \quad (2)$$

$$\frac{d\theta}{dt} = \Delta\omega + K_d m(t) \quad (3)$$

The stereo signal has the following structure.

$$S(t) = (L + R) + (L - R)\cos\omega_s t + K \cos\omega_p t \quad (4)$$

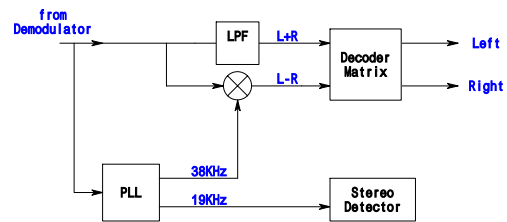


Fig. 5. Demodulation system for stereo signal.

Thus the stereo sound is reconstructed in digital domain using the block diagram shown in figure 5. PLL, mixer, and filter are formed in digital domain. A good stereo separation of 55 dB has been attained.

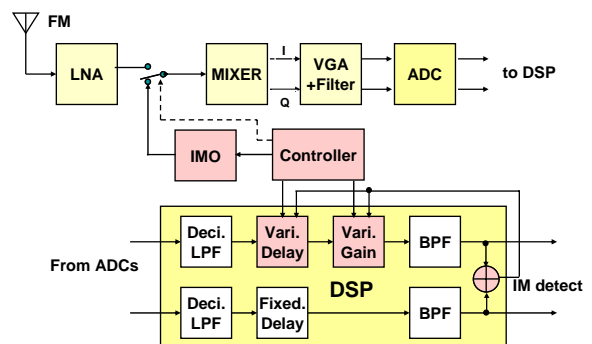


Fig. 6. Image rejection system.

A conventional image reject ratio by using analog method is about 40 dB, at most. Thus digital image

rejection method shown in figure 6 was applied to attain the image rejection ratio of more than 60 dB.

Image signal oscillator generates the image signal and the controller controls signal delay and gain in one path of I/Q signal to minimize the image signal in digital domain.

Figure 7 shows the tuner board on which the digital-centric RF CMOS IC is mounted. The number of external components is only 11 and no adjustment point is required. This IC can realize stable signal receiving by controlling gain of each stage and various parameters by monitoring unwanted signals, as well as wanted signal.



Fig. 7. FM/AM tuner board using digital-centric CMOS LSI.

IV. Digital-RF technology

The global trend of RF CMOS technology is to use digital technology as much as possible and to use analog technology for only essential parts [3]. The biggest reason of this trend is that analog circuits are seriously affected by device mismatches, PVT fluctuations, and change of environment, as a result, the performance and production yield are unstable. The other reason is the cost increase by technology scaling.

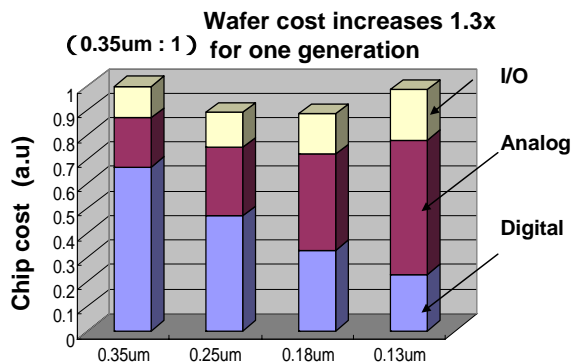


Fig. 8. Estimated cost of mixed signal LSI.

Figure 8 shows the cost estimation of mixed signal LSI for each technology generation normalized by 0.35 um CMOS under the assumption that the areas of the original LSI are 70% for digital circuits and 30% for analog and I/O circuits and the area for digital circuit will be reduced along with technology scaling and area for analog and I/O circuits are kept same. The cost for analog will increase even if area is kept same, because wafer cost increases about 30% for one technology generation advance. Thus it is important to shrink analog circuits along with technology scaling [3].

Furthermore, more flexible and reconfigurable wireless systems are demanded to realize multi-standard and multi-mode wireless systems and technology called “digital RF” has emerged [4]. The proposed technologies are full digital PLL and sampling mixer.

1) Full digital PLL

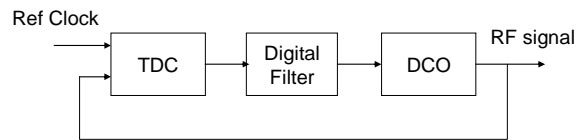


Fig. 9. Full digital PLL.

Figure 9 shows system configuration of full digital PLL [5] [6]. Time to Digital Converter (TDC), digital filter, and Digital controlled Oscillator (DCO) are used instead of conventional Phase Frequency Detector (PFD), analog filter, and Voltage Controlled Oscillator (VCO), respectively.

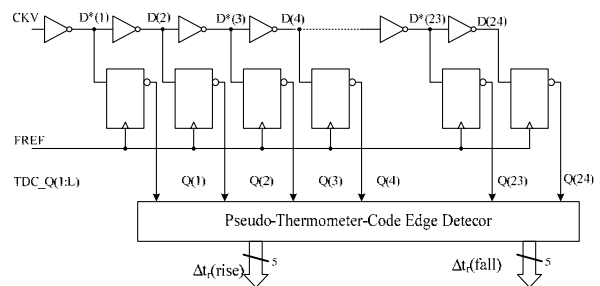


Fig. 10. Time to Digital Converter.

TDC uses inverter delay circuits and latches and realizes several 10 ps resolution, as shown in figure 10. DCO uses array of varactors. A conventional VCO also uses varactors, however the DCO uses different operation mode, as shown in figure 11.

DCO uses two low sensitive regions and changes the number of states by digital words in contrast to that the sensitive region is used in a conventional VCO. One serious issue of VCO is increase of phase noise caused by modulation of varactor voltage in high sensitive

operating region. The digital control in low sensitive region is the effective solution. However one issue of

Fig. 11. Digital Controlled Oscillator (DCO).

this DCO is to require very small capacitance to realize high control resolution of oscillating frequency. A very small capacitance of less than 1 fF is required and it is not easy to realize extremely small capacitance. The delta-sigma method can relax this issue however some noise will be caused and will increase phase noise.

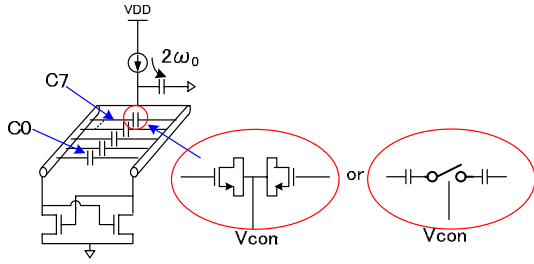


Fig. 12. DCO using distributed capacitor array along with transmission line.

To address this issue, we proposed distributed capacitor array along with transmission line, shown in figure 12 [7]. The voltage of oscillating wave has a distribution along with position. At the open end the voltage is largest and at the short end it is smallest, thus the sensitivity of capacitor to oscillating frequency depends on the position, as shown in figure 13.

The large dynamic range of sensitivity more than 100 has been measured and this effect will relax the capacitor array issue. We will realize more fine resolution DCO with reasonable capacitors.

The TDC looks having another issue. The resolution of current TDC is determined by the signal propagation delay of inverters. Furthermore latches and inverters have an uncertainty in timing; therefore time resolution may not be improved by technology scaling. Further investigation on TDC is required.

2) Sampling mixer

A sampling mixer is an interesting idea to process the RF signal [4]. The signal processing method for RF signal is conventionally continuous time method, however recent technology scaling enables to apply the discrete time signal processing to RF signal. Figure 14 shows the sampling mixer circuit. RF signal is sampled and array of passive switched capacitor circuits realizes filter function without any active circuits such as operational amplifiers.

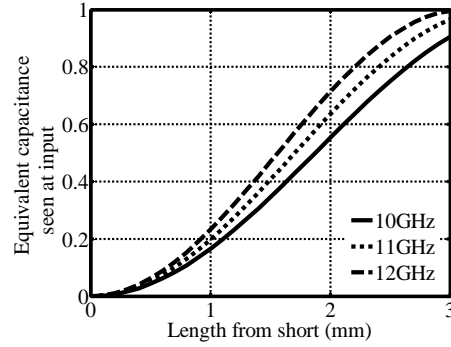
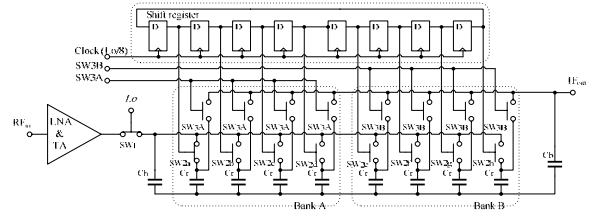


Fig. 14. Sampling mixer.

$$|H(f)| = (1-a) \frac{\left| \frac{\sin\left(MN\pi\frac{f}{f_s}\right)}{\sin\left(\pi\frac{f}{f_s}\right)} \right|}{\sqrt{1+a^2-2a\cos\left(N2\pi\frac{f}{f_s}\right)}} \frac{1}{\sqrt{1+b^2-2b\cos\left(MN2\pi\frac{f}{f_s}\right)}}$$

The transfer function of this circuit is;



(5)

where,

Figure 15 shows frequency characteristics. Relatively sharp filter characteristics as a RF filter and second order filter function as a base band filter can be obtained. Also mixing function can be realized through sampling process.

This circuit technology looks interesting for future multi-band and multi-mode wireless systems; this is because the filter characteristics can be changed easily by changing the number of taps, capacitor ratios, and clock frequency. However performance is not sufficient for many applications, in particular for wide band systems and wide change of clock frequency is not easy. Then tuner application sounds difficult. Furthermore no remarkable advantage compared to conventional mixer and continuous time base-band filter has been demonstrated. This technology also needs further investigation.

$$a = \frac{C_h}{C_h + C_r} \quad b = \frac{C_b}{4C_r + C_b}$$

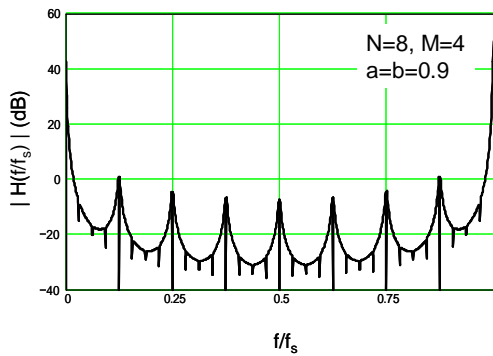


Fig. 15. Frequency characteristics of the sampling mixer.

V. Conclusion

Analog-centric RFCMOS technology has played important role to give the motivation to change the technology from conventional discrete device technology or bipolar IC technology to CMOS technology. However it has many issues such as poor performances, weak in PVT fluctuations, and cost increase with technology scaling. The most important advantage of CMOS technology to legacy RF technology must be the feature that CMOS can use more high performance digital circuits with cheapest cost. In fact, analog-centric RF-CMOS technology has failed the success of FM/AM tuner business and the digital-centric CMOS technology is becoming attractive for many users. It has many advantages; such as high performance, no adjustment points, high productivity, and low cost.

Therefore digital-centric CMOS technology must be right way and digital RF technology that can apply digital technology to RF circuits has emerged, however it is not matured and further investigations are expected.

ACKNOWLEDGEMENT

The authors wish to acknowledge Niigata-Seimitsu Corporation for disclosing the technology of RF-CMOS IC for FM/AM tuner and Win Chaivipas for his advice to full digital PLL technology.

REFERENCES

- [1] Akira Matsuzawa, "RF-SoC -Expectations and Required Conditions," IEEE Tran. On Microwave Theory and Techniques, Vol. 50, No. 1, pp. 245-253, Jan. 2002.
- [2] Akira Matsuzawa, Mixed Signal SoC Era," IEICE, Trans. Electron., Vol. E87-C, No. 6, pp. 867-877, June, 2004.
- [3] Akira Matsuzawa, " Analog IC Technologies for Future Wireless Systems", IEICE Trans. Electron, vol. E89-C, No. 4, pp. 446-454, Apr. 2006.
- [4] R.B. Staszewski, K. Muhammad, D. Leipold, Chih-Ming Hung, Yo-Chuol Ho, J.L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, Jinseok Koh, S. John, Irene Yuanying Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O.E. Eliezer, E. de-Obaldia and P.T. Balsara, "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, pp. 2278-2291, December 2004.
- [5] R. B. Staszewski, D. Keipold, K. Muhammad and P. T. Balsa, "Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicrometer CMOS Process," IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 50, No. 11, pp.815-828, November 2003.
- [6] R. B. Staszewski, C-M. Hung, D. Keipold and P. T. Balsa, "A First Multi-gigahertz Digitally Controlled Oscillator for Wireless Applications," IEEE Trans. on Microwave Theory and Techniques, Vol. 51, No. 11, pp.2154-2164, November 2003.
- [7] Win Chaivipas, Takeshi Ito, Takashi Kurashina, Kenichi Okada, and Akira Matsuzawa "Fine and Wide Frequency Tuning Digital Controlled Oscillators Utilizing Capacitance Position Sensitivity in Distributed Resonators", A-SSCC 2007.