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Trends in high speed ADC design

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Speed and power

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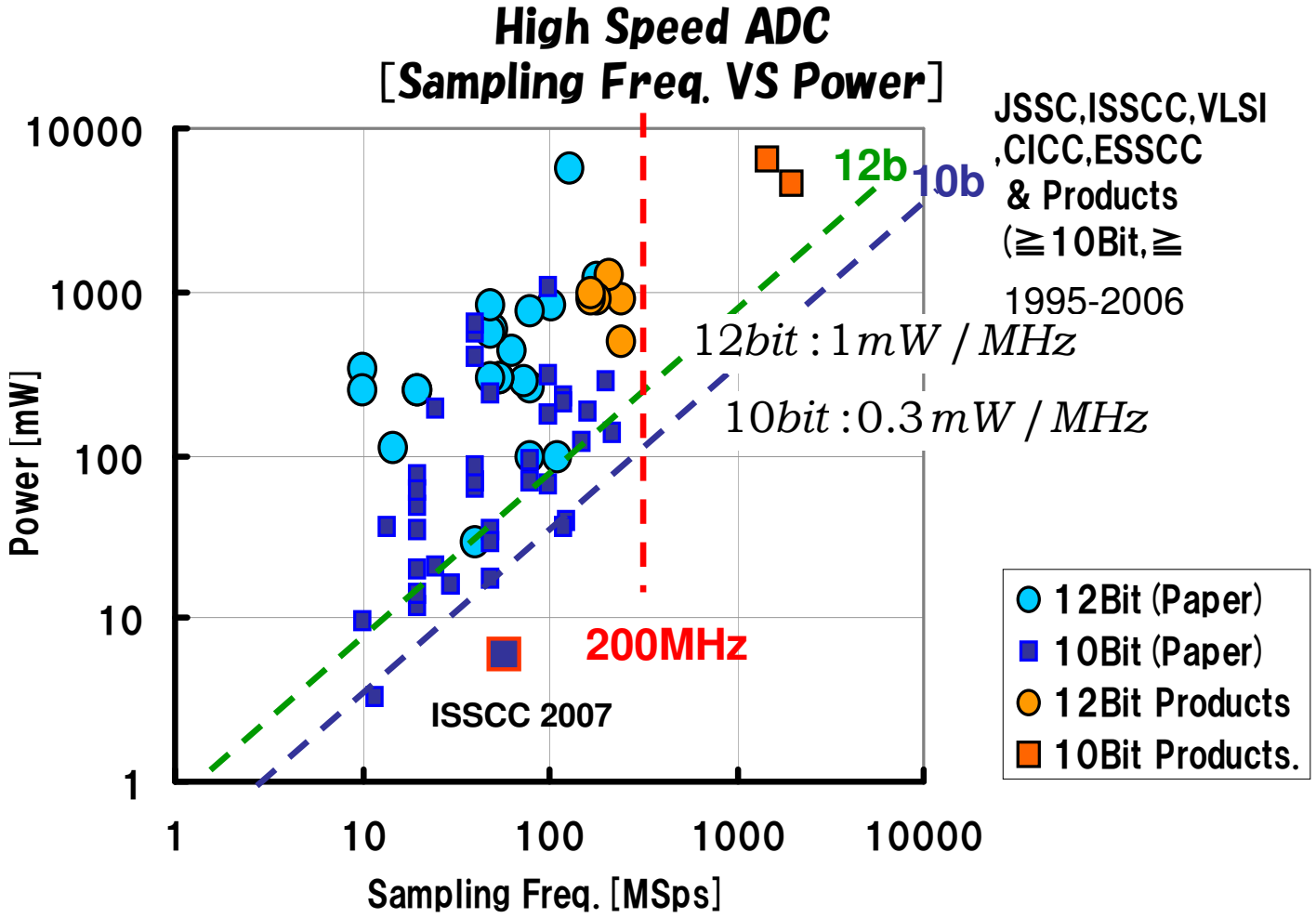
Conversion speed has saturated at 200 MHz
Smaller mW/MHz is needed for low power operation.
0.3mW/MHz for 10bit and 1mW/MHz for 12bit are the bottom lines.



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Pipelined ADC

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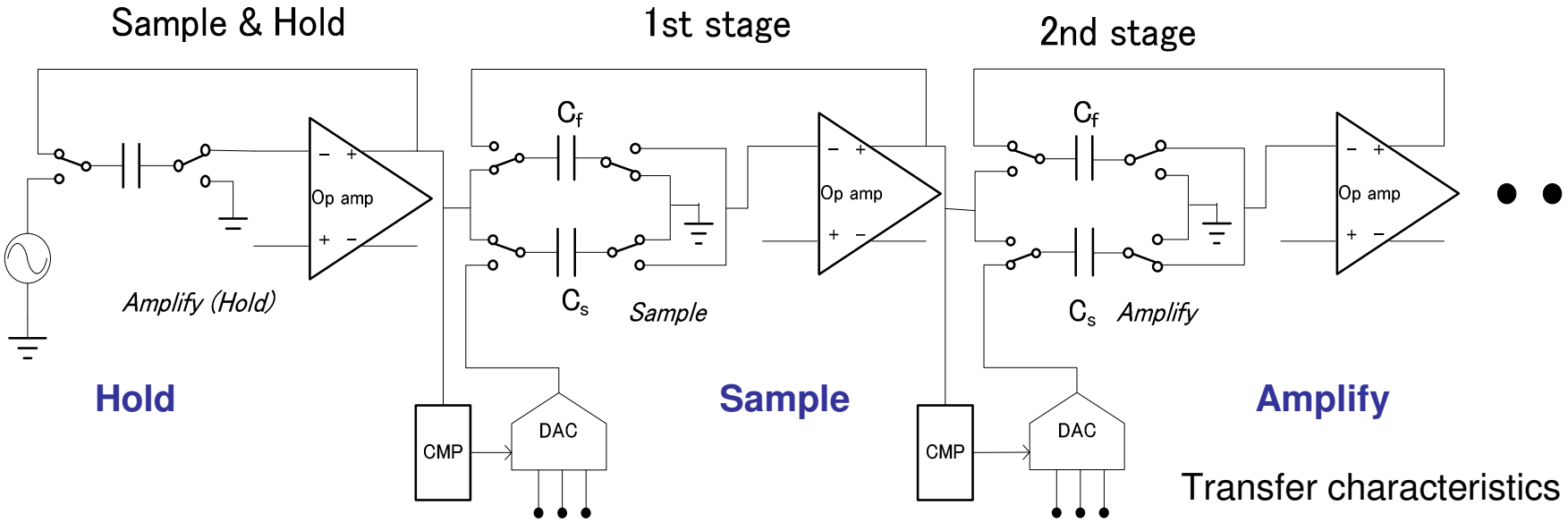
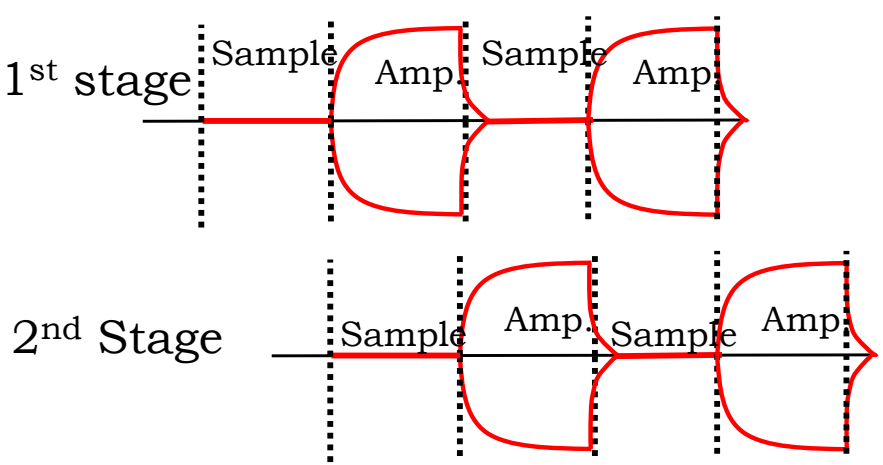
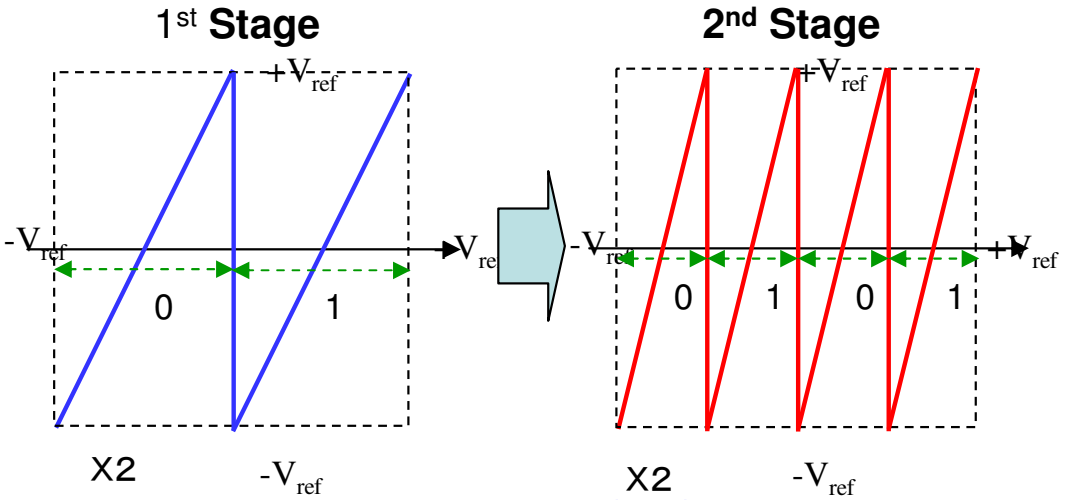
Folding I/O characteristics makes higher resolution along with pipeline stages.







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Technology scaling for analog

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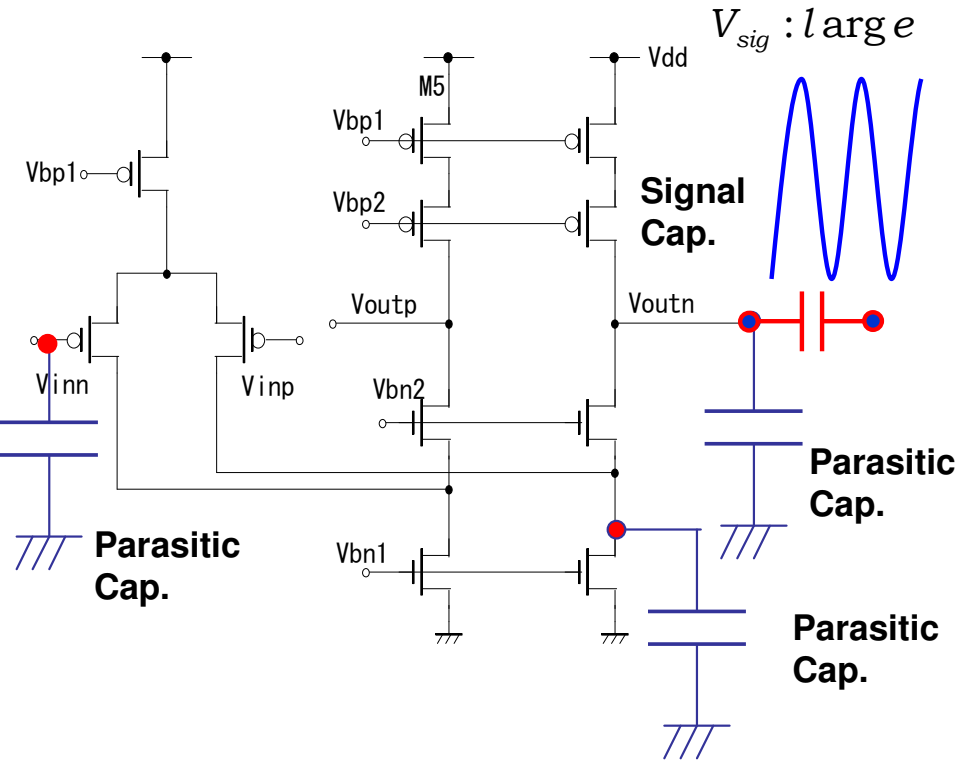
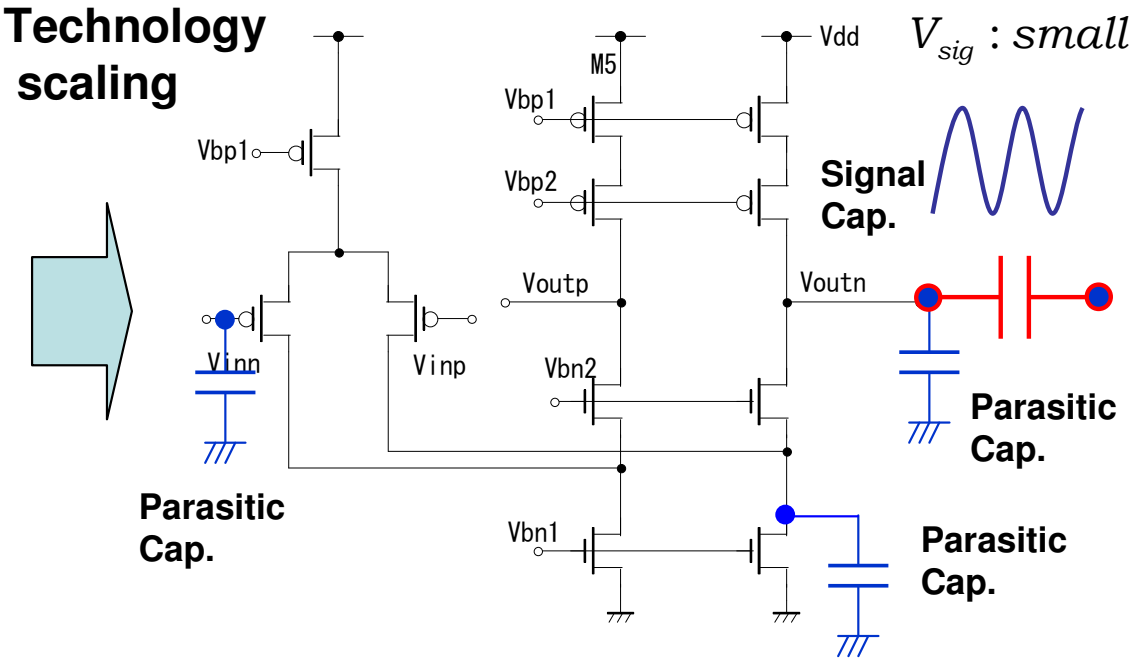
Technology scaling can reduce parasitic capacitances. However signal capacitance will increase to keep the same SNR at lower voltage operation.

Parasitic capacitance → smaller
Operating voltage → lower
Signal swing → lower

Signal capacitance →larger
Voltage gain →lower



Technology scaling



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Performance model for pipelined ADC

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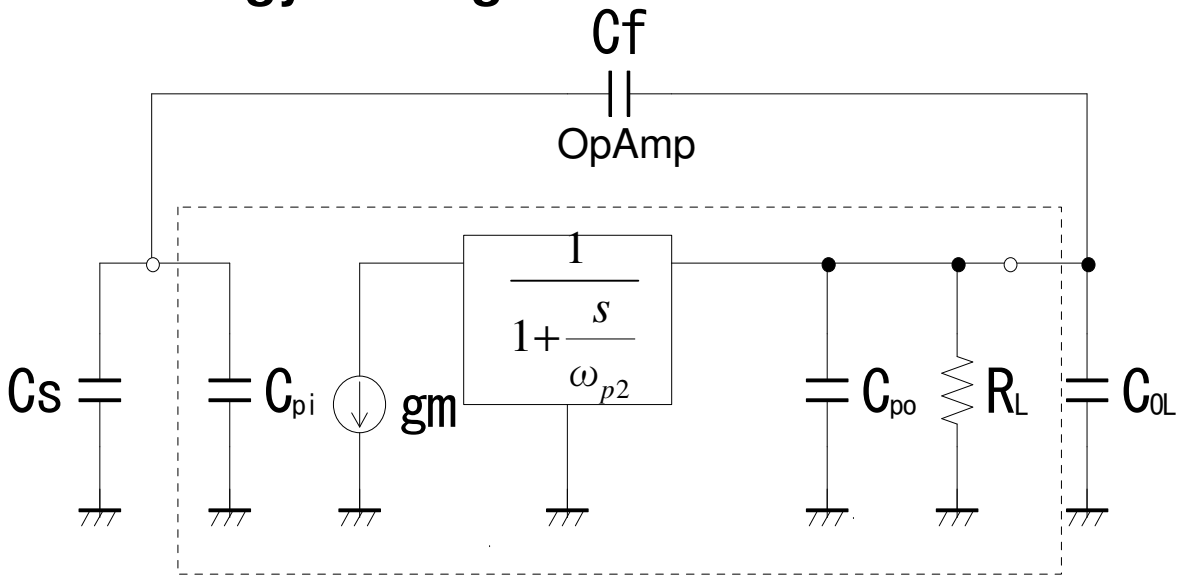
We have developed the performance model for pipeline ADC that can treat technology scaling.



g_m : *Transconductance of input stage*

C_s, C_f : *Signal capacitance for feedback loop*

C_{pi}, C_{po} : *input & putput paracitic capacitance*

C_{oL} : *Load capacitance*

R_L : *Output resistance*

ω_{p2} : *Second pole of OpAmp*

A. Matsuzawa, "Analog IC Technologies for Future Wireless Systems," IEICE, Tan on Electronics, Vol. E89-C, No.4, pp. 446-454, April, 2006.

$$GBW_{\_close} = \frac{g_m}{2\pi C_L}\beta$$

$$\beta = \frac{C_f}{C_f + C_s + C_{pi}}$$

$$C_L = C_{po} + C_{oL} + \frac{C_f\left(C_s + C_{pi}\right)}{C_f + C_s + C_{pi}}$$

$$C_{oL} = \frac{C_s + C_f}{2} \qquad C_o = C_s = C_f = C_{oL}$$

$$GBW_{\_close} = \frac{g_m}{2\pi C_o}\frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)} = \frac{I_{ds}}{\pi C_o V_{eff}}\frac{1}{\left(2+\frac{\alpha_{pi}I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po}I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi}I_{ds}}{C_o}\right)}$$

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Scaling and analog device and circuit parameters

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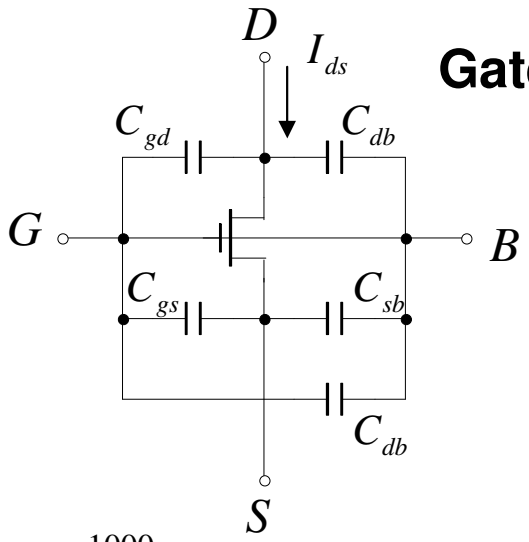
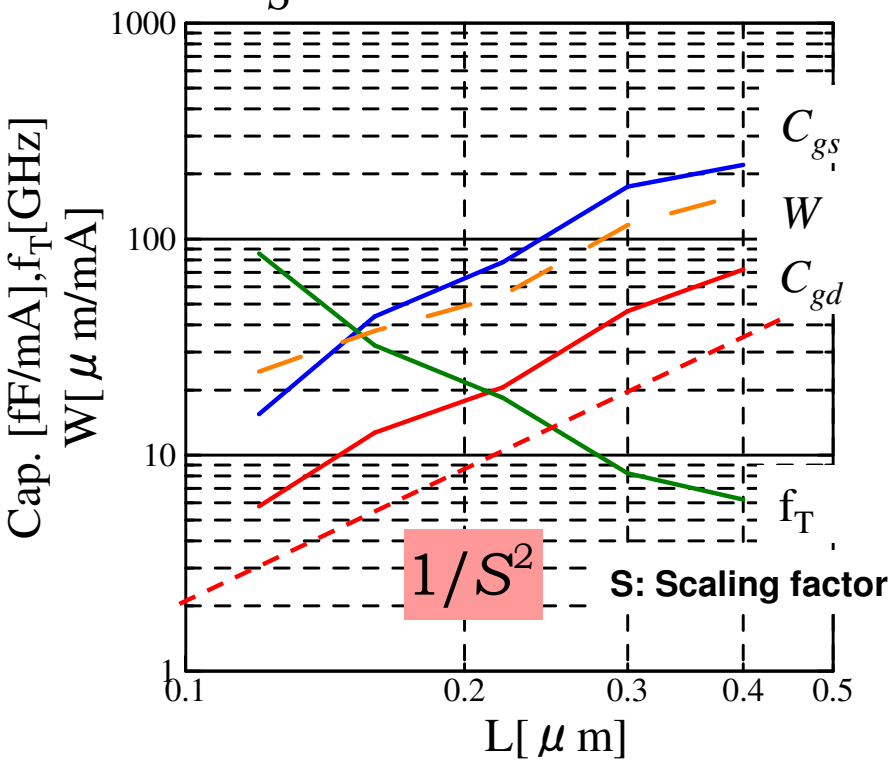


Gate width and capacitances decrease with technology scaling.

V_{eff}=0.175V

$$W = \frac{2L}{\mu C_{ox} V_{eff}^{\ 2}} I_{ds}$$



(a)W_N,W_P[μm/mA],V_{A_N}, V_{A_P}[V]

DR	W_N	W_P	V_{A_N}	V_{A_P}
90nm	24.3	74.9	0.82	0.69
0.13μm	37.5	147	0.82	0.64
0.18μm	54.8	219	0.99	0.93
0.25μm	116.0	396	0.78	0.97
0.35μm	162.0	603	1.01	0.86

(b)C_{pi_N}, C_{pi_P},C_{po}[fF/mA], ω_{p2_N}, ω_{p2_P}[GHz]

DR	C_{pi_N}	C_{pi_P}	C_{po}	ω_{p2_N}	ω_{p2_P}
90nm	23.7	93.4	94.5	9.35	15.4
0.13μm	65.5	249	168	7.7	10.3
0.18μm	115	475	340	2.06	4.7
0.25μm	236	662	832	0.83	1.7
0.35μm	303	1034	892	0.54	1.7

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Determination of signal capacitance

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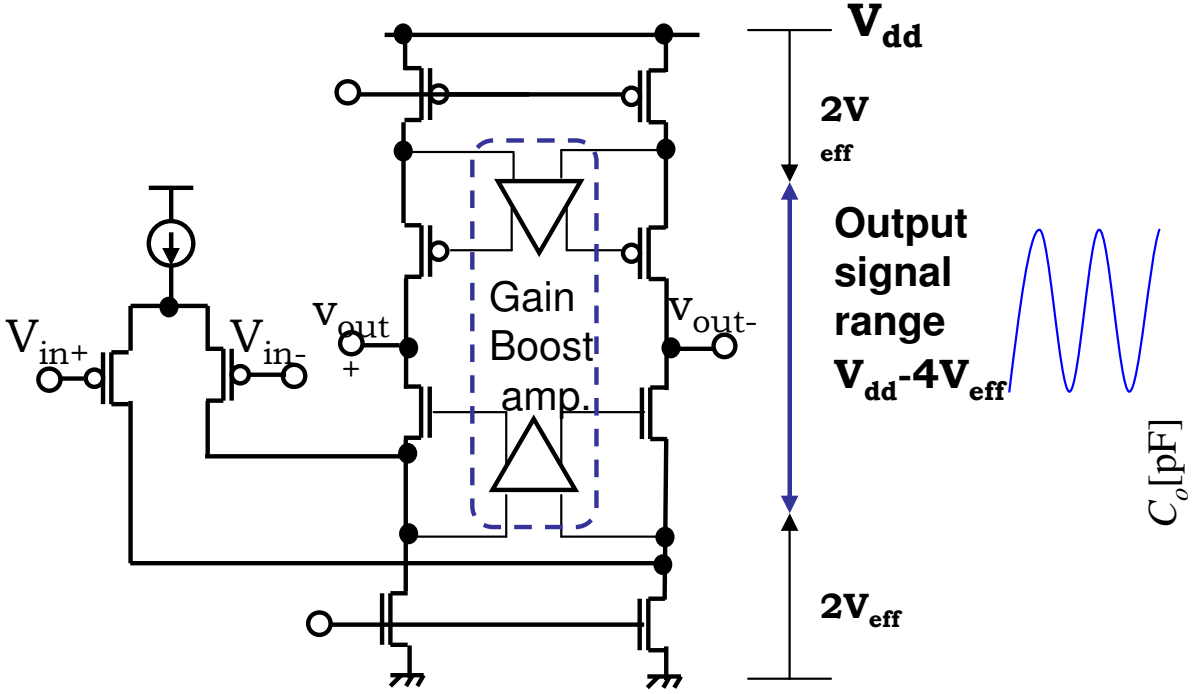
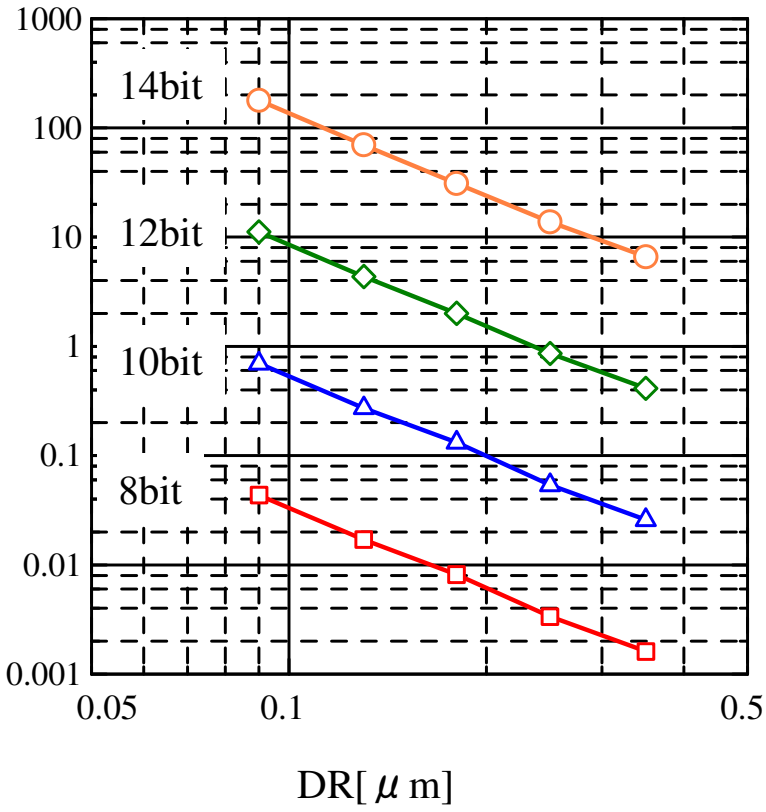
Larger resolution requires larger signal capacitance.
Furthermore, Voltage lowering increases signal capacitance more.

$$C_o \geq 1.66\times10^{-19}\left(\frac{2^N}{V_{sig}}\right)^2$$





	90nm	0.13 μm	0.18 μm	0.25 μm	0.35 μm
V_{dd}	1.2V	1.5V	1.8V	2.5V	3.3V
V_{sig_pp}	1.0V	1.6V	2.2V	3.6V	5.2V

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Performance curve

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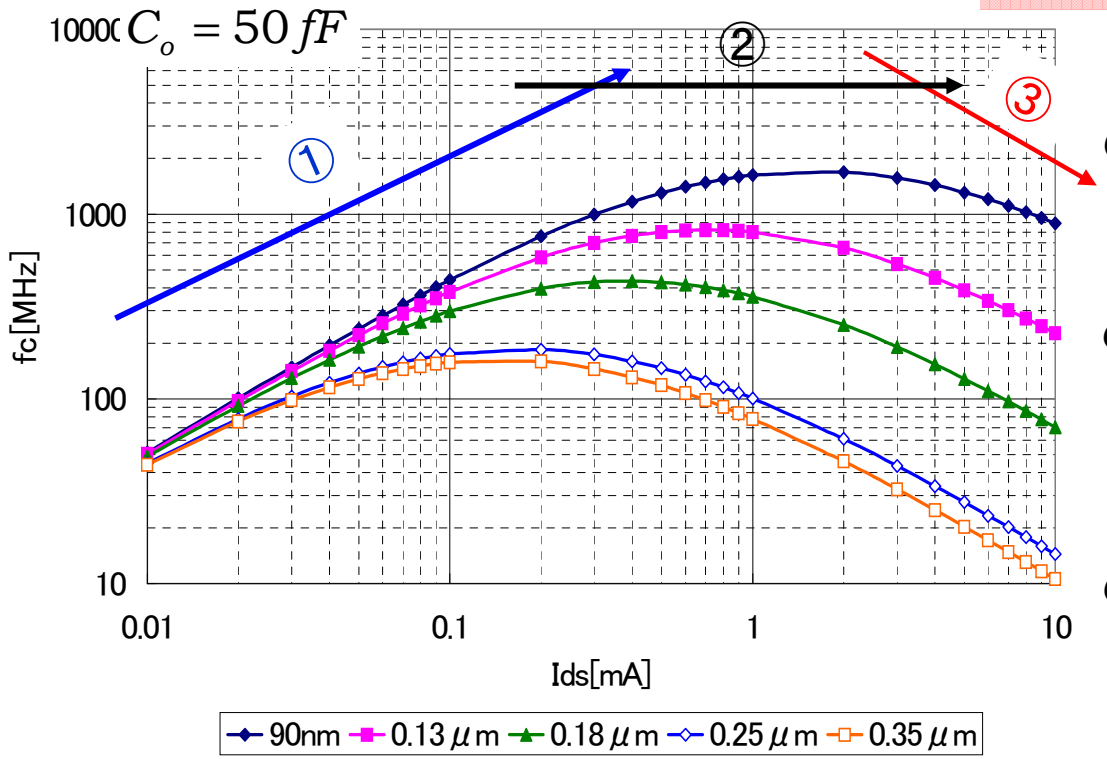
Performance exhibits convex curve.
There is the peak conversion frequency and the optimum current.
Current increase results in increase of parasitic capacitances and decrease of conversion frequency in the higher current region.

$$GBW_{\_close} = \frac{I_{ds}}{\pi C_o V_{eff}} \frac{1}{\left(2+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi} I_{ds}}{C_o}\right)}$$



① $C_o \gg C_{po}, C_{pi}$

$$GBW_{\_close} \approx \frac{I_{ds}}{\pi C_o V_{eff}} \cdot \frac{1}{3} \qquad (\propto I_{ds})$$

② $C_{pi} < C_o < C_{po}$

$$GBW_{\_close} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3+\alpha_o} \qquad (Constant)$$

③ $C_o < C_{po}$、$C_o < C_{pi}$

$$GBW_{\_close} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3+\alpha_i \alpha_o I_{ds}} \qquad (\propto \frac{1}{I_{ds}})$$

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Performance summary

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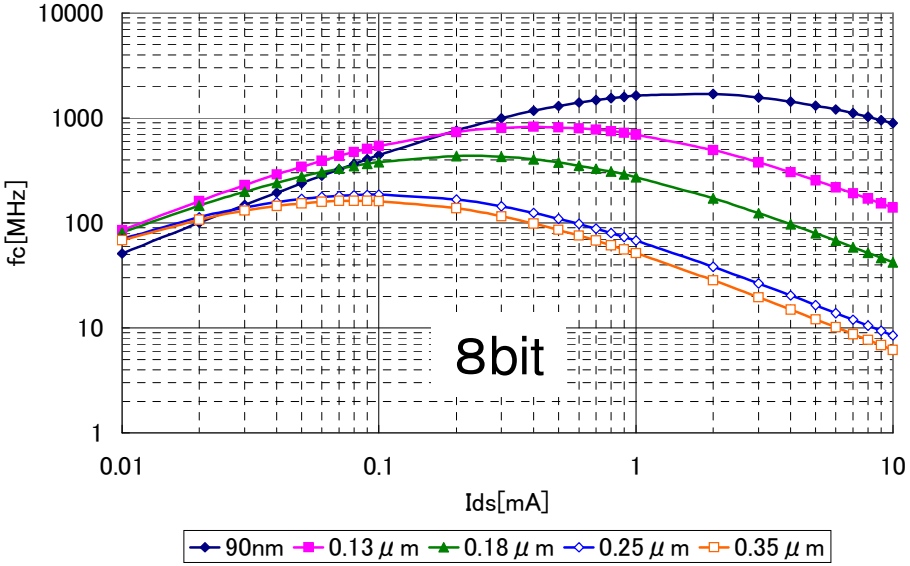
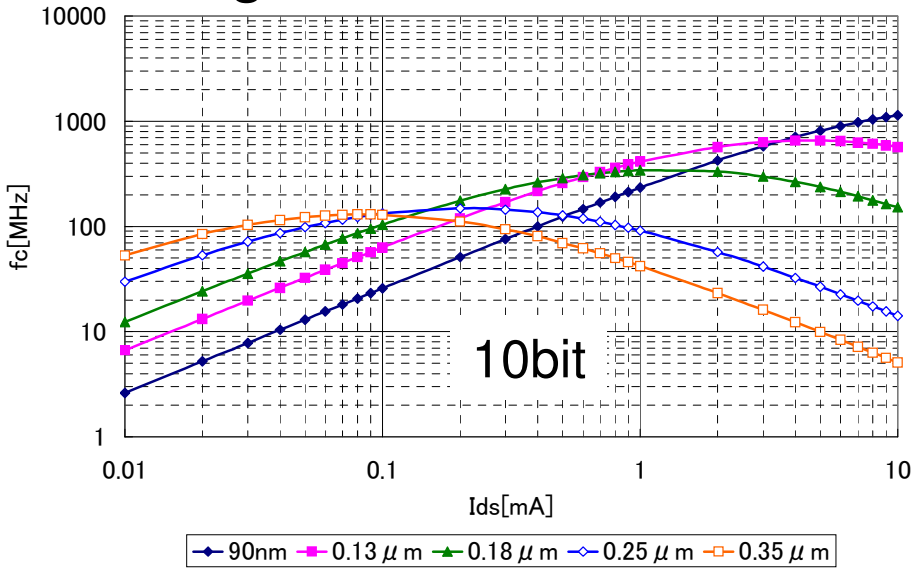
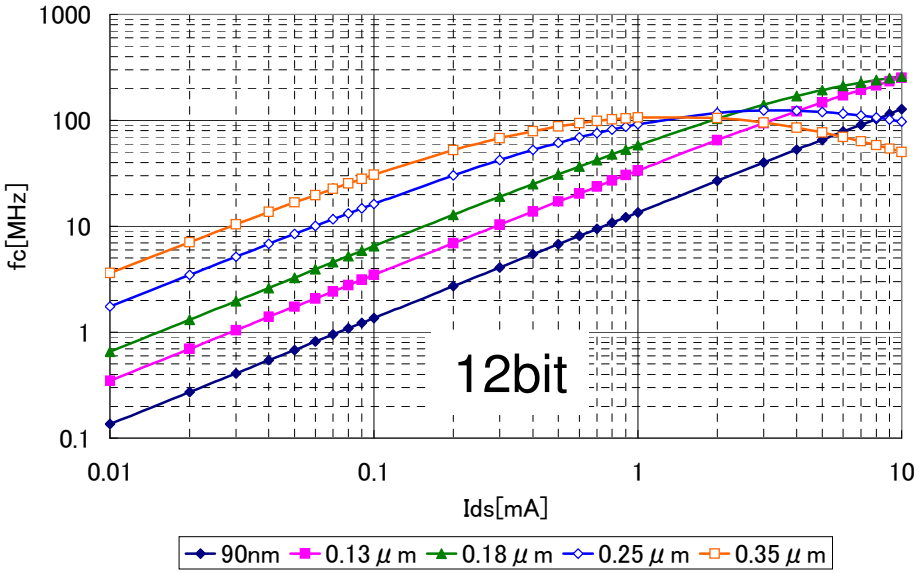
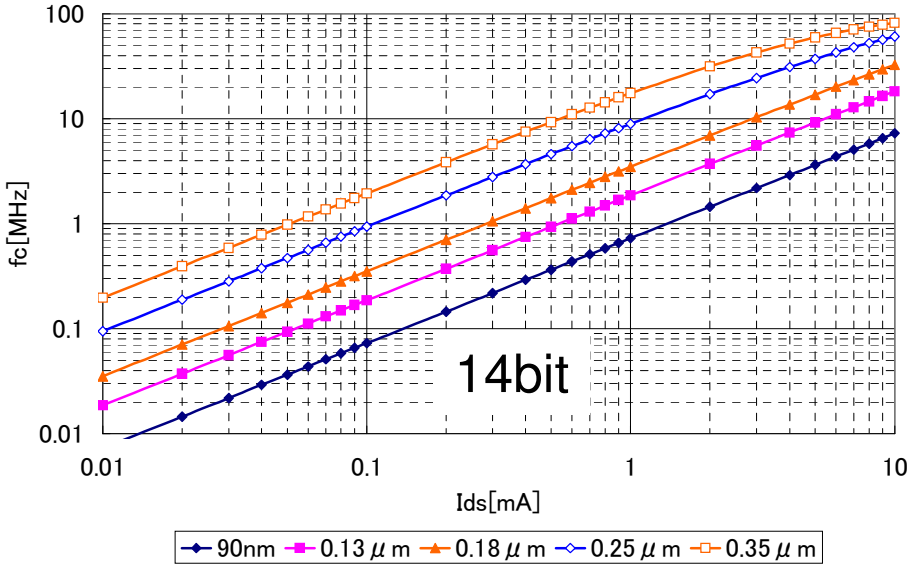
Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.









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Optimization of OpAmp in Pipelined ADC

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90nm CMOS, near sub-threshold operation, and SC level-shift have realized 10bit 80MHz ADC with 0.8V operation and small power of 6.5mW

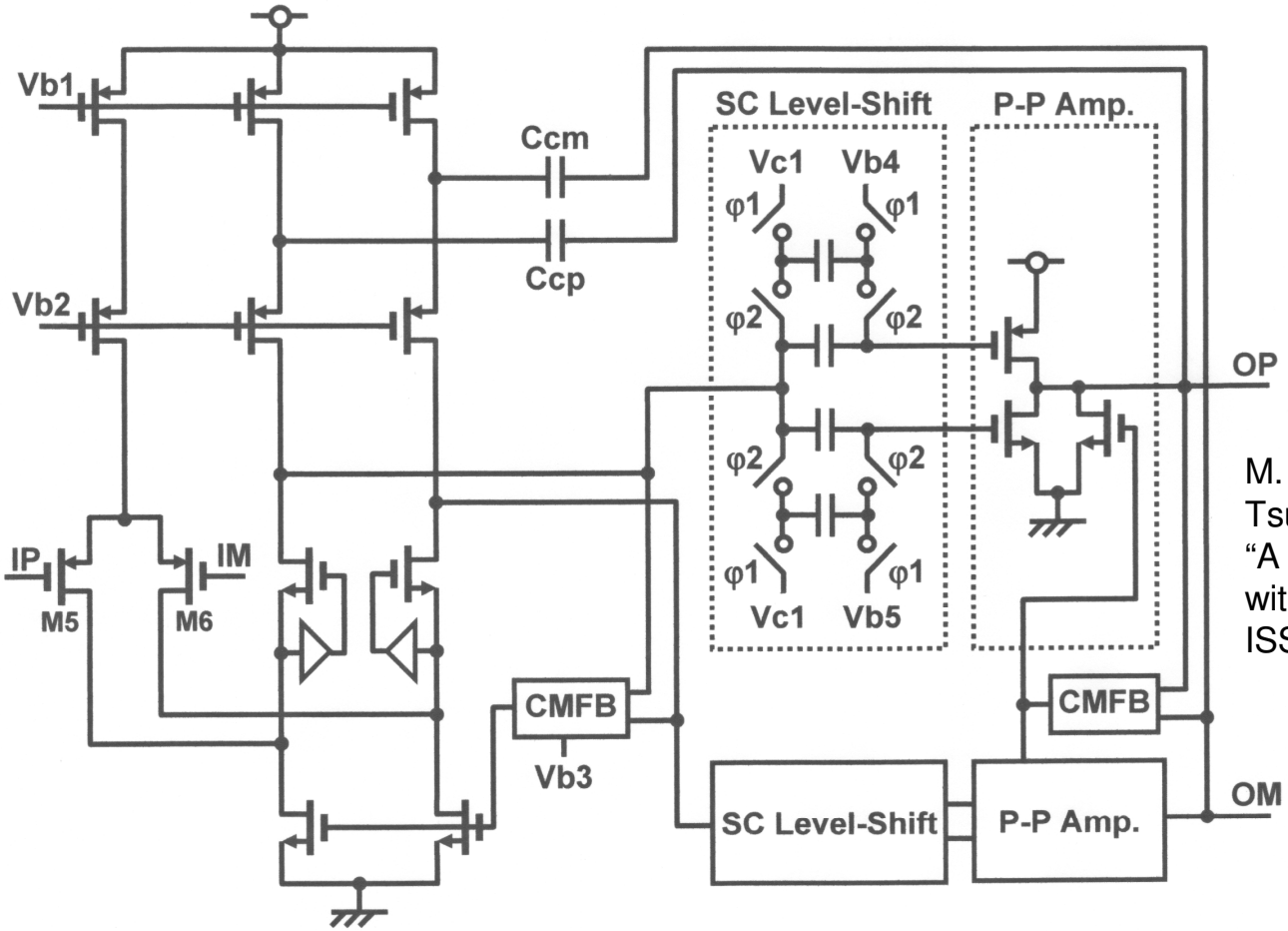

Figure 25.1.2: Schematic of two-stage amplifier.

M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto
"A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing," ISSCC, Dig. Tech. paper, pp. 452-453, 2007.

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Results

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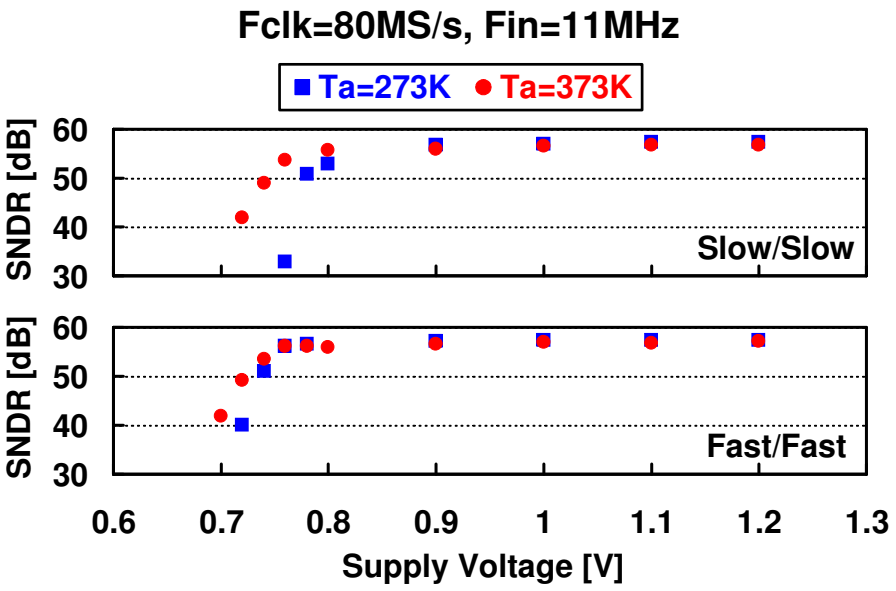
FoM=0.2pJ/step 0.08mW/MHz

Technology	1P10M 90nm CMOS with MIM Capacitors	
Resolution	10bit	
Conversion Rate	80MS/s	
Active Area	1.18mm x 0.54mm	
Input Range	1.2Vp-p Differential	
Supply Voltage	0.8V	1.2V
SNDR	55.0dB @2MHz 51.4dB @41MHz	56.9dB @2MHz 55.6dB @41MHz
Total Power Consumption	6.5mW	13.3mW
INL	< 1.0LSB	< 0.5LSB
DNL	< 0.8LSB	< 0.4LSB



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Optimization of V_{eff}

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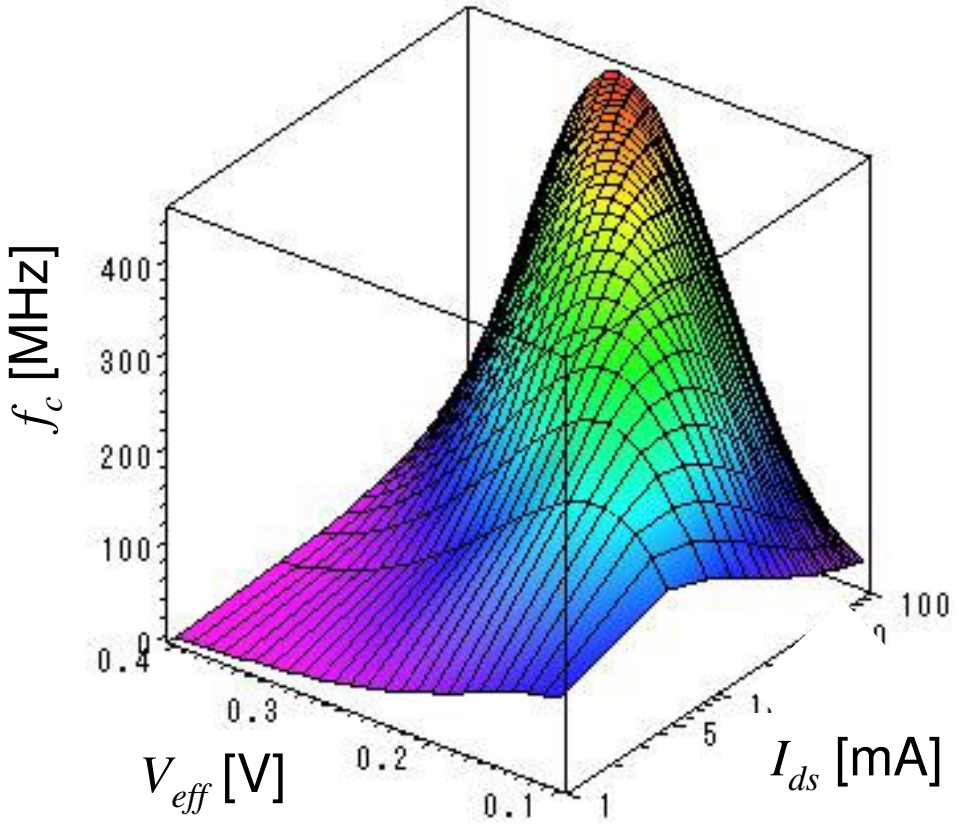
Optimum V_{eff} is a function of resolution, current, and design rule.

The lower V_{eff} is recommended for scaled CMOS technology.

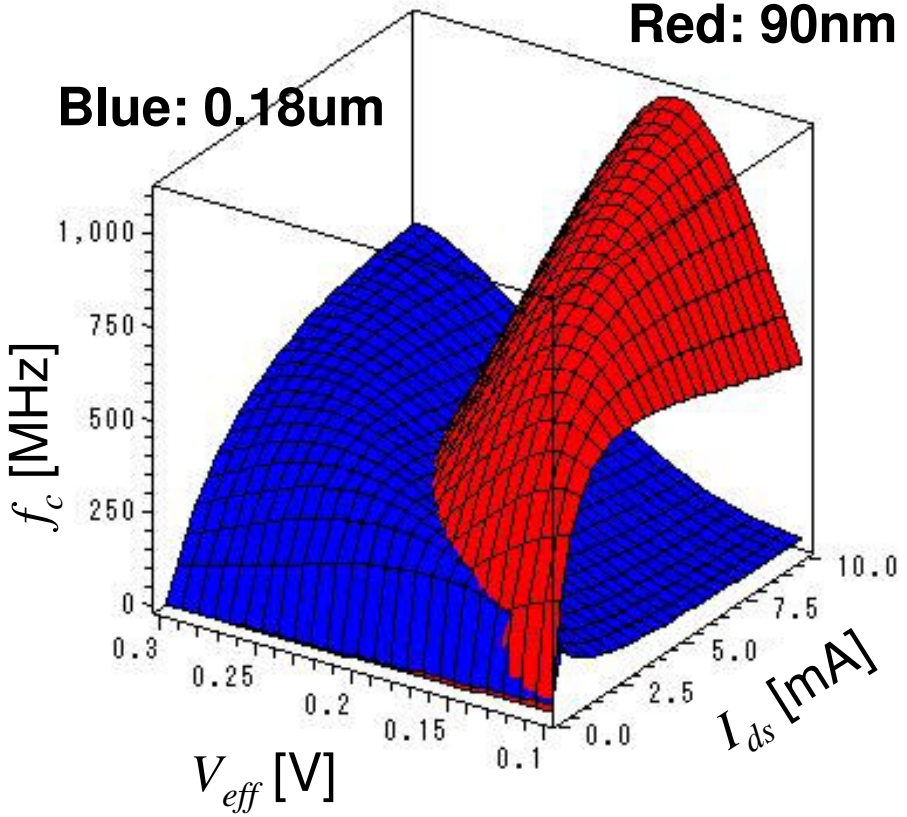
12 bit, 0.18um CMOS



10 bit

Red: 90nm

Blue: 0.18um



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Challenge to realize pipelined ADC without OpAmp

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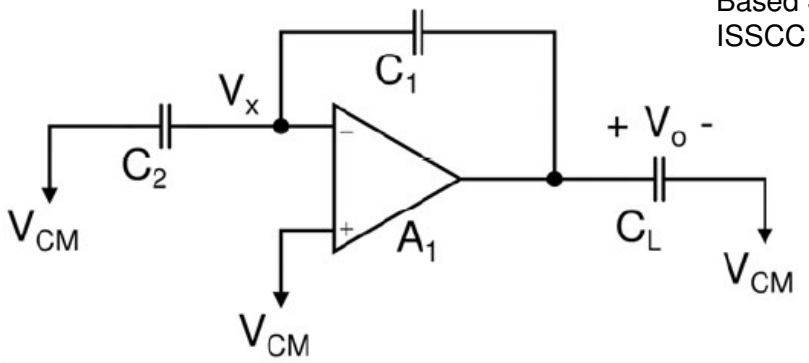
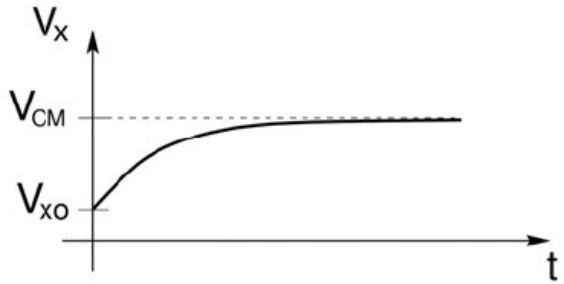
Comparator controlled current source can realize the virtual ground.

Now challenge for not use of OpAmp in ADC design has started.

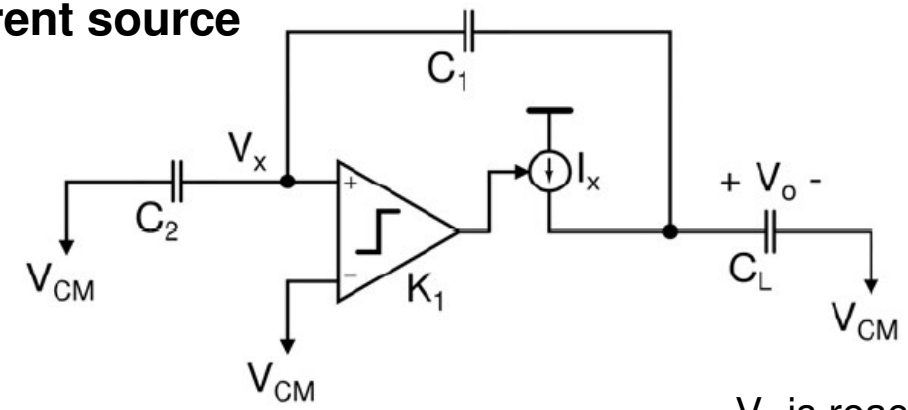
Conventional OpAmp



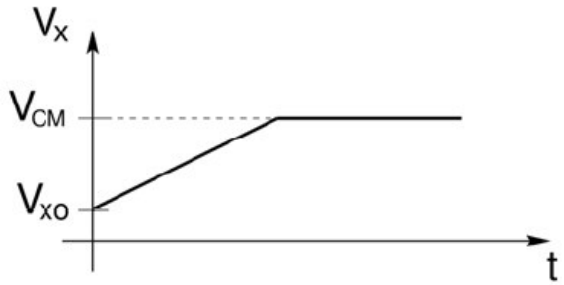
T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H. Lee, "Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.



Comparator controlled current source



V_x is reaching the virtual ground voltage asymptotically



V_x is reaching the virtual ground voltage with constant rate

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Realistic comparator controlled current source

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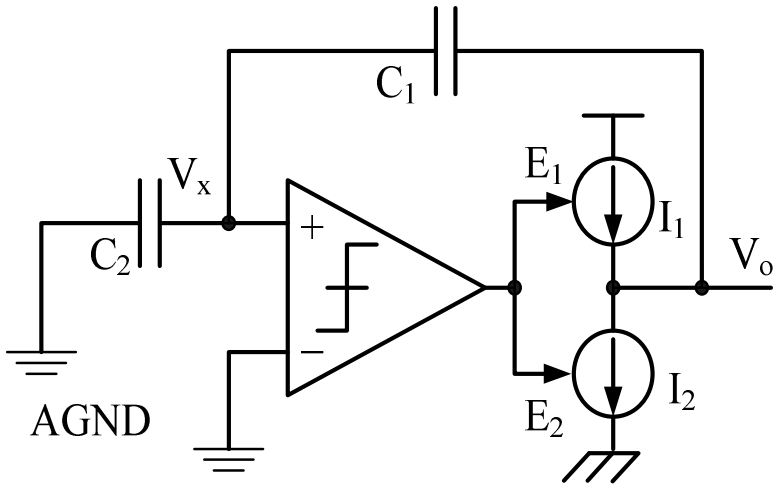
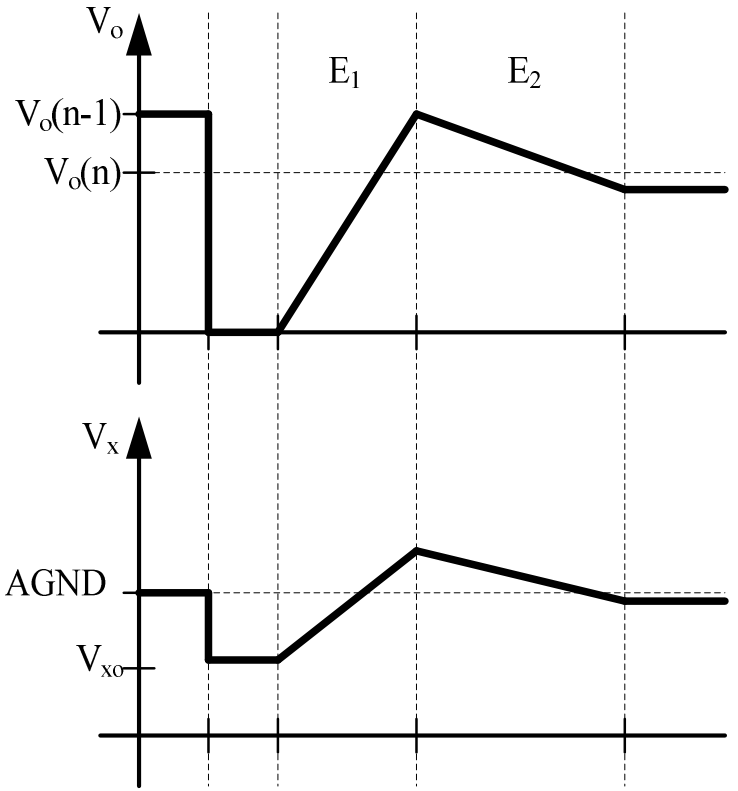
Time delay ($V_x \rightarrow V_o$) causes voltage offset. Small inverse current source has been introduced. The offset voltage can be reduced and does not effect the conversion linearity.



$I_2 << I_1$



T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H. Lee, "Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.

10b, 8MHz ADC has been developed. Pd=2.5mW. Lowest Pd/MHz

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Results

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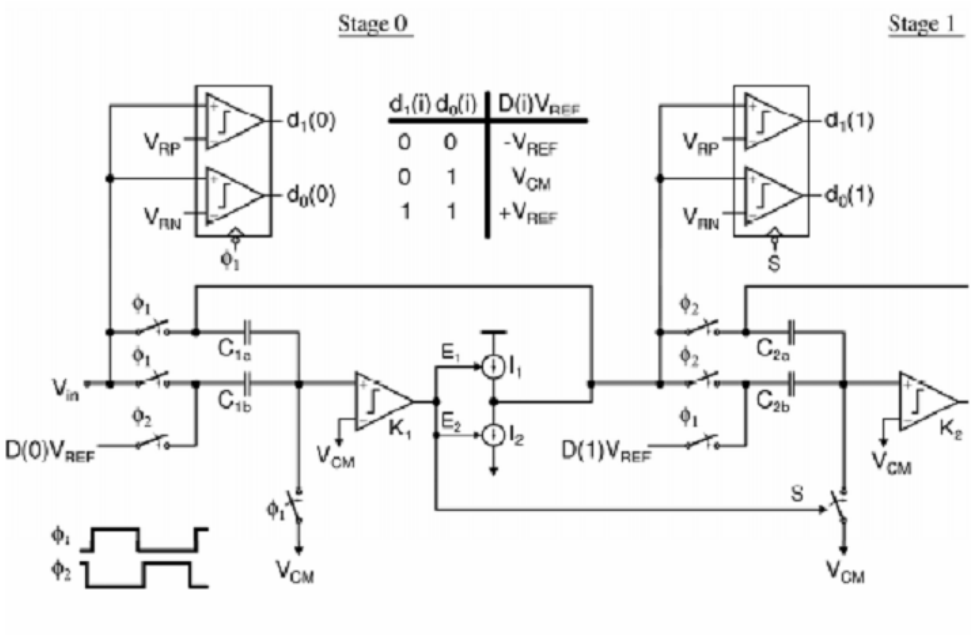
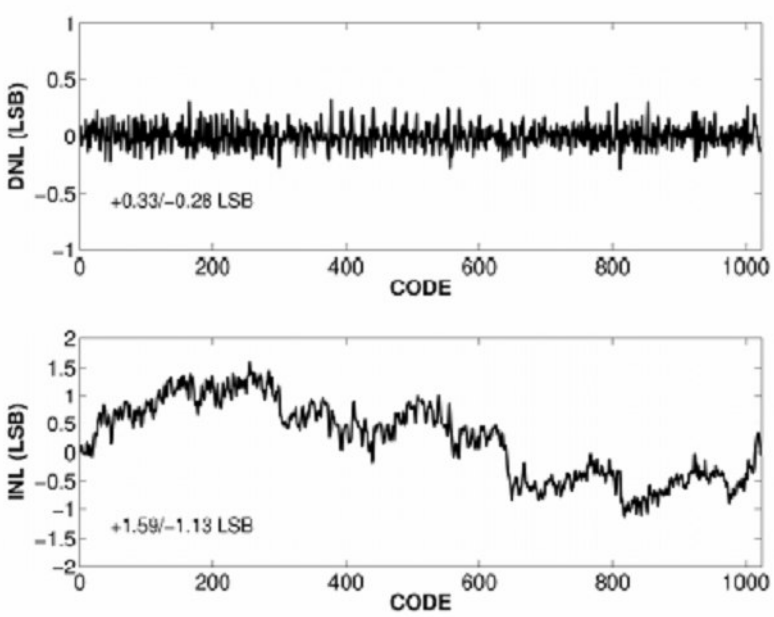
Small FoM, however not amazingly

10b ADC **FoM =0.3pJ/step, 0.3mW/MHz**





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Sub-ranging ADC

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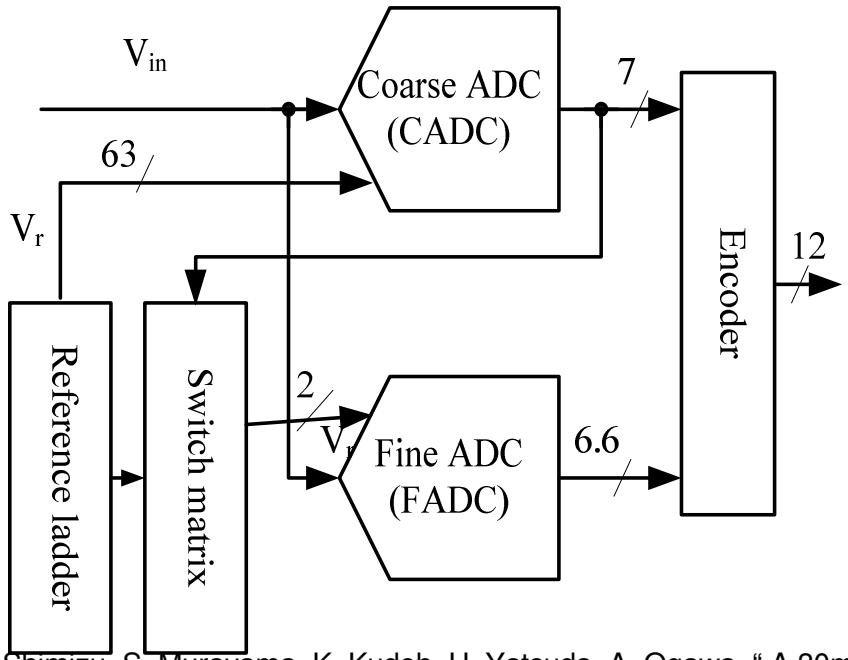
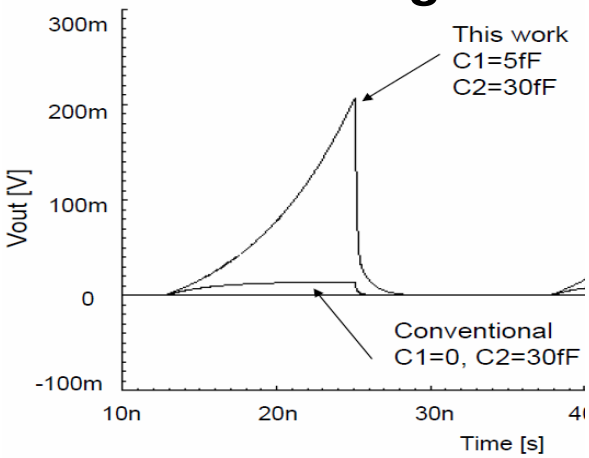
Sub-ranging ADC also doesn't require OpAmp and suitable for LV operation. However it requires low offset voltage comparators.

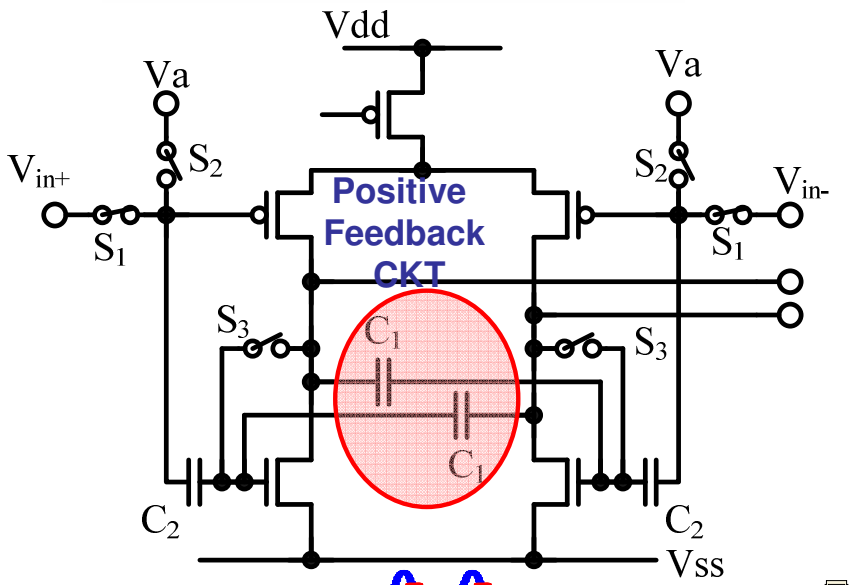
Use of positive feedback technique has realized low offset voltage.

Technology revival has been found.

Pd/MHz =0.75mW/MHz which is lowest value!!







7]Y. Shimizu, S. Murayama, K. Kudoh, H. Yatsuda, A. Ogawa, " A 30mw 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 222-225. Feb. 2006.

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Results

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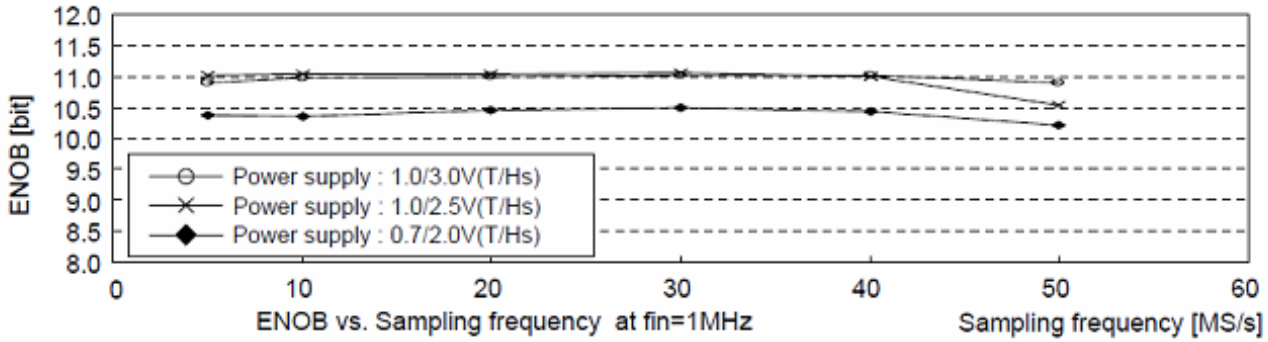
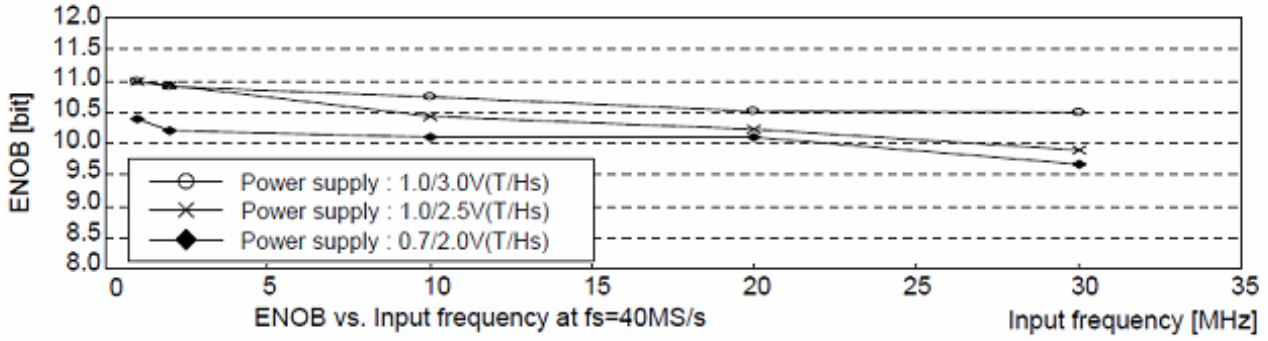
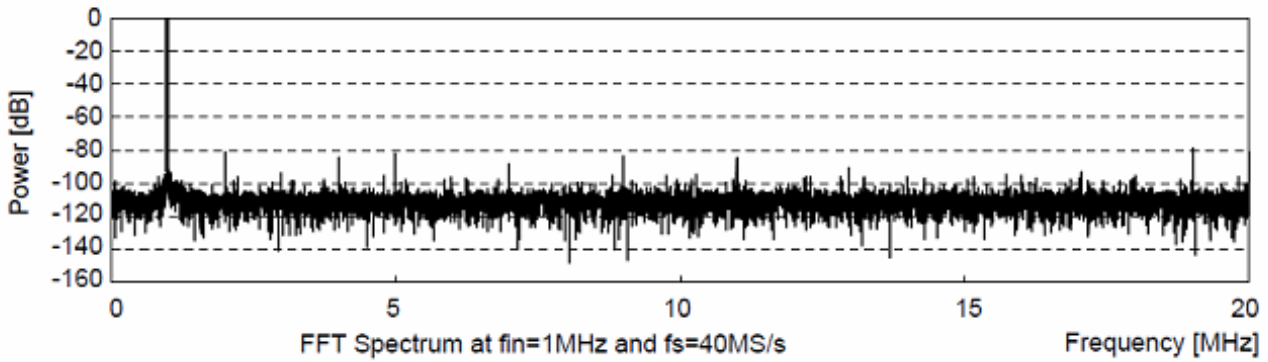
Attain high ENOB of 10.5-11.0
30mW at 40MHz

90nm CMOS 1V Operation

0.4pJ/step







Successive approximation ADC

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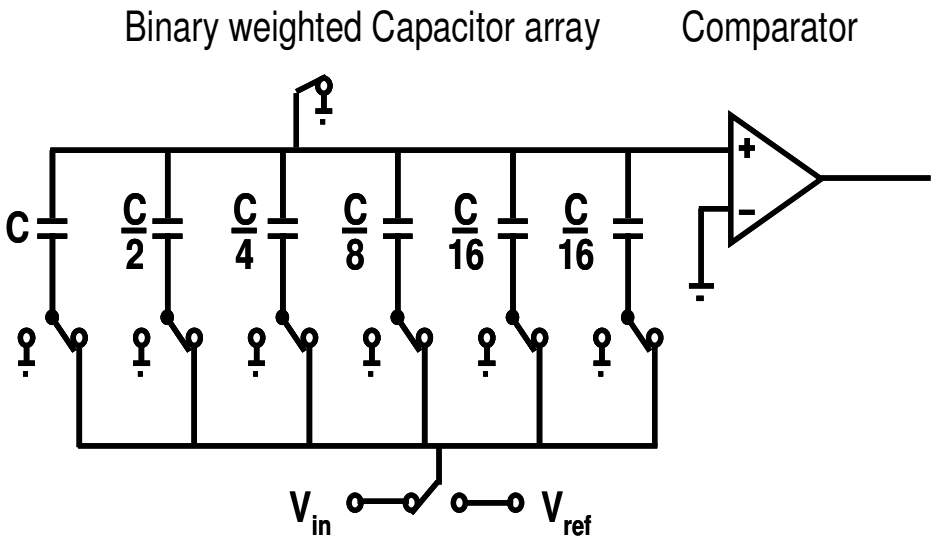
Successive approximation ADC has been used long time as a low power and low speed ADC. It doesn't require OpAmp but capacitor array and comparator. Thus this architecture looks suitable for scaled and low voltage CMOS.

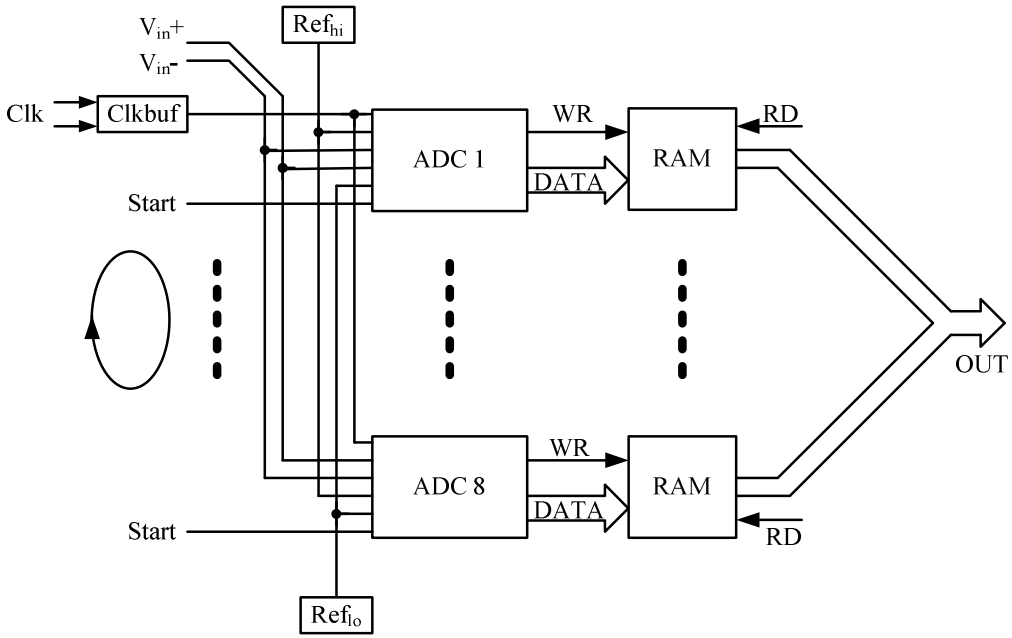
Now challenge for renewal of this conventional architecture has started.

Successive approximation ADC

SA-ADC



Eight interleaved SA-ADCs with 90nm CMOS attain 600MHz operation.



D. Draxelmayr, "A 6b 600MHz 10mW ADC Array in Digital 90nm CMOS," IEEE, ISSCC 2004, Dig. of Tech. Papers, pp. 264-265, Feb. 2004.

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Improvement of SA-ADC

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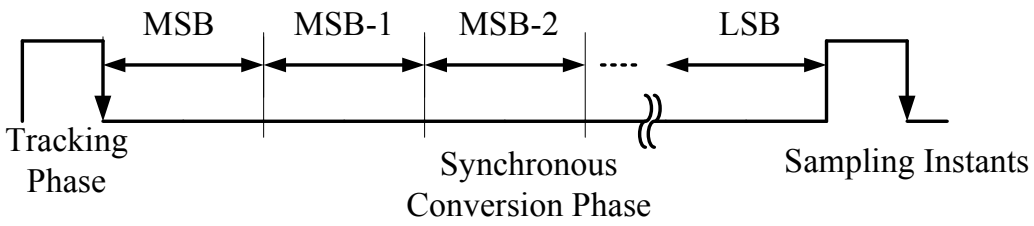
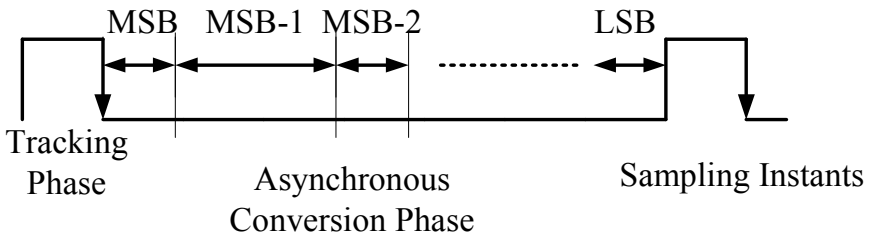
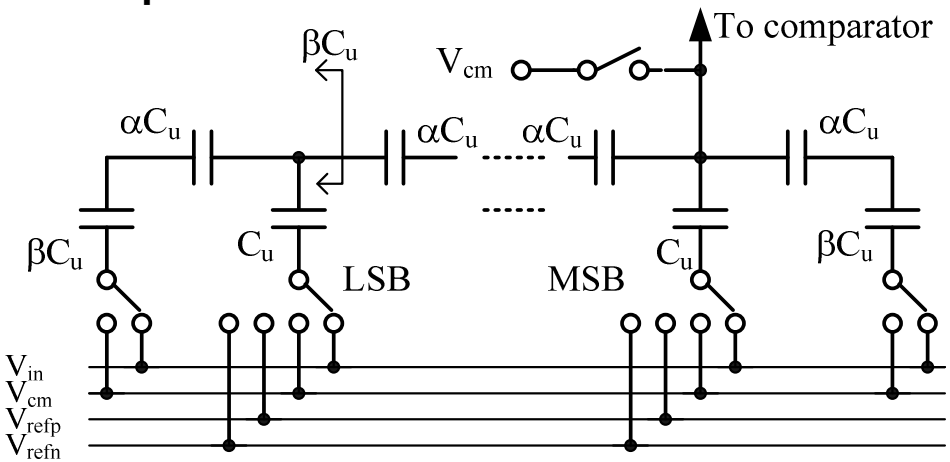
Asynchronous clock increases conversion frequency.
Use of proper radix reduces capacitance.

Asynchronous clock





Capacitor ladder with some radix number



6bit 600MHz 5.3mW ADC has been realized with 0.13um CMOS

$$\beta = 1 + \alpha \| \beta$$

$$radix = 1 + \frac{\beta}{\alpha}$$

S. W. M. Chen and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13um CMOS," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.

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Newest SAR ADC

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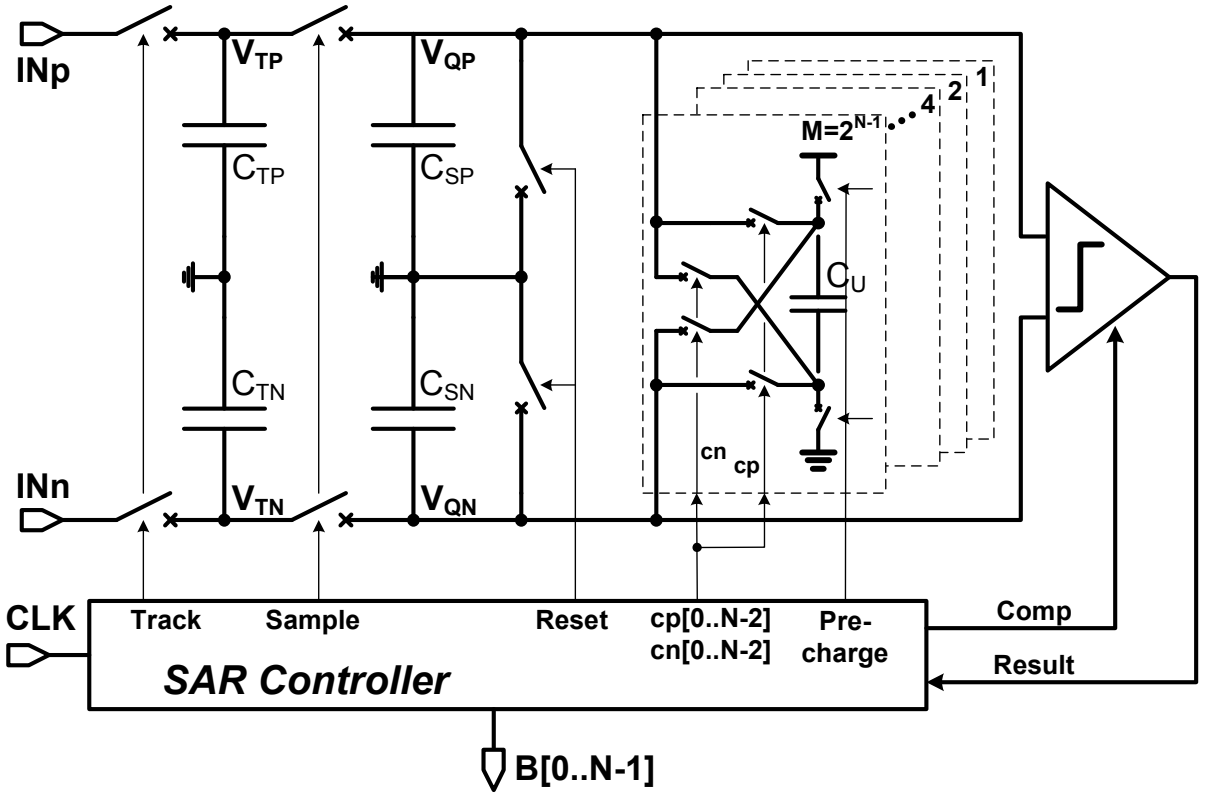
SAR ADC must be one of the good solution for scaled analog technology.
No OPamp is needed.

No static power consumption.
Higher signal swing and small capacitance



$$Q_{REF} = \sum_i 2^i C_U \cdot V_{DD}$$

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

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Analog operation with capacitances

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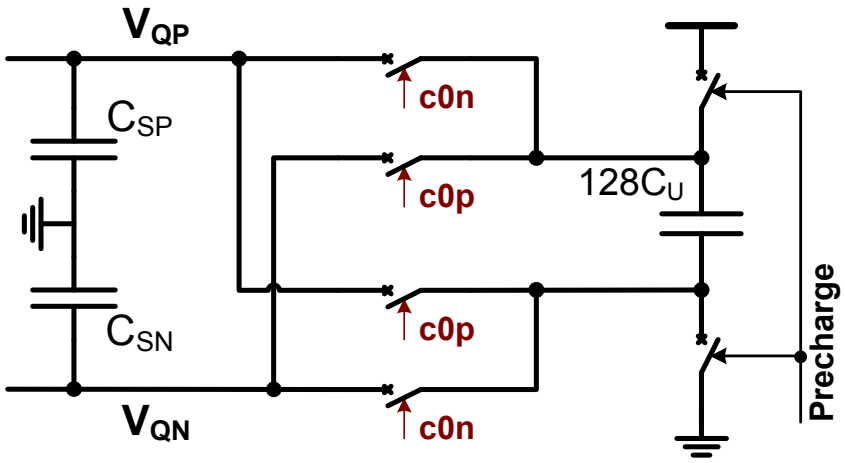
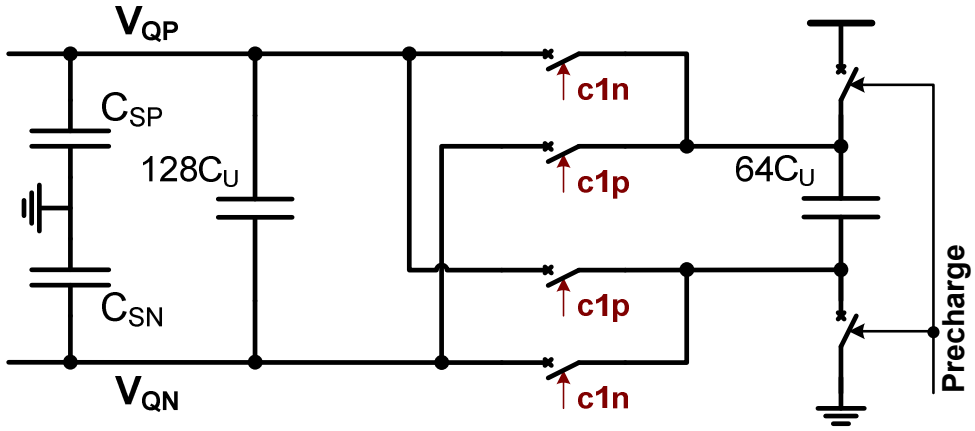
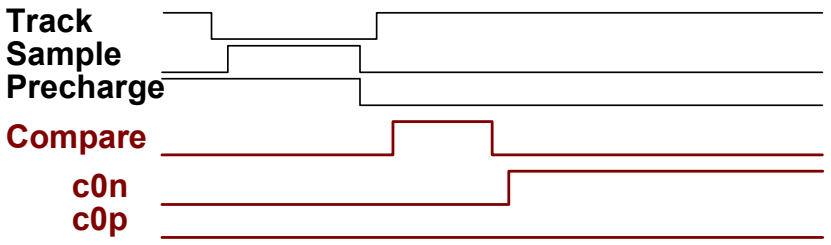
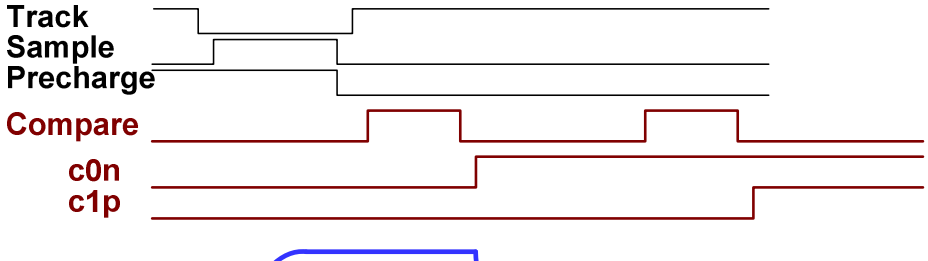
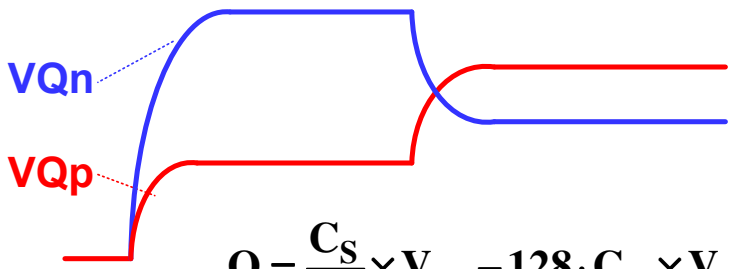
Capacitances can realize analog operation for SAR ADC.
No static current is required and higher signal swing can be used.



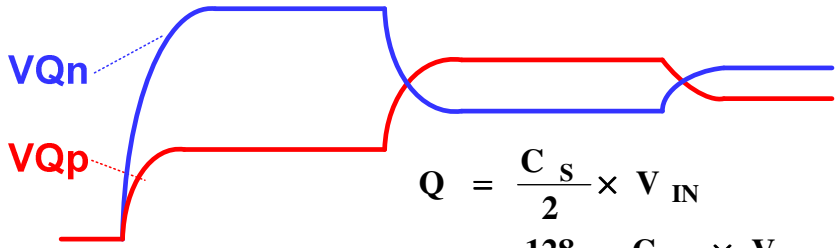








$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD}$$



$$Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD} + 64 \cdot C_U \times V_{DD} \pm \ldots$$

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Results

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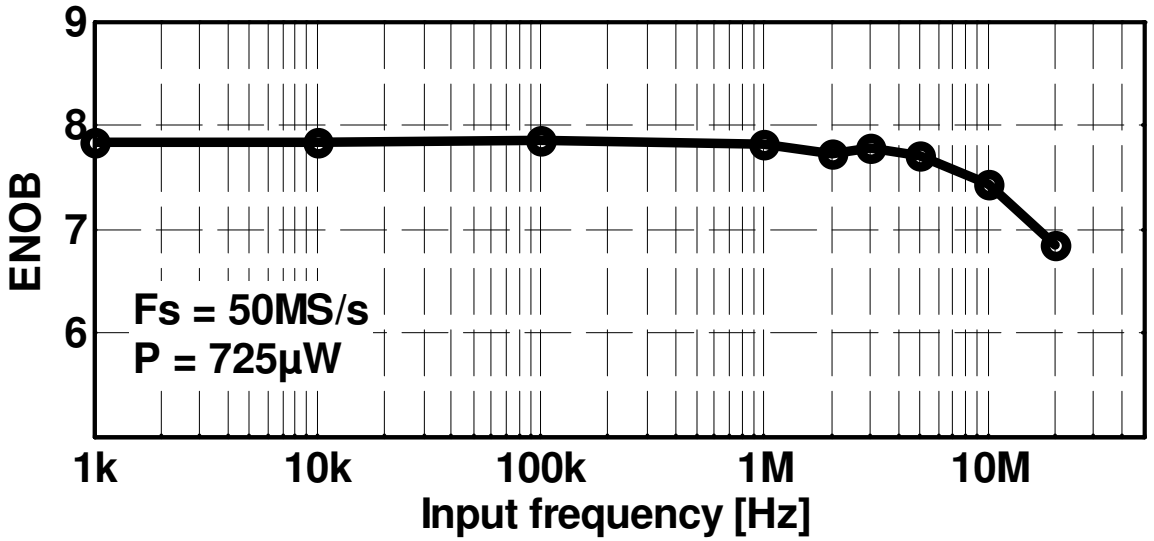
Amazing small FoM=65fJ/step has been attained.



8bit, 0.3mW at 20MHz

J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

ISSCC06 Paper #	Arch.	Fs [MS/s]	ENOB	P [mW]	FoM [fJ]	FoM includes		
						Ref.	Clock	Dec.
3.1	CTΔΣ	40	12	50	300	-	Yes	Yes
3.4	ΔΣ	4.4	12.6	13.8	500	-	No	No
12.1	PL	100	9.4	39	570	-	-	-
12.3	Subr.	50	10.4	30	440	-	-	-
12.4	PL−CBSC	7.9	8.7	2.5	760	-	-	-
12.5	SAR	0.1	10.5	0.025	170	No	No	-
12.7	PL	50	9.2	15	510	-	-	-
31.1	Flash	1250	3.7	2.5	160	-	-	-
31.5	SAR	300	5.3	2.65	220	No	Yes	-
This work	**CS−SAR**	**20**	**7.8**	**0.29**	**65**	**Yes**	**Yes**	-

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High resolution and high speed SAR ADC

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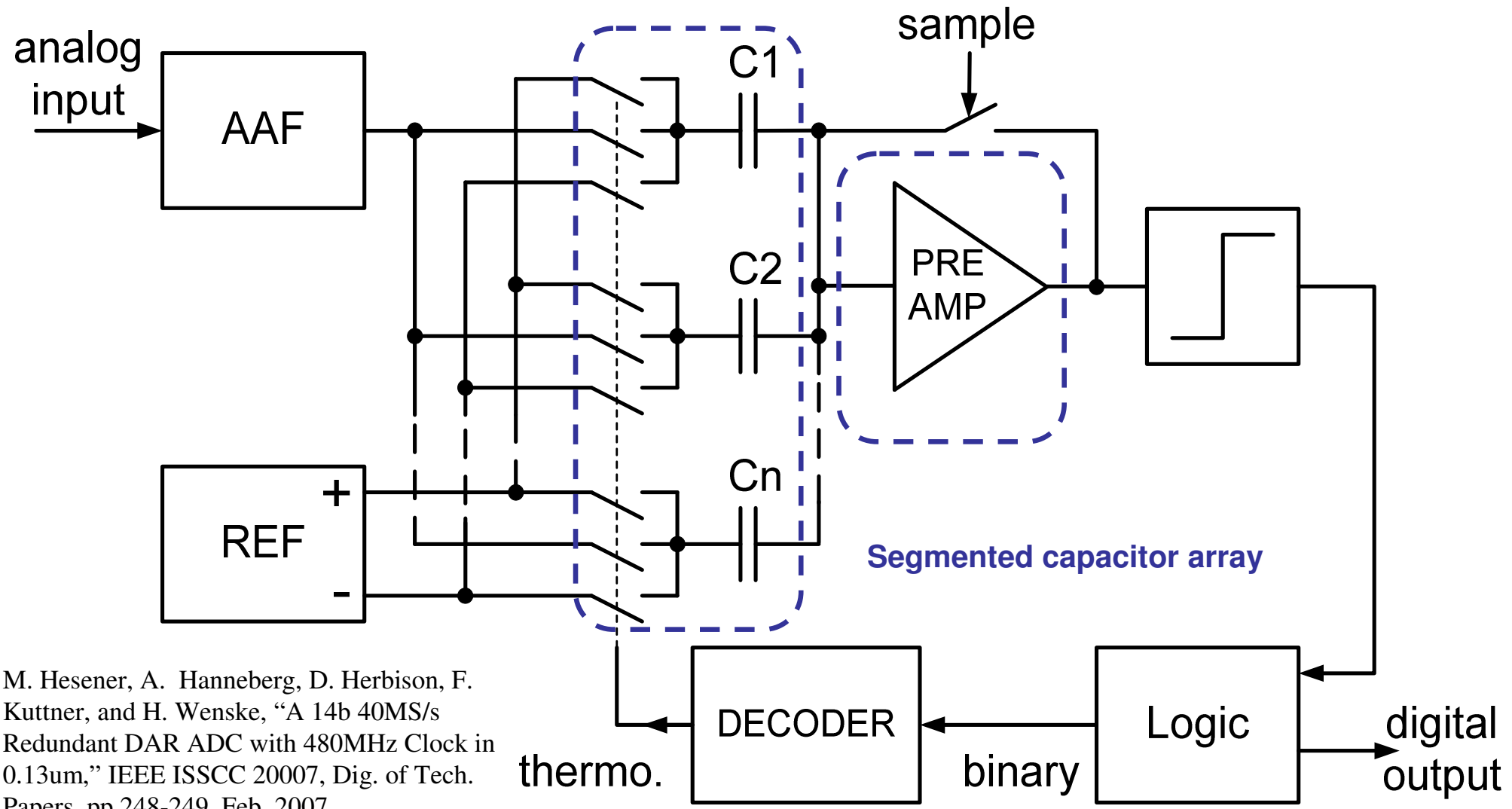
To increase the resolution, a pre-amplifier is located in front of a comparator



M. Hesener, A. Hanneberg, D. Herbison, F. Kuttner, and H. Wenske, "A 14b 40MS/s Redundant DAR ADC with 480MHz Clock in 0.13um," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.248-249, Feb. 2007.

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Results

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High conversion rate of 40MS/s and low power of 66mW have been attained

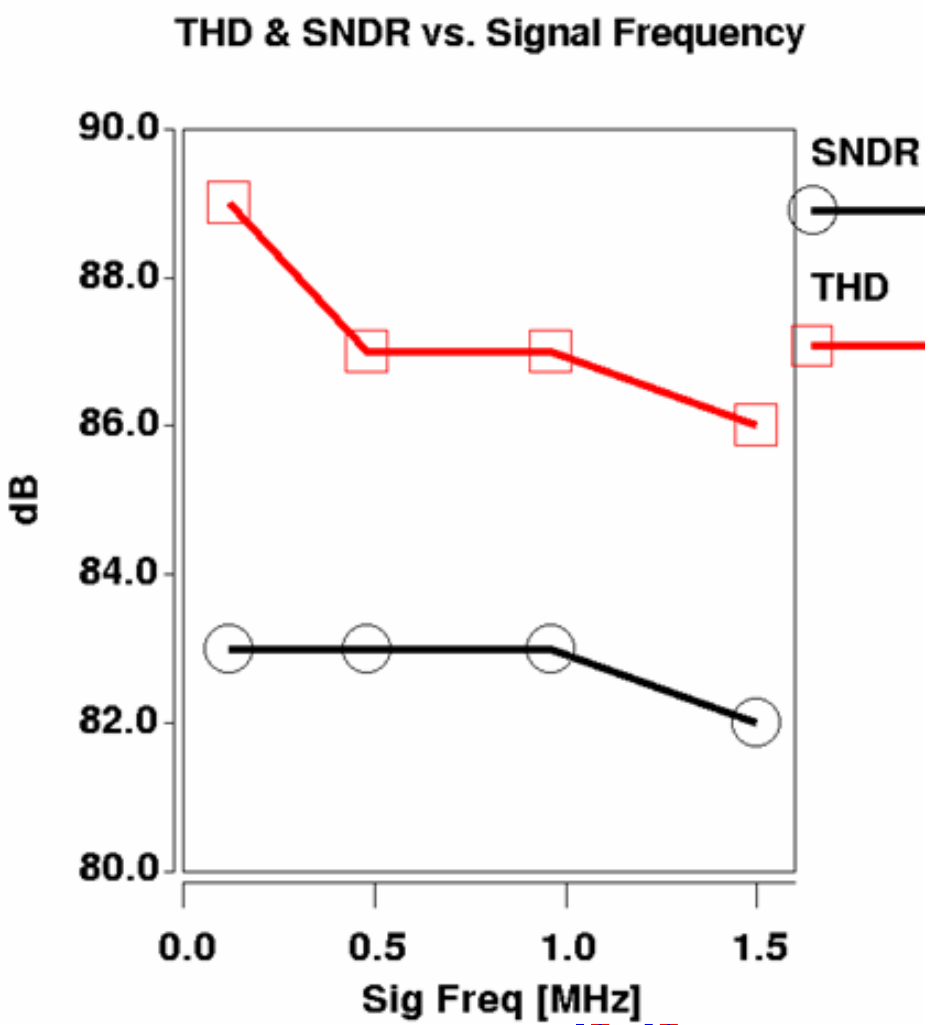
High ENOB of 13.5bit has been attained

High

FoM=0.14pJ/step

0.13um CMOS

Supply voltage	1.5V
Input range	±0.9V diff.
Sample frequency	40MHz
Internal clock frequency	480MHz
Analog power	49mW
Digital power	17mW
Total power	66mW



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Delta-sigma ADC

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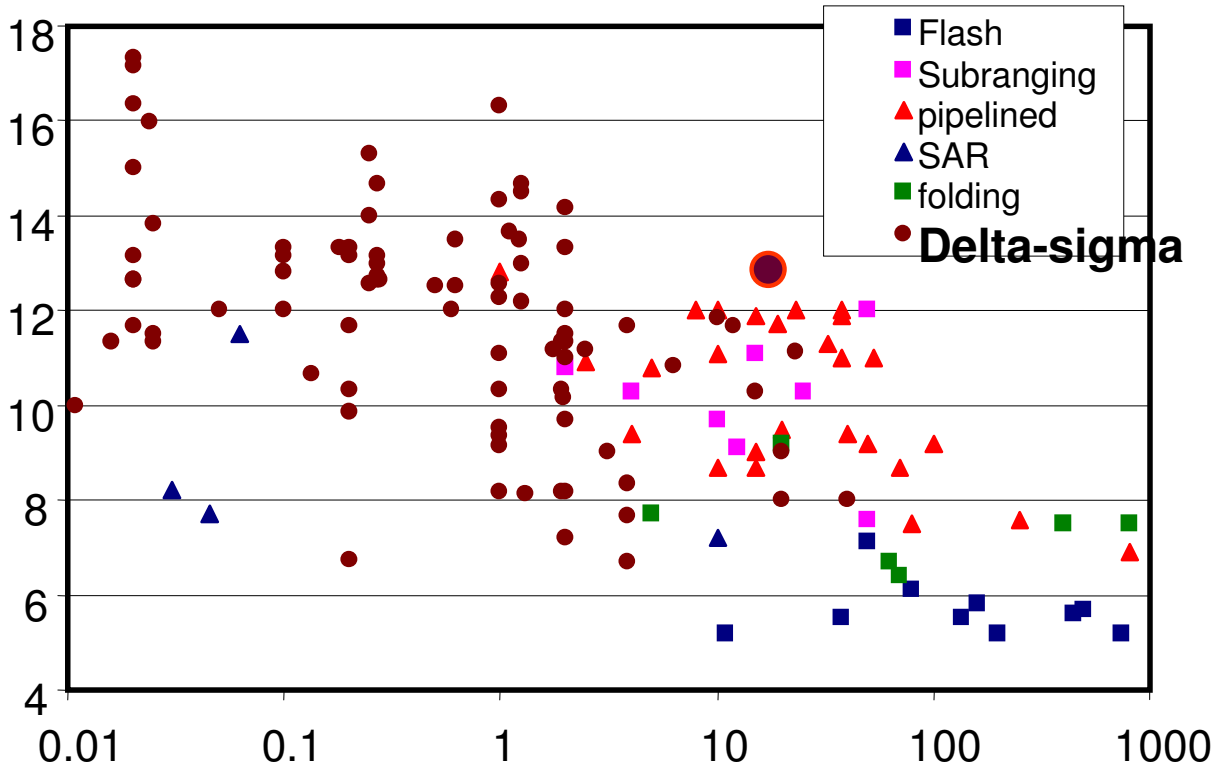
In delta-sigma ADC, higher operating frequency can increase SNR. For higher resolution ADC, the delta-sigma method must be vital.

Nyquist ADC:

$$SNR \propto CV_{sig}^2$$

Delta-sigma ADC:

$$SNR \propto CV_{sig}^2 \cdot M^{\alpha}$$



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Wide-band delta-sigma ADC

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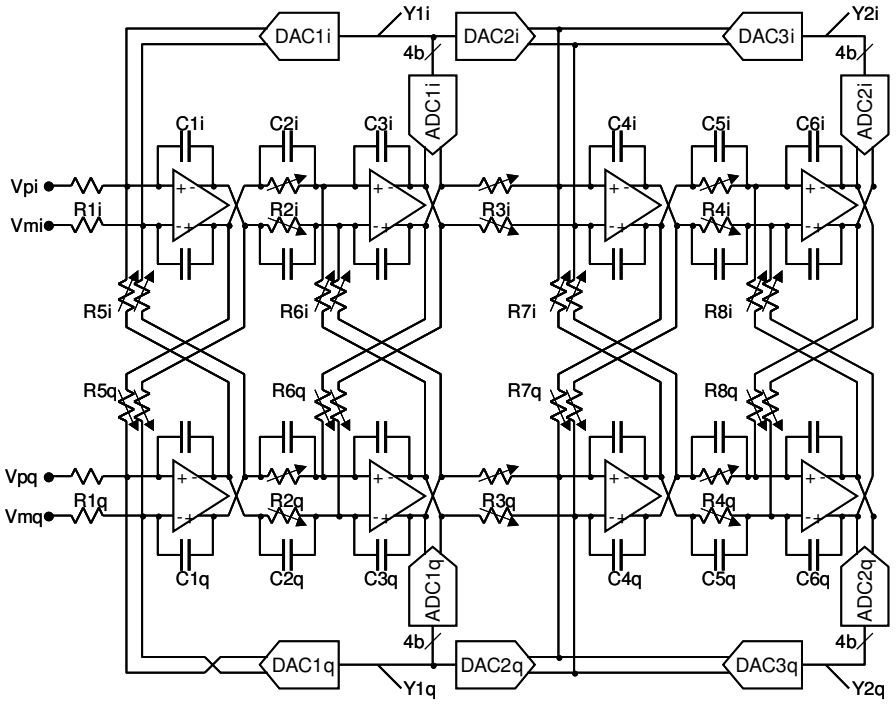
Delta sigma ADCs have emerged as a strong rival to high resolution nyquist ADCs

90nm CMOS、BW=20MHz, DR(=SNR)=77dB, 50mmW, FoM=200fJ/conv.

L. J. Breems, et., al.
"A 56mW CT Quadrature Cascaded SD Modulator with 77dB in a Near aero-IF 20MHz Band.
ISSCC 2007, pp. 238-239.



Technology	90nm CMOS, 1P6M
Supply voltage	1.2V
Architecture	CT quadrature cascaded ΣΔ modulator (2-2, 4b)
Sampling frequency	340MHz
Bandwidth	20MHz @ 10.5MHz IF
Max. input voltage	1Vp (differential)
Dynamic range*	77dB (97dB @ 200kHz, 115dB @ 3kHz)
Peak SNR / SNDR*	71dB / 69dB
Image rejection	>55dB (for -1MHz input tone)
Active chip area	0.5mm^2
Power consumption	50mW (analog), 6mW (digital)
Figure-of-merit (FOM)	0.2pJ/conv. (FOM=P/(2^enob*2*BW))

(*1MHz input signal, signal bandwidth is 20MHz)

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Summary

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- **Technology issues due to technology scaling**
  - **Low voltage operation → small headroom**
  - **Reducing voltage gain**
  - **Small voltage swing → larger signal capacitance**
  - **Difficult to realize high resolution ADCs**

- **Design challenges of ADCs**
  - **Pipelined ADC**
    - **Optimization of OpAmp**
    - **Comparator controlled current source**
  - **Revival of ADC architectures**
    --- No use of OpAmps ----
    - **Sub-ranging ADC**
    - **SAR ADC**
  - **Delta-sigma ADC is increasing signal bandwidth**