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Compensation techniques for integrated analog device issues

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- Integrated analog devices
- V_T mismatch compensations
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  - Comparator
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- Mismatch and absolute value compensations in circuits
  - I/Q imbalance and image rejection
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Integrated analog devices

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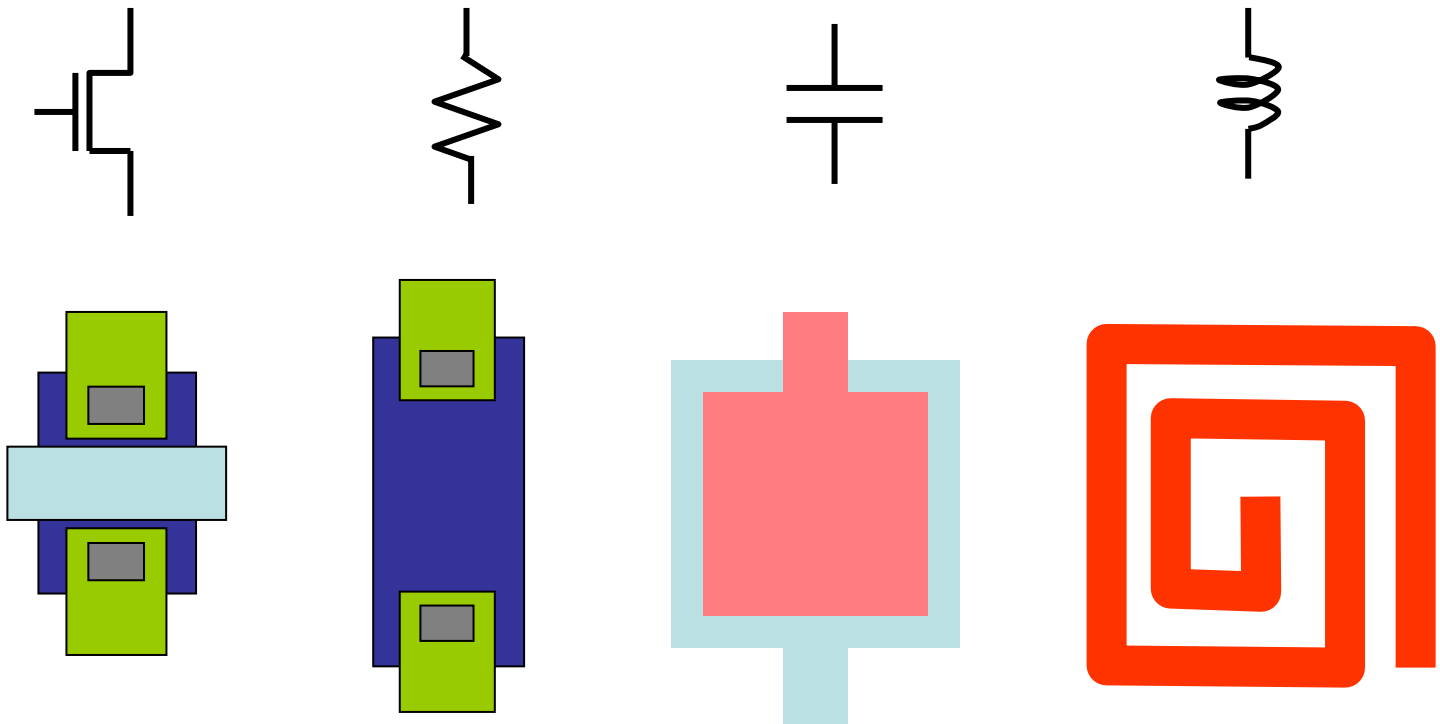
Analog circuits need many passive devices, as well as transistors

MOS Transistor **Resistor** **Capacitor** **Inductor**



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Characteristics of passive devices

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Passive components has some imperfections

	Diffusion Resistance	Poly Resistance	Poly to Poly Capacitance	Gate Capacitance	MIM Capacitance
Sheet R or C	20-100 ohm	20-100 ohm	0.5-2 fF/um^2	2-5 fF/um^2	0.5-2 fF/um^2
Absolute accuracy (3sigma; %)	10	10	5-10	2-5	5-10
Relative accuracy (3sigma; %)	0.2-2	0.2-2	0.05-0.2	0.05-0.2	0.05-0.2
Temperature Coefficient (%/deg C)	0.05-0.2	0.1-0.2	0.002	0.002	0.001
Voltage Coefficient (%/V)	0.05-0.2	0.01-0.05	0.005	0.01	0.001
Comment	Large VC Leak	Low VC Low leak	Low VC Cost up	High VC	Good Q (RF) Cost up

V_T mismatch

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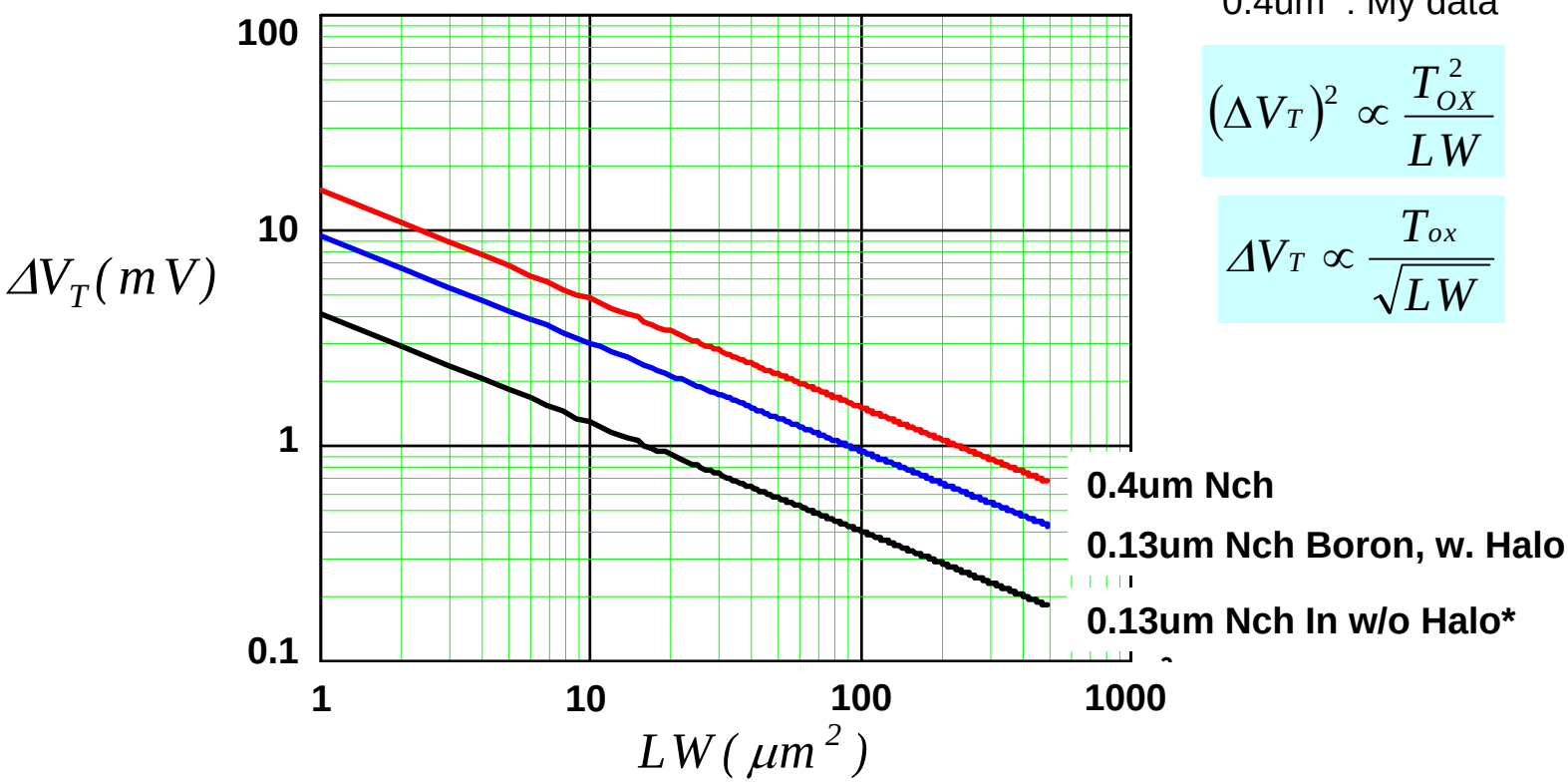
V_T mismatch causes offset voltage of an amplifier and a comparator.
Larger gate area is needed to reduce offset voltage,
however results in decrease of performances, such as BW and PD.

0.13um: Morifuji, et al., IEDM 2000
0.4um : My data

$$(\Delta V_T)^2 \propto \frac{T_{OX}^2}{LW}$$

$$\Delta V_T \propto \frac{T_{ox}}{\sqrt{LW}}$$



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V_T fluctuations in a wafer

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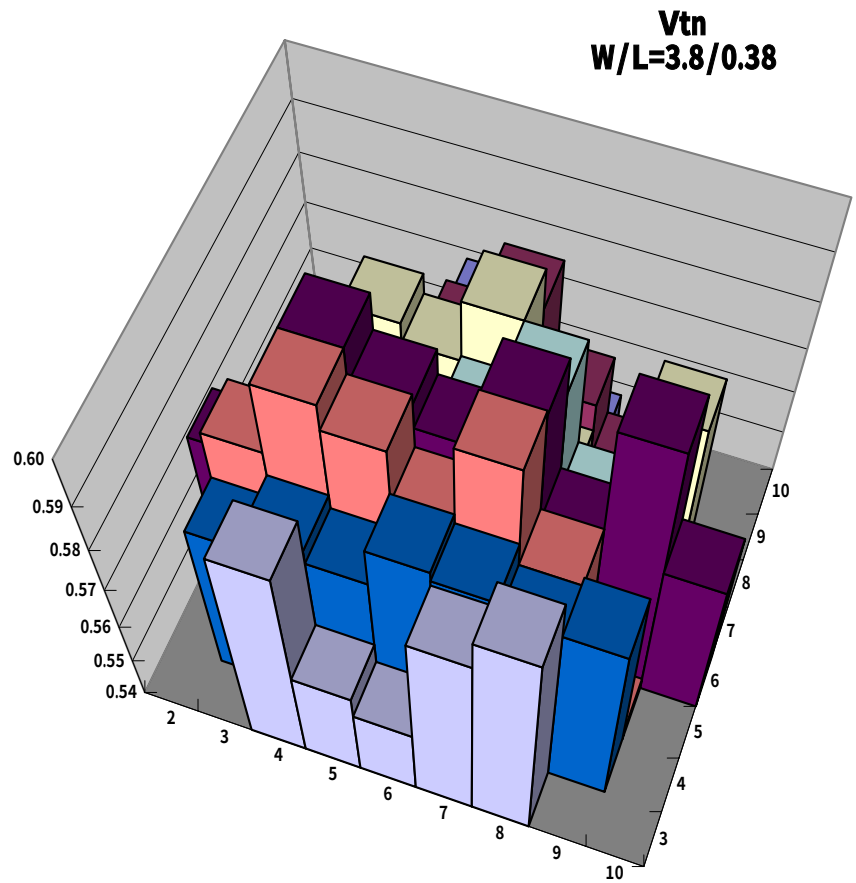
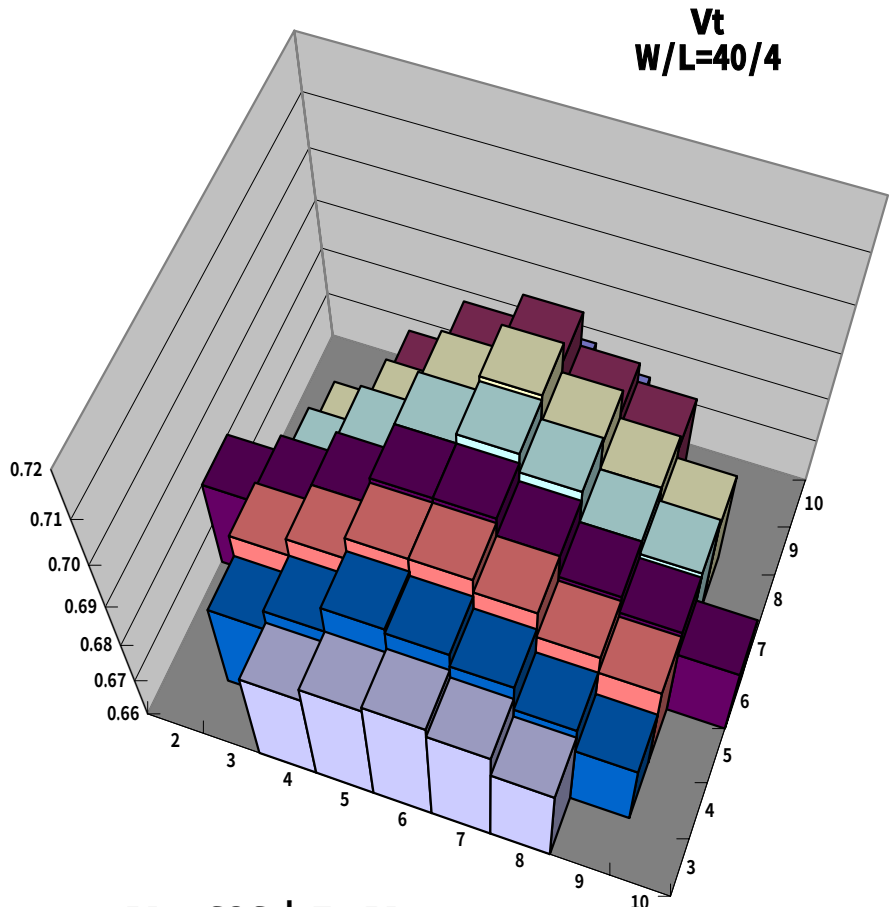
V_T fluctuation for small device looks random in a wafer.
V_T fluctuation for large device have some gradients in a wafer.



Vt =575±18mV



Vt =686±7mV

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Influence of V_T mismatch in current staring DAC

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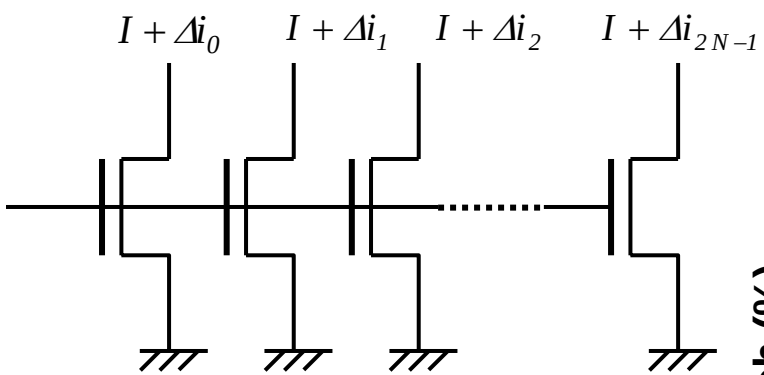
Higher resolution DAC requires smaller current mismatch which is mainly caused by V_T mismatch.



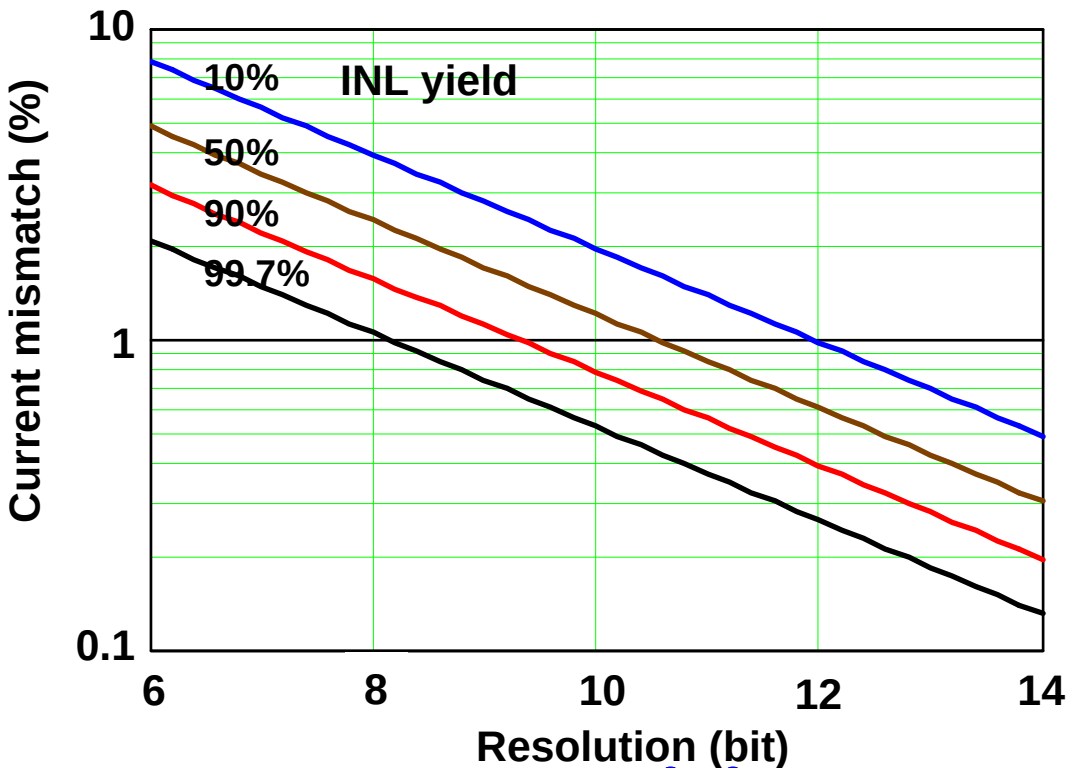
$$\frac{\sigma(I)}{I} \approx \frac{1}{2C\sqrt{2^N}}$$

N: resolution

C: Constant determined by INL

$$\left(\frac{\sigma(I)}{I}\right)^2 \propto \frac{1}{2^N}$$

Van den Bosch,.. Kluwer 2004



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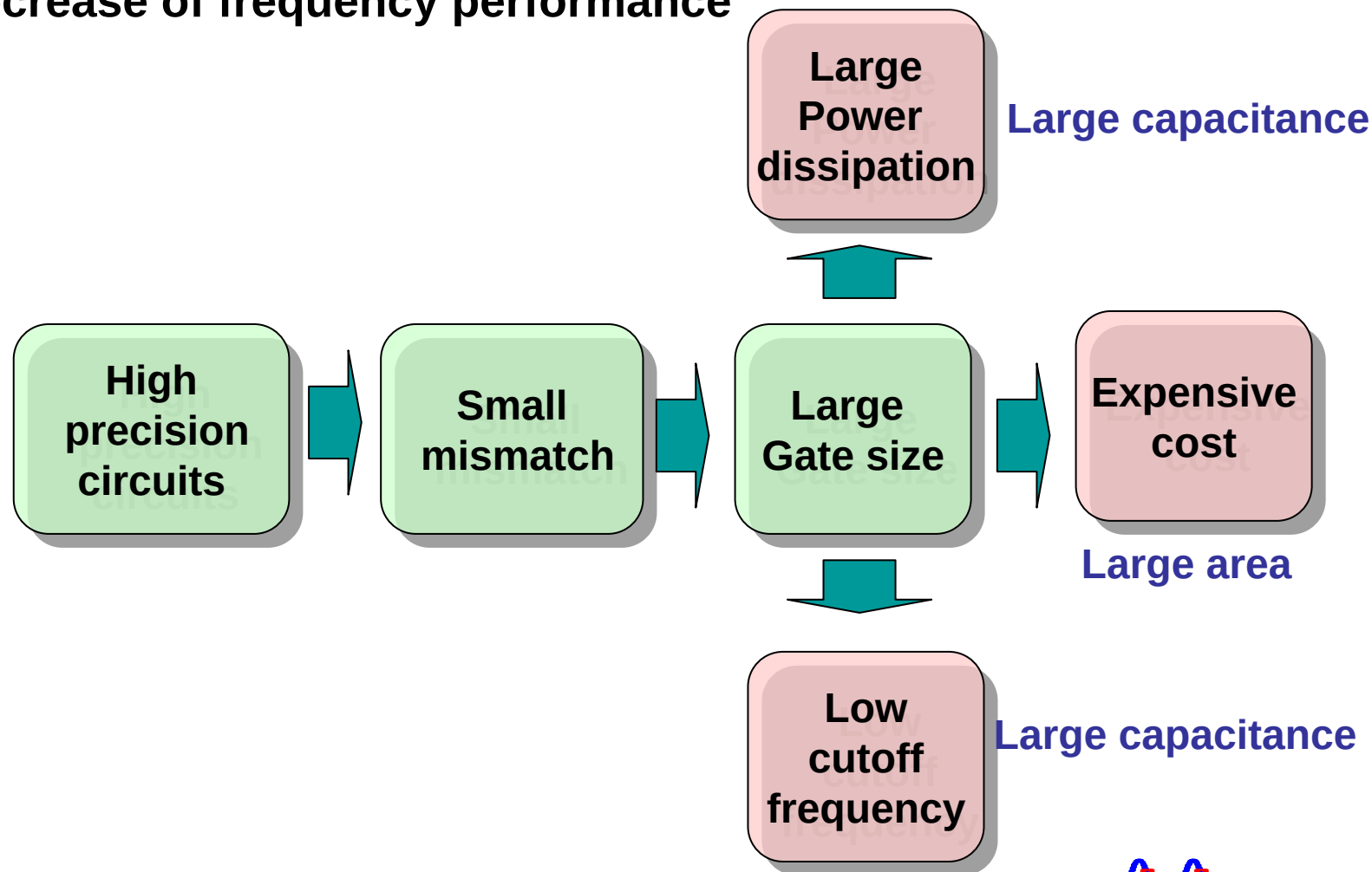
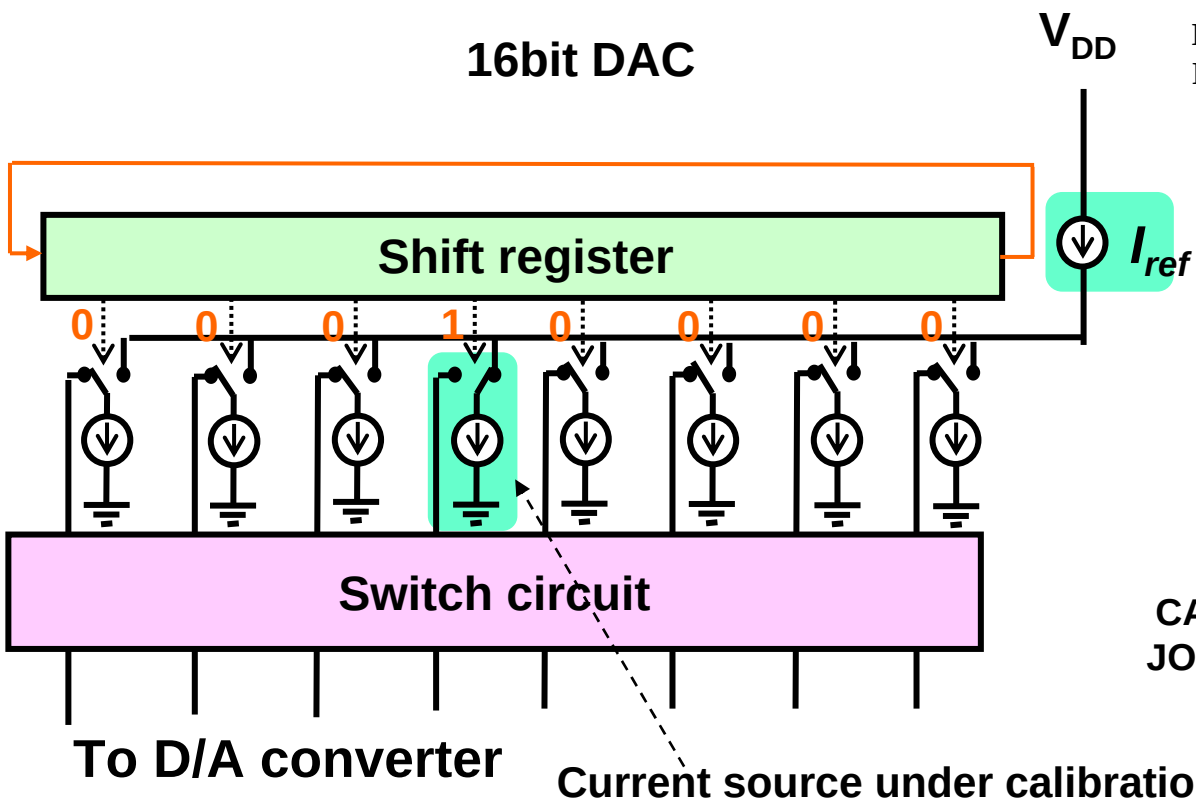
Issue in high precision analog design

High precision analog circuit design conventionally results in increase of power dissipation and IP cost, decrease of frequency performance

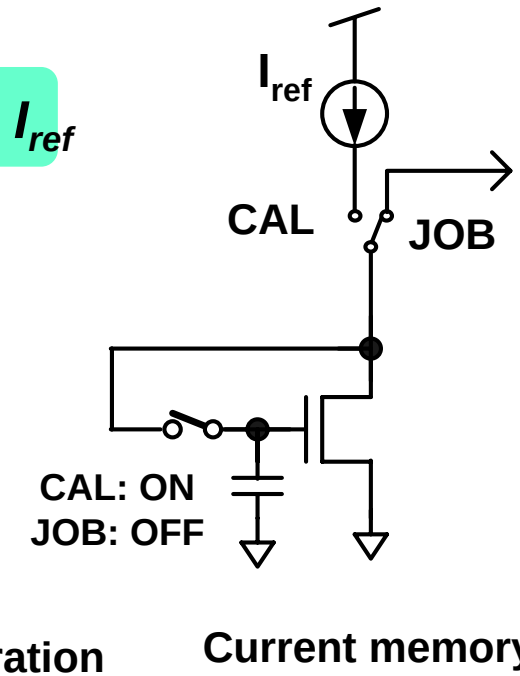


Dynamic current compensation

Each current source can be set equal by current memory method.
Shit register and one extra current source can realize calibration on the job.



H.J. Schouwenaas, et al.,
IEEE, JSC, vol.23, pp.1290-1297, Dec, 1988.



Self-Calibrated DAC

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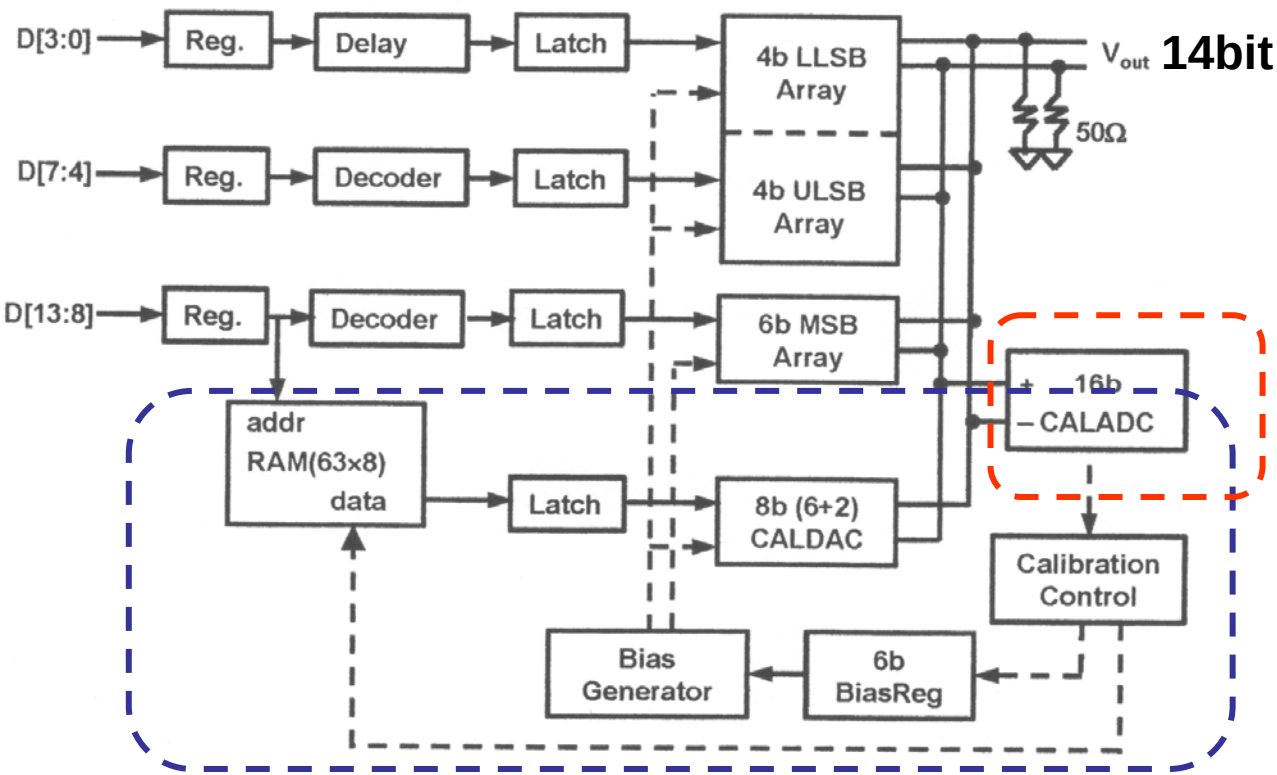
CAL-ADC measures non-linearity of DAC and compensates it's non-linearity by CAL-DAC with logic



Y. Cong and R. L. Geiger,
Iowa state university, ISSCC 2003

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Effectiveness and issues of CAL-DAC

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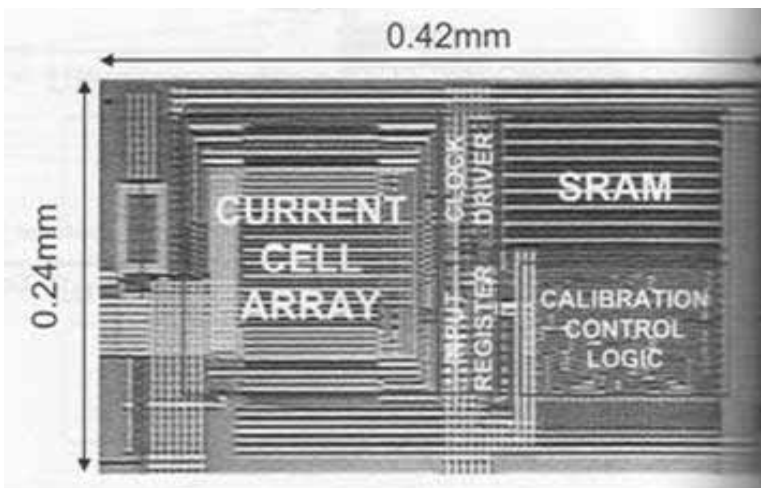
Digital calibration can reduce non-linearity dramatically.
We can realize high precision DAC in small area and power dissipation.

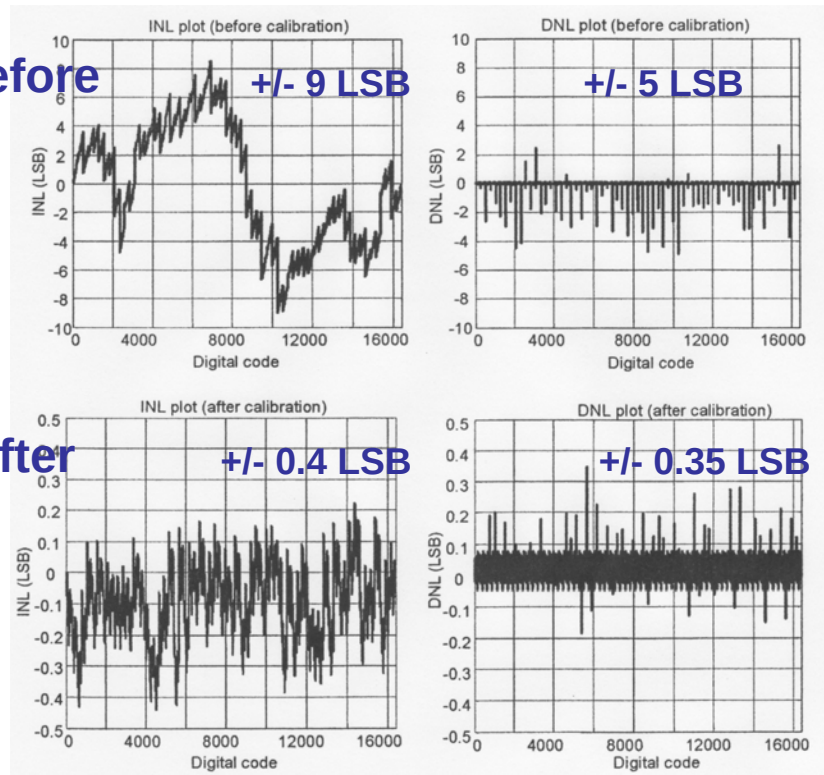
However, unrealistic, because it needs high precision ADC!!

14bit DAC **INL** **DNL**

14b 100MS/s DAC
1.5V, 17mW, 0.1mm^2, 0.13um
SFDR=82dB at 0.9MHz, 62dB at 42.5MHz

Area: 1/50 **Pd: 1/20**





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Self-Calibrated Binary DAC

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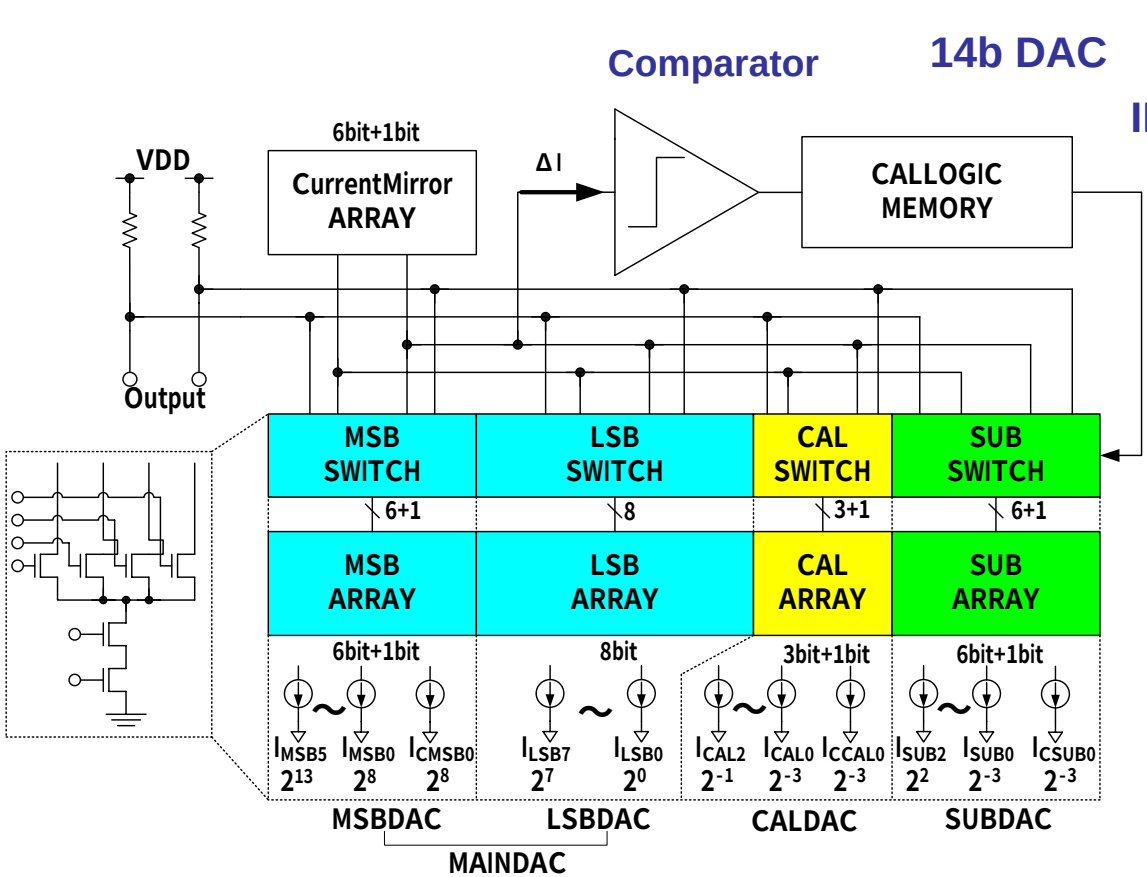
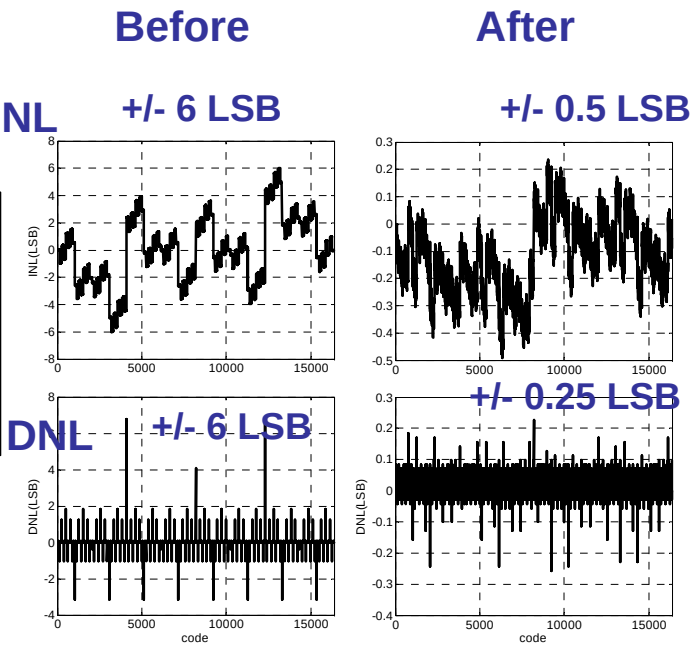
We have developed self-calibrated Binary DAC without CAL-ADC. Comparator can calibrate non-linearity. No high precision ADC is needed.





Y. Ikeda, A. Matsuzawa, "Digital Calibration Method for Binary-Weighted Current-Steering D/A-Converters without Calibration ADC", IEICE TRANS. ELECTRON, vol. E90-C, No.6, pp.1172-1180, June. 2007

Error compensation by comparator

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Nature of binary weighted values

$$\frac{1}{2^m} = \sum_{n=1}^{i} \frac{1}{2^{m+n}} + \frac{1}{2^{m+i}}$$

Example

$$\frac{1}{2^4} = \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} + \frac{1}{2^8}$$

1) Measure LSB value by CAL DAC with certain accuracy. $\frac{I_o}{2^N}$

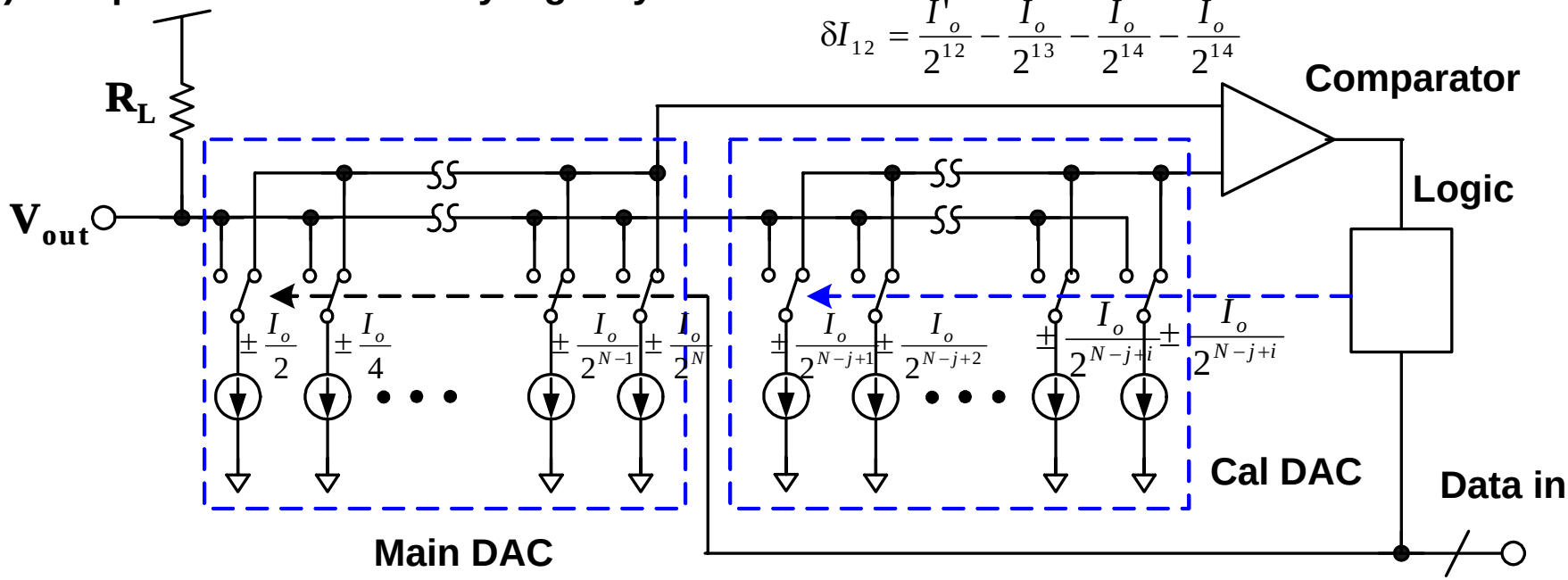
2) Measure the error of each current source by comparator with binary search .

$$\delta I_m = \frac{I'_o}{2^m} - \sum_{n=1}^{N-m} \frac{I_o}{2^{m+n}} - \frac{I_o}{2^N}$$

$$\delta I_{13} = \frac{I'_o}{2^{13}} - \frac{I_o}{2^{14}} - \frac{I_o}{2^{14}}$$

$$\delta I_{12} = \frac{I'_o}{2^{12}} - \frac{I_o}{2^{13}} - \frac{I_o}{2^{14}} - \frac{I_o}{2^{14}}$$

3) Compensate the errors by digitally



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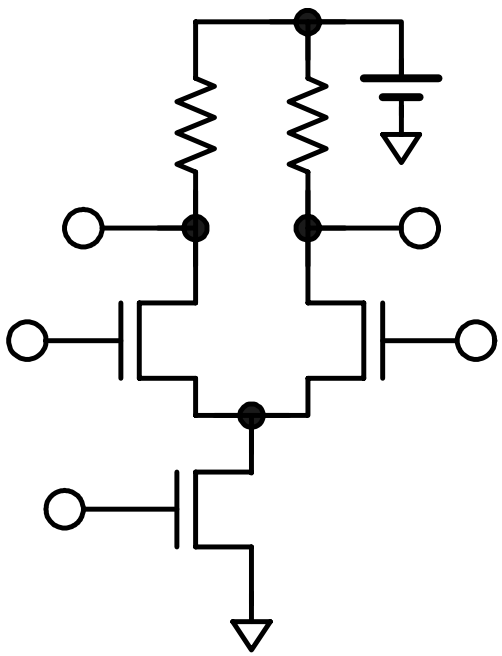
Comparator and offset suppression

Store the offset voltage in capacitor and subtract it from the signal

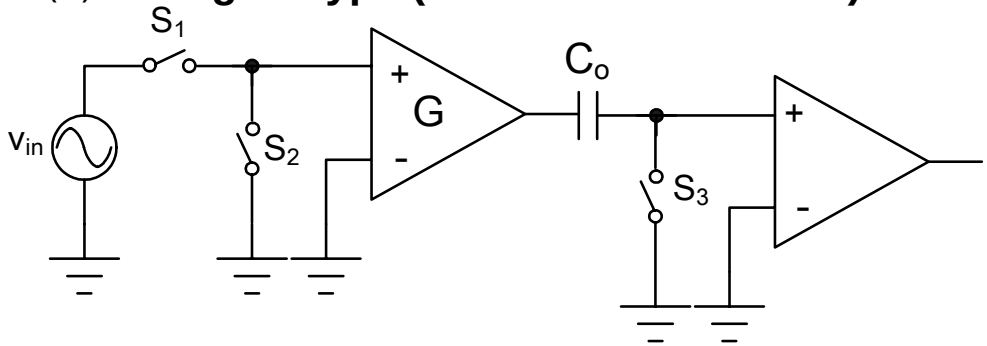
V_{off} at sigma reaches 30mV in CMOS comparator



Basic CMOS comparator

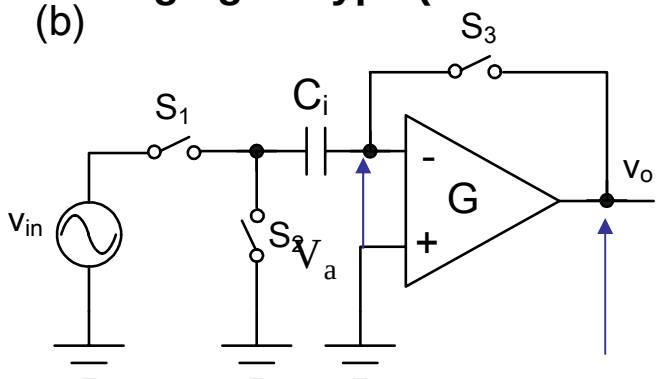
Offset suppression

(a) **Low gain type (feed forward method)**



High gain type (feedback method)

(b)



$$(V_a - V_{os})(-A) = V_o = V_a$$

$$\therefore V_o = V_a = \frac{A}{1+A} V_{os}$$

Digital Comparator offset compensation

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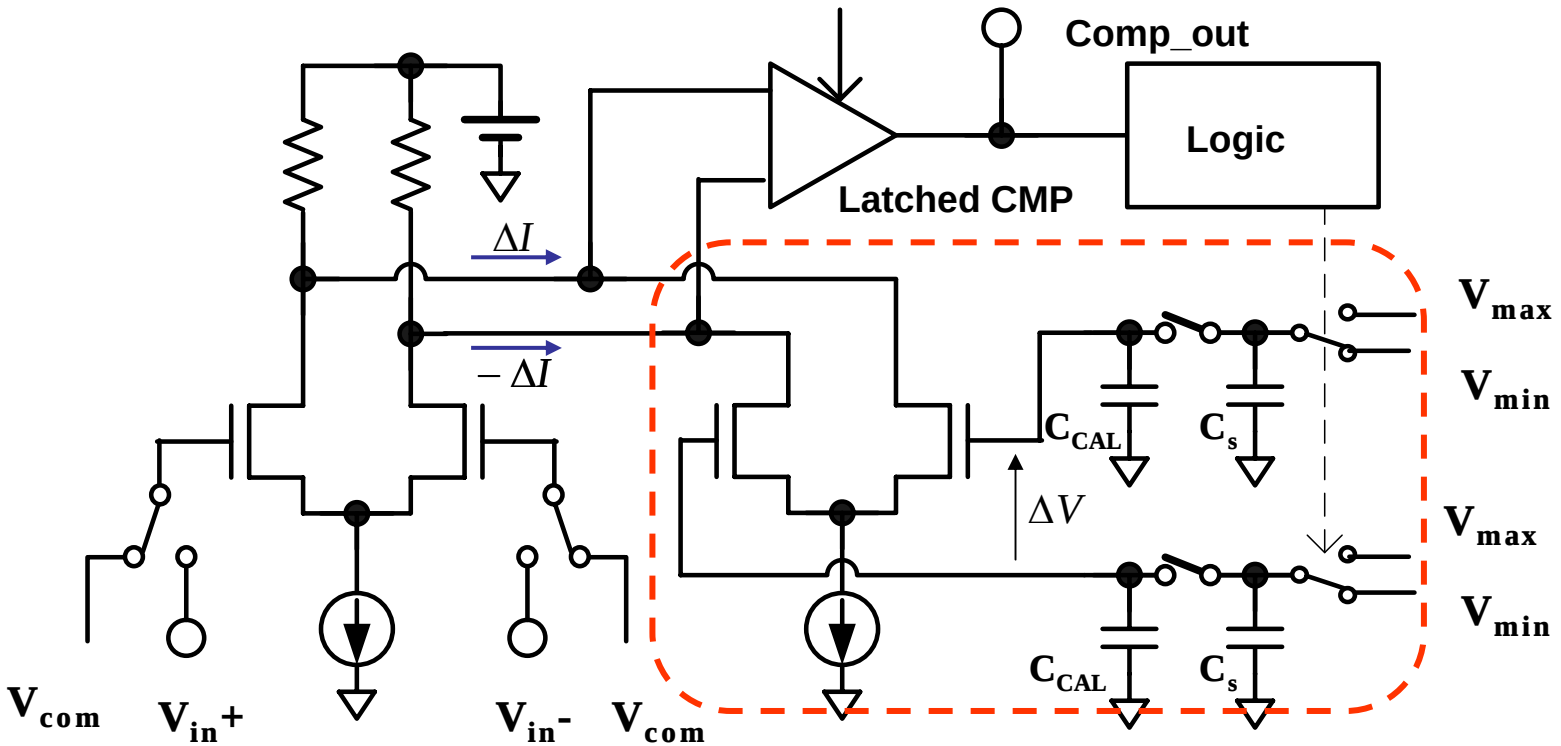
Offset voltage of latched comparator can't be compensated by previous method. Because it has no bias point. In this case, digital method should be applied.

Input terminals are shorted and the output signal controls applied voltage to the differential pair in CAL circuits so that the frequency of occurrence in differential output signals become equal.



CAL circuits

$C_{CAL}=10\ C_s$

"A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC"
Pedro M. Figueiredo, et al., ISSCC 2006

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Capacitor mismatch in pipelined ADC

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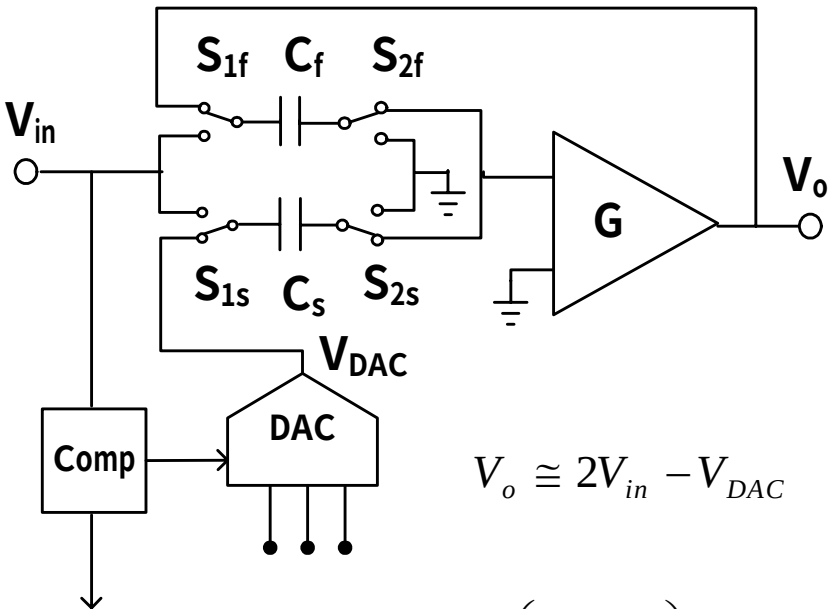
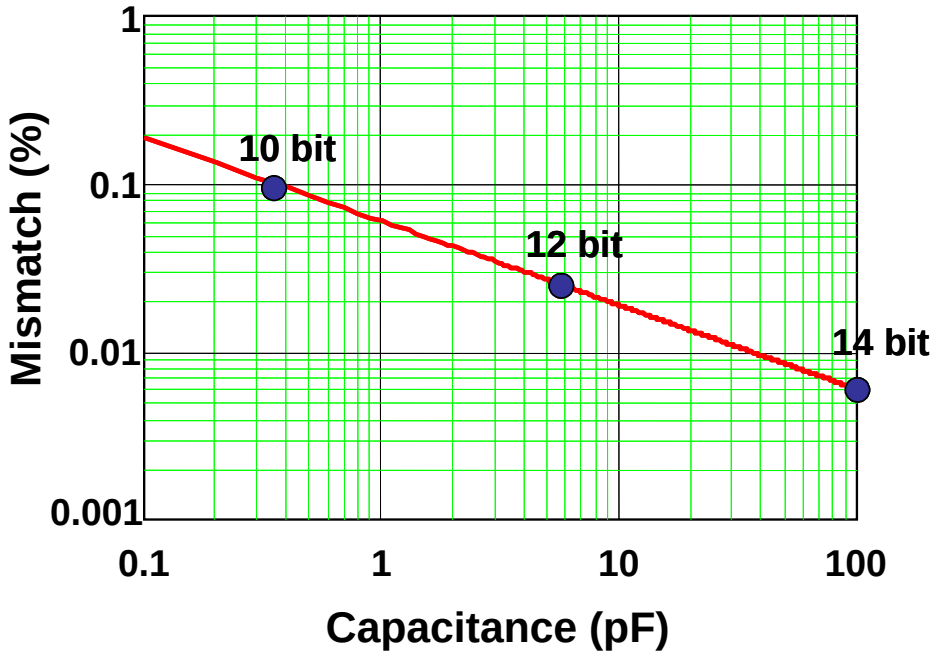
Capacitor mismatch in pipelined ADC determines the conversion accuracy. For the higher resolution, the larger capacitance is needed.



$$V_o \cong 2V_{in} - V_{DAC}$$



$$V_o \cong V_{in}\left(1+\frac{C_s}{C_f}\right)-\frac{C_s}{C_f}V_{DAC}$$

$$\Delta V_o = \left(\frac{\Delta C_s}{C_s}-\frac{\Delta C_f}{C_f}\right)\left(V_{in}-V_{DAC}\right) \qquad \frac{\Delta C}{C} < \frac{1}{2^N}$$

$$\frac{\Delta C}{C}(\sigma) = \frac{2\times 10^{-4}}{\sqrt{C_{(pF)}}}$$

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Capacitor mismatch compensation

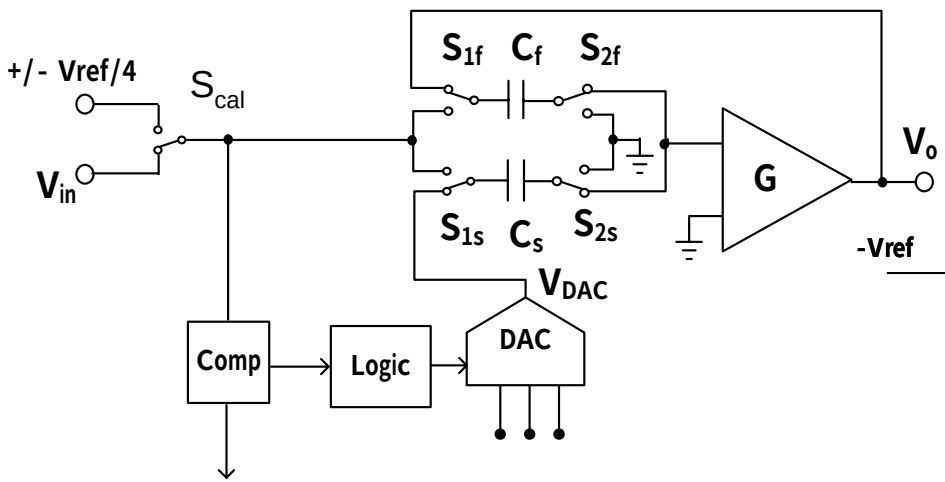
Capacitor mismatch causes the large conversion value differences at the input voltage where the comparator changes the DAC voltage.

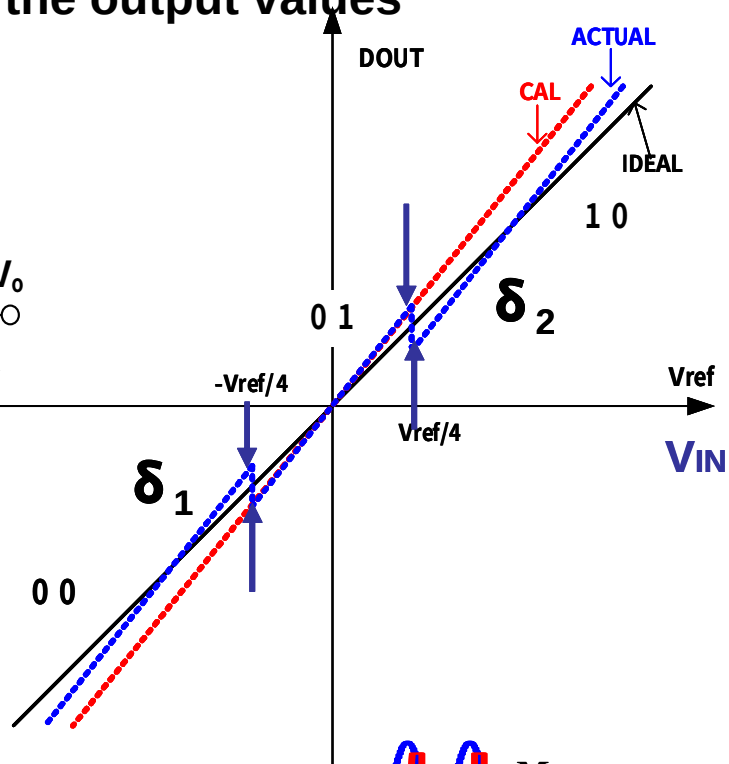
Compensation method:

1) Select input signal to +/- $V_{ref}/4$

2) Convert this value with V_{DAC}=0 and +/- V_{ref} and obtain δ_1 and δ_2 .

3) Add or subtract this δ_1, δ_2 to or from the output values





S. Y. Chung and T. L. Sculley," A Digitally Self-Calibrating 14-bit 10MHz CMOS Pipelined A/D Converter." IEEE, JSC, Vol. 37, No.6, pp. 674-683, June 2002.

1/fノイズ

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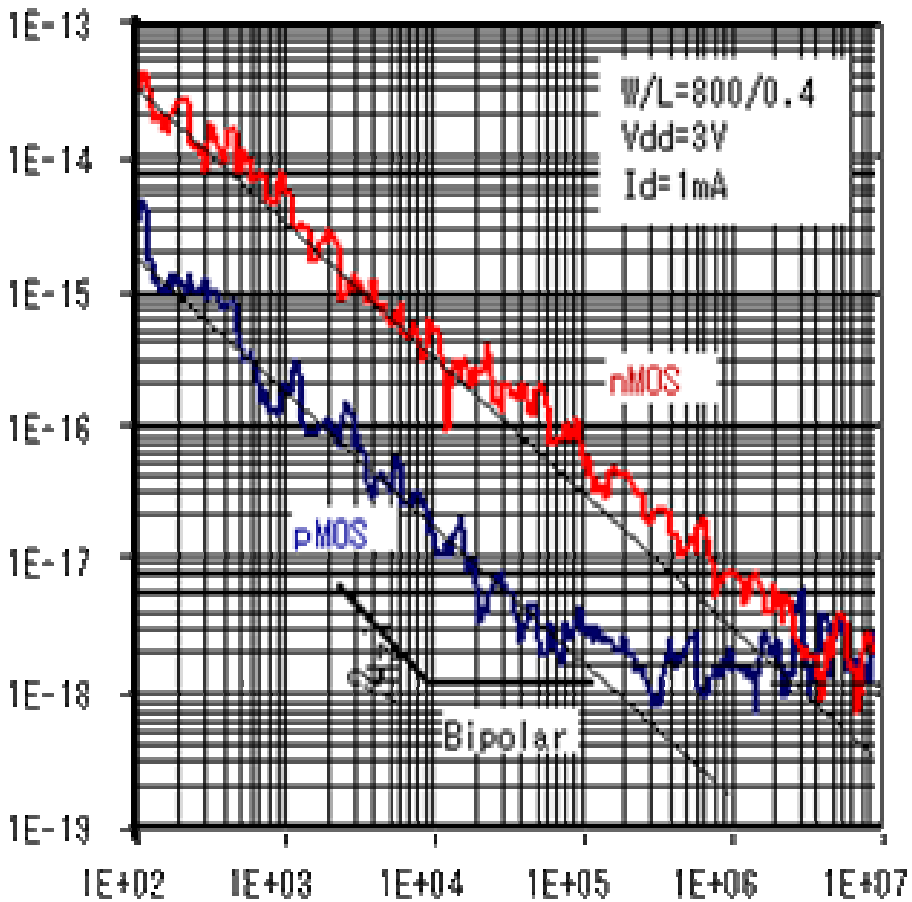
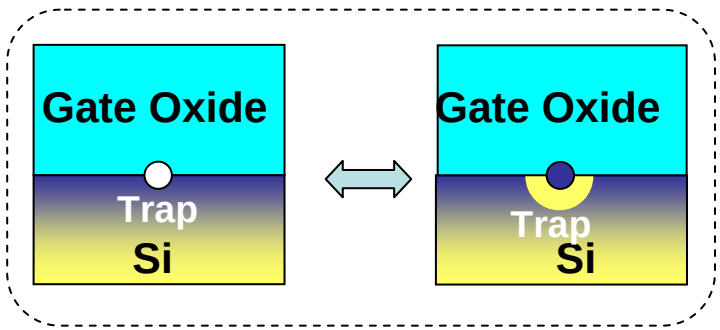
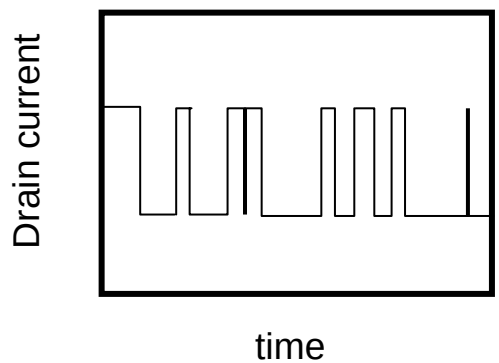
1/f noise degrades SNR of base-band signal seriously.
The 1/f noise from MOS is one or two order of magnitude higher than bipolar.
The larger gate area is needed to reduction this noise.



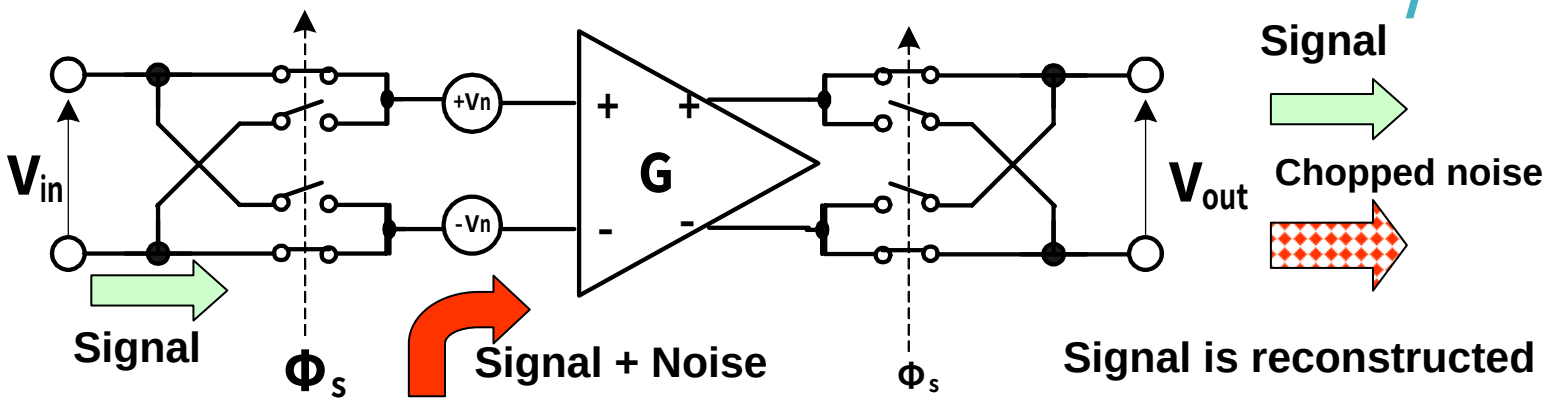
$$S_{\Delta V_G} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}$$





Chopper amplifier

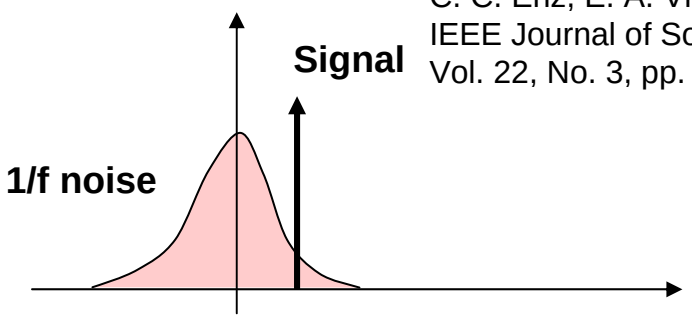
Chopper technique is often to be used to reduce the effect of 1/f noise.

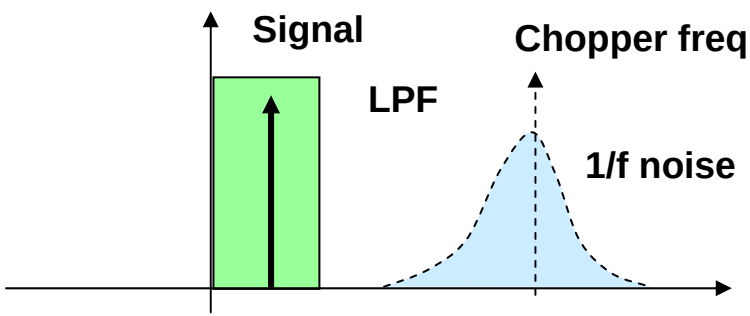


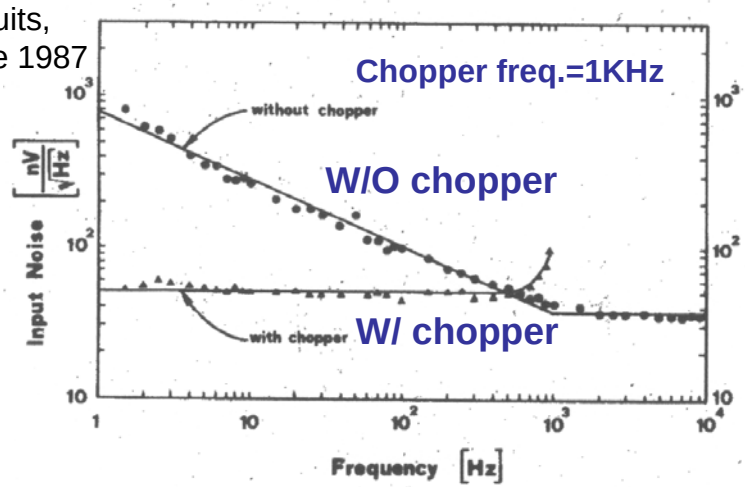
Signal is reconstructed

Noise is filtered out

C. C. Enz, E. A. Vittoz, and F. Krummenacher,
IEEE Journal of Solid-State Circuits,
Vol. 22, No. 3, pp. 335-342, June 1987







$$S_{Nout}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n:odd}}^{\infty} \frac{1}{n^2} |G(f - nf_s)|^2 S_{Nin}(f - nf_s)$$

Image-rejection mixers

Image can be rejected theoretically.
However, the image still remains due to gain and phase mismatch.

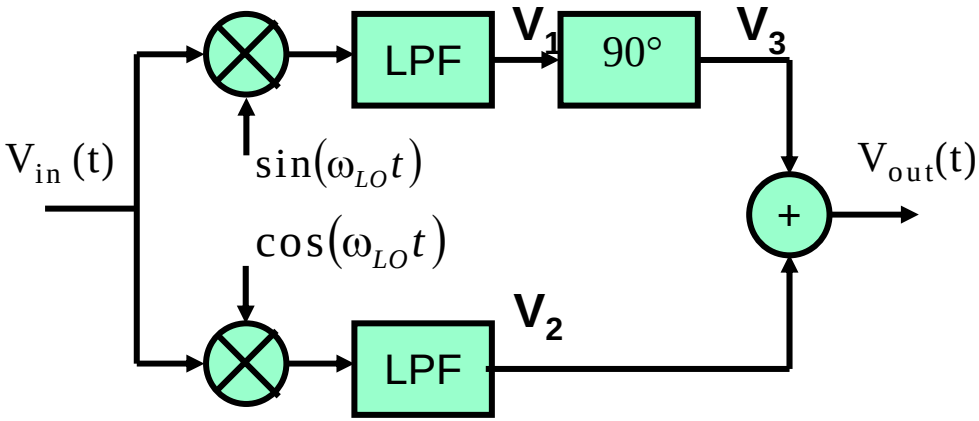
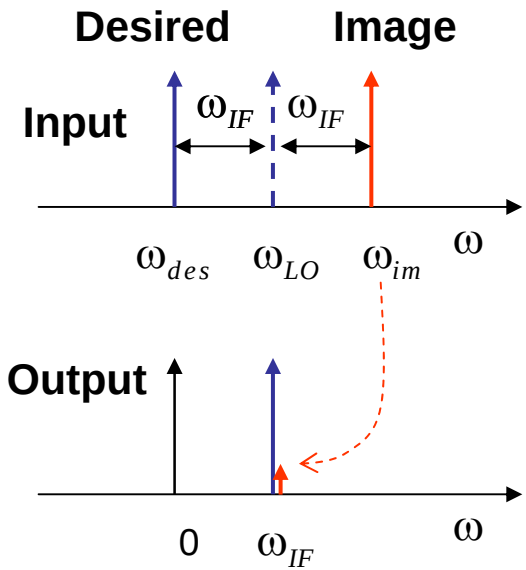


Image rejection mixer



$$V_1(t) = -\frac{V_{des}}{2}\sin(\omega_{des} - \omega_{LO})t + \frac{V_{im}}{2}\sin(\omega_{LO} - \omega_{im})t$$

$$V_2(t) = \frac{V_{des}}{2}\cos(\omega_{des} - \omega_{LO})t + \frac{V_{im}}{2}\cos(\omega_{LO} - \omega_{im})t$$

$$V_1(t) \rightarrow 90^\circ \ shift = V_3(t) = \frac{V_{des}}{2}\cos(\omega_{des} - \omega_{LO})t - \frac{V_{im}}{2}\cos(\omega_{LO} - \omega_{im})t$$

$$V_{out}(t) = V_{des}\cos(\omega_{des} - \omega_{LO})t$$

Image is rejected, however,…

Gain mismatch and phase error

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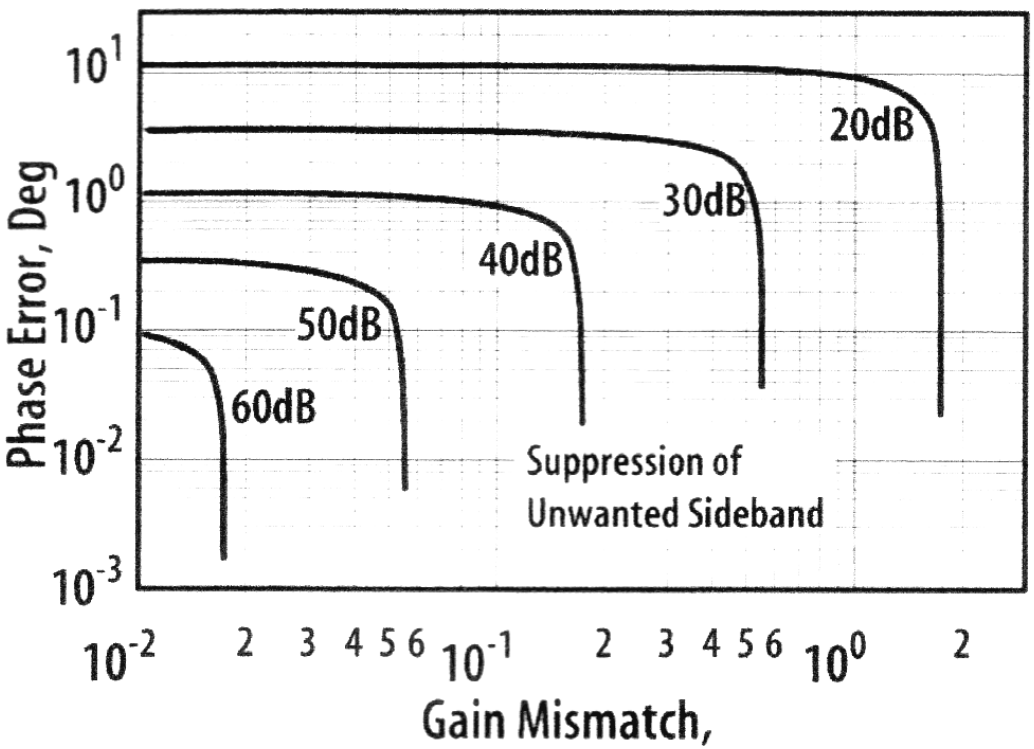
It is very difficult to realize high image rejection ration being higher than 40 dB by analog techniques.

0.1 deg and 0.01% are needed for IRR of 60dB



Conventional IRR: 35dB

IRR: Image rejection ratio

$$IRR \approx \frac{\left(\frac{\Delta G}{G}\right)^2 + (\Delta\theta)^2}{4}$$

A. Rofougaran, et al., IEEE J.S.C. Vol.33, No.4, April 1998. PP. 515-534.

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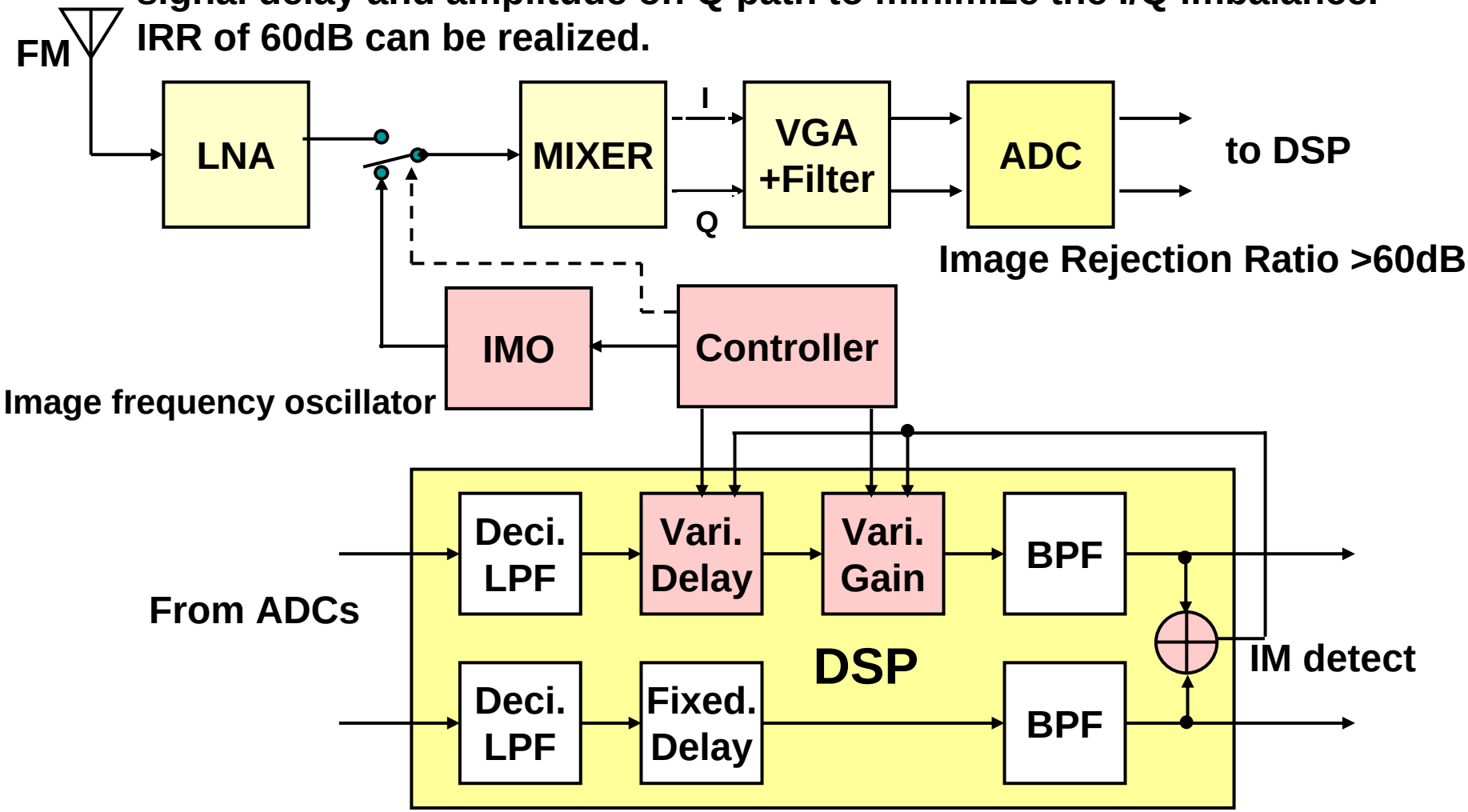
Digital image rejection technique

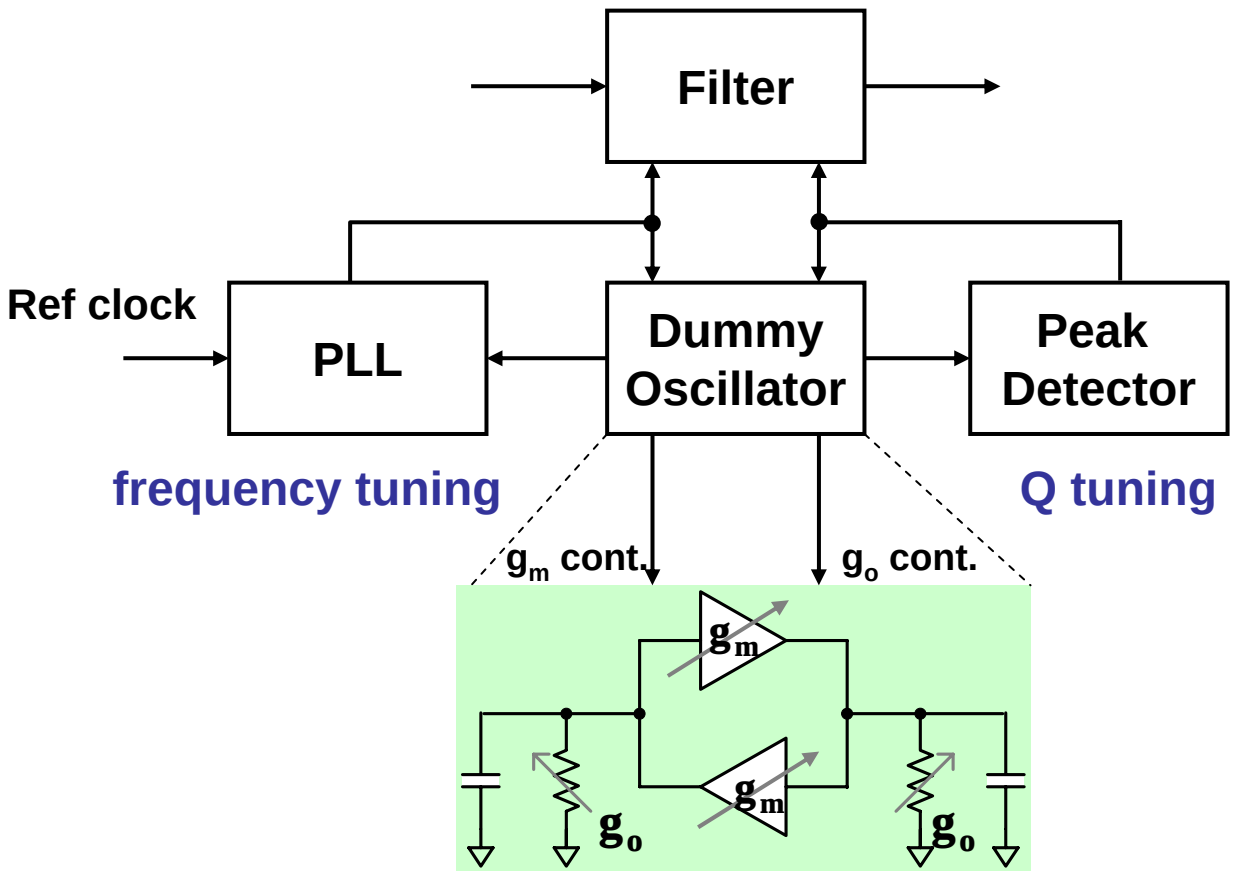
The dummy image signal is generated by IMO and the controller controls signal delay and amplitude on Q path to minimize the I/Q imbalance. IRR of 60dB can be realized.



CT filter tuning

RC or gmC circuits can realize active filter circuits,
However, frequency characteristics and Q of the filter are strongly affected by Absolute value of R, C, gm and PVT fluctuation.
Then, the filter tuning circuit is vital.

Filter circuit can be used as oscillator, if the Q become infinity.



Digital calibration in mixed signal SoC

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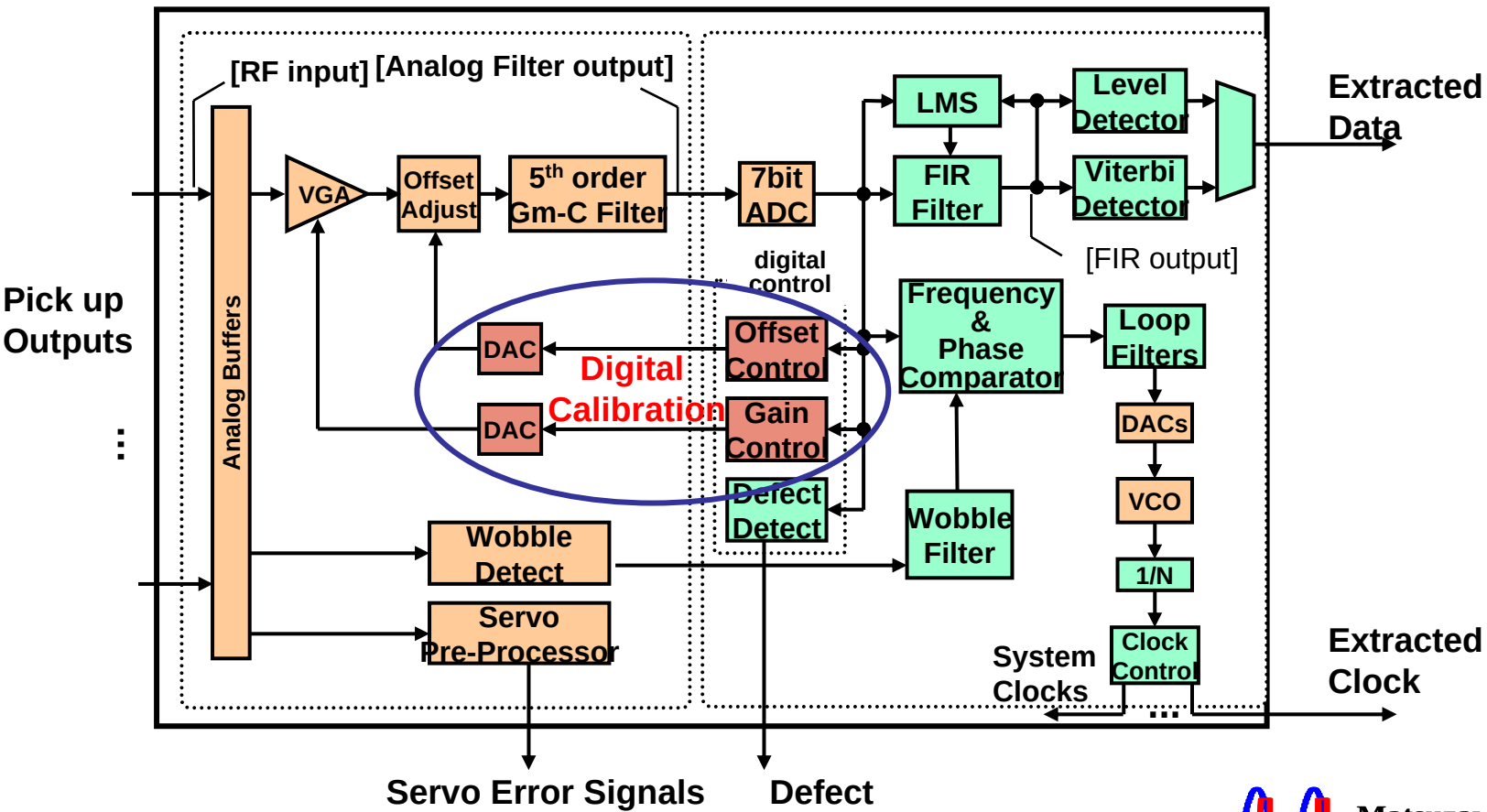
To keep high production yield and stable operation against PVT fluctuation, mixed signal SoC has many digital self calibration circuits.
MCU controls many analog parameters.

PRML circuit for DVD recorder



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Issues of analog compensation techniques

- **Basically use discrete-time technology**
  - **Difficult to apply Continuous-Time circuits.**
  - **Needed clock causes another noise.**
- **Some need calibration period**
  - **At power on**
    - **Needs not short time to wait the system becomes stable.**
    - **Some different situation at the power on.**
  - **Idling time on the job**
    - **Can get sufficient time for calibration?**
    - **Too much system depended.**
- **Calibration on the job**
  - **Conventionally needs extra circuits. Cost and power consumption increase.**
  - **Needs many calibration time, if statistical methods are used.**

Conclusion

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- **Analog circuits require compensation technique**
  - **Mismatch is inversely proportional to the square root of area.**

$$\Delta V_T, V_{n\_1/f}, \left(\frac{\Delta C}{C}\right), \left(\frac{\Delta R}{R}\right) \propto \frac{1}{\sqrt{S}}$$

  - **Control of absolute vale of device parameters is difficult.**
  - **Also, device parameters are affected PVT fluctuation easily.**
  - **If not use of compensation techniques**
    - **Large area, large power consumption, poor frequency performance.**
- **Compensation techniques are very effective to improve precision of circuits, production yield, and durability to PVT fluctuations**
- **However, they have many issues**
  - **Basically DT method are used and difficult to apply CT circuits.**
  - **Need calibration periods**