Compensation techniques for integrated analog device issues

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1. Introduction

For many applications in various areas—from communications, networks, storage systems, sensors, and displays to power supplies—the analog and RF parts of recent LSI technologies play an important role. There are, however, many issues with integrated devices, such as mismatch, noise, and distortion. This paper reviews some important compensation techniques to address these issues.

2. Capacitor Mismatch

Device mismatch causes degradation of circuit accuracy. For example, the accuracy of a pipelined ADC, which is the major A/D conversion architecture for high speed applications [1], is mainly determined by its capacitor mismatch.

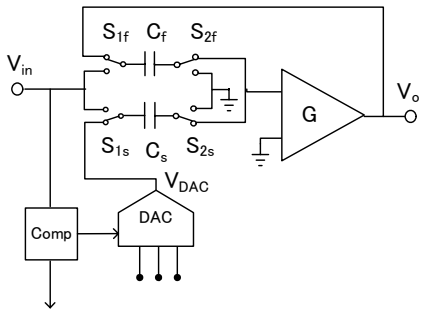

Fig. 1. Conversion unit in a pipelined ADC.

Figure 1 shows a conversion unit in a pipelined ADC. If the voltage gain of an operational amplifier is large enough, the output voltage V_o is

$$V_o \cong V_{in}\left(1+\frac{C_s}{C_f}\right)-\frac{C_s}{C_f}V_{DAC}. \qquad (1)$$

The closed loop gain has to be exactly two, otherwise nonlinearity errors will occur. Furthermore, capacitor mismatch is a major error source in pipelined ADCs; an acceptable capacitor mismatch is

$$\frac{\Delta C}{C} < \frac{1}{2^N}, \qquad (2)$$

where N is the resolution of the ADC.

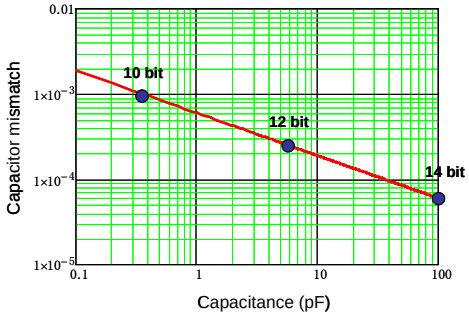

Fig. 2. Capacitor mismatch vs. capacitance.

The capacitor mismatch is inversely proportional to the square root of the capacitance:

$$\frac{\Delta C}{C} \propto \frac{1}{\sqrt{C}}. \qquad (3)$$

Therefore, a larger capacitance is required for ADCs with a higher resolution, as is shown in Figure 2. Unfortunately, this leads to a decrease of conversion speed and an increase in power dissipation and IP cost.

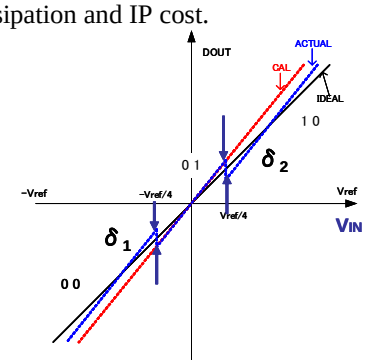

Fig. 3. I/O transfer curve of a pipelined ADC.

Recently, a digital calibration method has been applied to address this issue [2]. Figure 3 shows the I/O transfer curve of a pipelined ADC. Large discontinuities are observed where the DAC voltages are changed, at V_{in} = +/-V_{ref}/4, causing large non-linearity errors. To suppress such errors, the discontinuities are measured by changing the DAC voltages from V_{ref} to zero or from zero to –V_{ref}, under the condition that the input voltage is fixed to

+/-V_{ref}/4. These error values are stored in the registers and subtracted from the uncorrected values.

This digital compensation technique can reduce the required capacitance and, therefore, increase the conversion speed and reduce the power dissipation as well as the IP cost.

3. V_T Mismatch

V_T mismatch causes the offset voltage to fluctuate and it determines the accuracy of analog circuits.

V_T mismatch is inversely proportional to the square root of the gate area,

$$\Delta V_T \propto \frac{1}{\sqrt{S_g}}. \quad (4)$$

Thus, analog circuits whose offset voltage needs to be small require a large gate area. This results in a decrease of operating speed and an increase of power dissipation and IP cost. One way to address this issue is to use the following analog compensation technique.

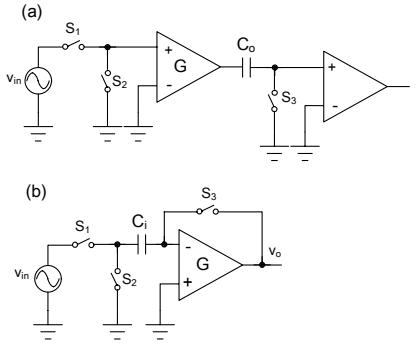

Fig. 4. Analog offset compensation circuits.

Figure 4 shows a conventional analog offset compensation technique using a switched capacitor method [3]. When the switches S_2 and S_3, in the circuit shown in Figure 4(a), are closed and the switch S_1 is opened, the amplified offset voltage appears at the output node and is stored on the capacitor C_o. If the switches S_2 and S_3 are opened and switch S_1 is closed, the sum of the amplified input signal and the offset voltage will appear at the output node, however, the stored voltage in C_0 cancels out the amplified offset voltage.

However, because the output voltage becomes saturated if the gain is too high, this method is only effective when the amplifier gain is small. Figure 4(b) shows an offset compensation technique if high gain amplifiers are used. When the switches S_2 and S_3 are closed and switch S_1 is opened, the offset voltage can be stored in the capacitor Ci and cancelled out.

4. 1/f Noise

1/f noise is a low frequency noise. Conventionally, the spectrum of 1/f noise reaches several MHz and reduces the SNR for many applications. Furthermore, the magnitude of 1/f noise of MOS transistors is two orders higher than that of bipolar transistors. A conventional technique to reduce the effect of this noise is to use the chopper amplification method [4].

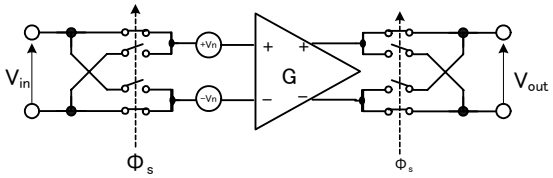

Fig. 5. Chopper amplification method.

The input signal drives the input terminal of an amplifier and the polarity is changed periodically by the clock pulse. The polarity of the output signal of the amplifier is also changed synchronously with the input clock pulse.

Thus, the switching does not affect the amplified signal; however, the polarity of the noise signal at the output node is changed periodically. The noise spectrum is changed alike:

$$S_{Nout}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n:odd}}^{\infty} \frac{1}{n^2} |G(f - nf_s)|^2 S_{Nin}(f - nf_s), \quad (5)$$

where G is the gain of the amplifier, f_s is the switching frequency for the chopping, and S_{Nn} is the noise spectrum density. The spectrum of the 1/f noise is shifted from around DC to around f_s, $3f_s$, $5f_s$…. The 1/f noise can therefore be suppressed by low-pass filtering. Unfortunately, this method also folds the thermal noise spectrum from higher frequencies to lower frequencies, thus increasing the effect of thermal noise. Therefore, the filter needs to be designed carefully.

5. Conclusion

The effects of integrated device issues, such as capacitor mismatch, V_T mismatch, or 1/f noise can be suppressed by analog and digital compensation techniques. The usefulness of these techniques is limited because of other requirements like short calibration period, clock pulses, and low operating speeds. More advanced compensation methods should be developed to address future integrated device issues.

References

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