Direction of RF-CMOS tuner technology

Akira Matsuzawa

Department of Physical Electronics
Tokyo Institute of Technology

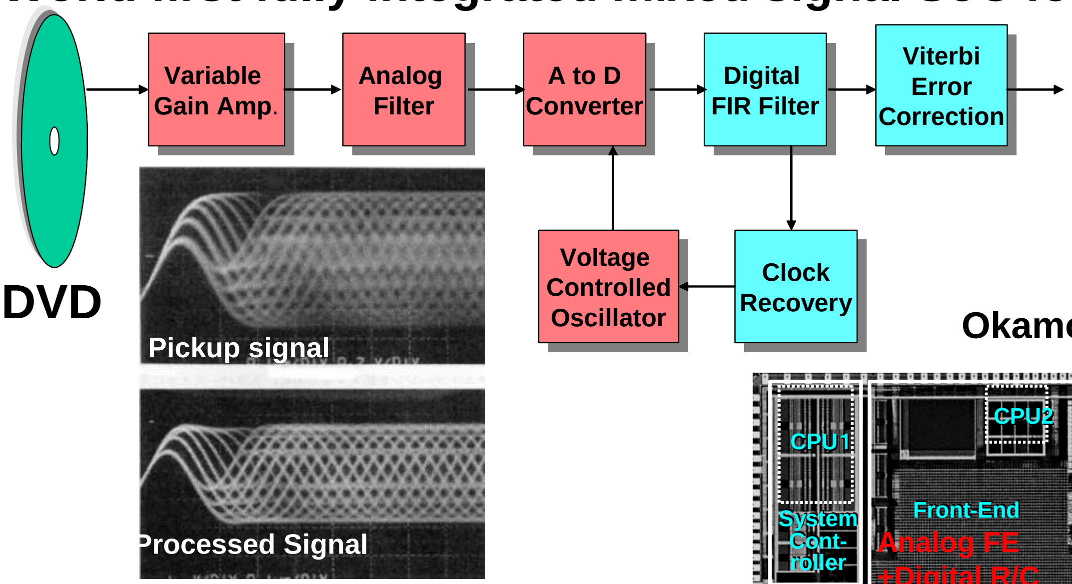
Matsuzawa & Okada Lab.

SoC for DVD systems

Before talking about RF-CMOS for tuners

Digital signal processing enables perfect cure for the damaged signals.

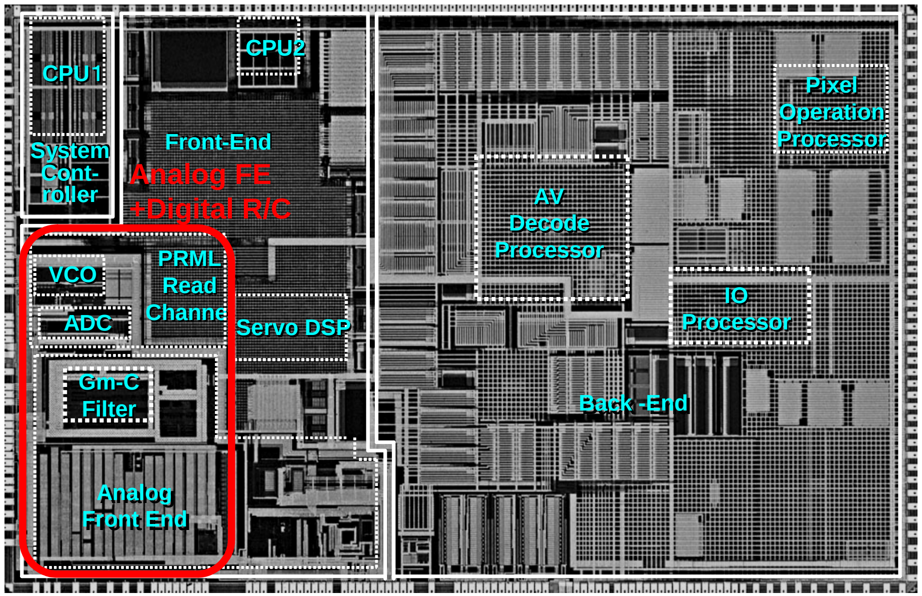
World first fully integrated mixed signal SoC for DVD systems has developed.



Digital read channel technology

0.13um CMOS, 24Mtr

Okamoto, et. al., ISSCC 2003.



7b, 400MHz, 40mW ADC has been developed

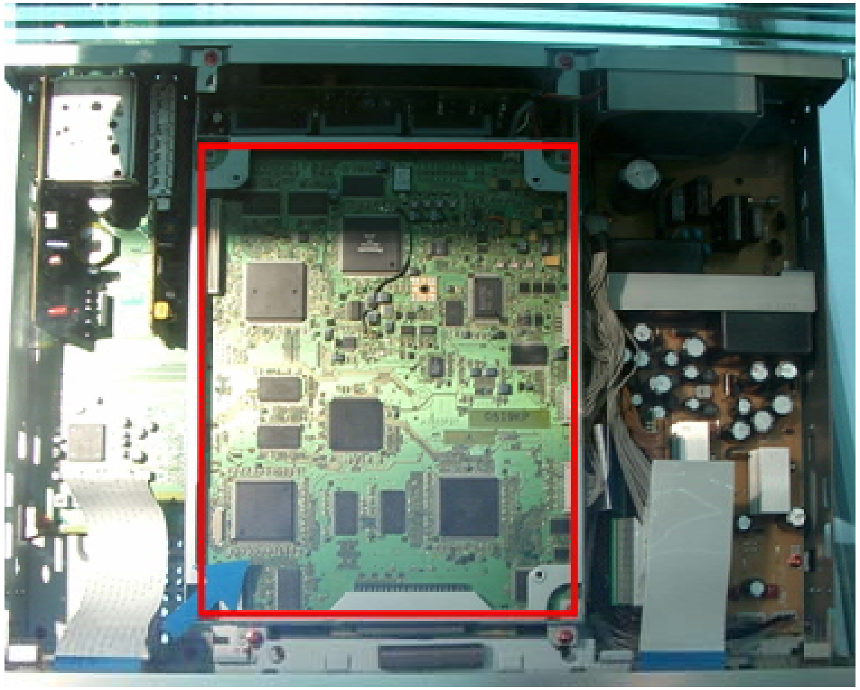
My last work in Panasonic

Power of SoC

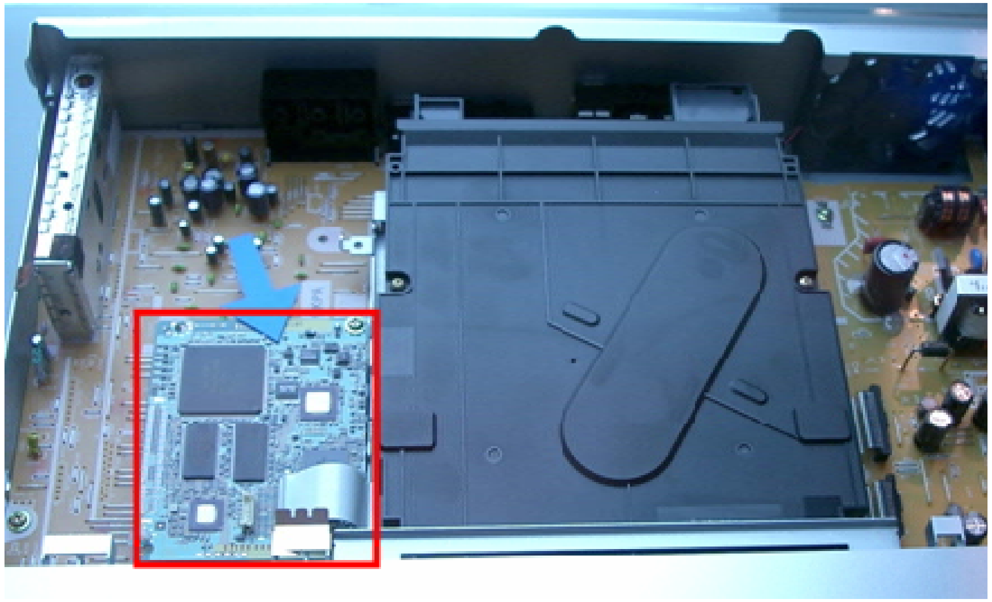
SoC has enabled performance increase and cost decrease.
Many components and ICs have been kicked out from the PC board.

Panasonic DVD recorder

Before SoC **Model;2000**



After SoC **Model; 2003**



Matsuzawa & Okada Lab.

Contents

- Conventional AM/FM tuner
- Analog-centric CMOS tuner
- Digital-centric CMOS tuner
- Feature of CMOS technology
- Conclusion

Courtesy Niigata-Seimitsu Co., Ltd.

E-mail: matsu@ssc.pe.titech.ac.jp
URL: http://www.ssc.pe.titech.ac.jp/

Current AM/ FM tuner system

Current AM/FM tuner uses 3 ICs and large # of external components.
Furthermore 12 adjustment points are needed.

Large # of products, but not expensive product.
More efforts for the cost reduction are still needed.

Bipolar IC = 1 (RF)
CMOS IC = 2 (PLL, RDS)
External Components=187

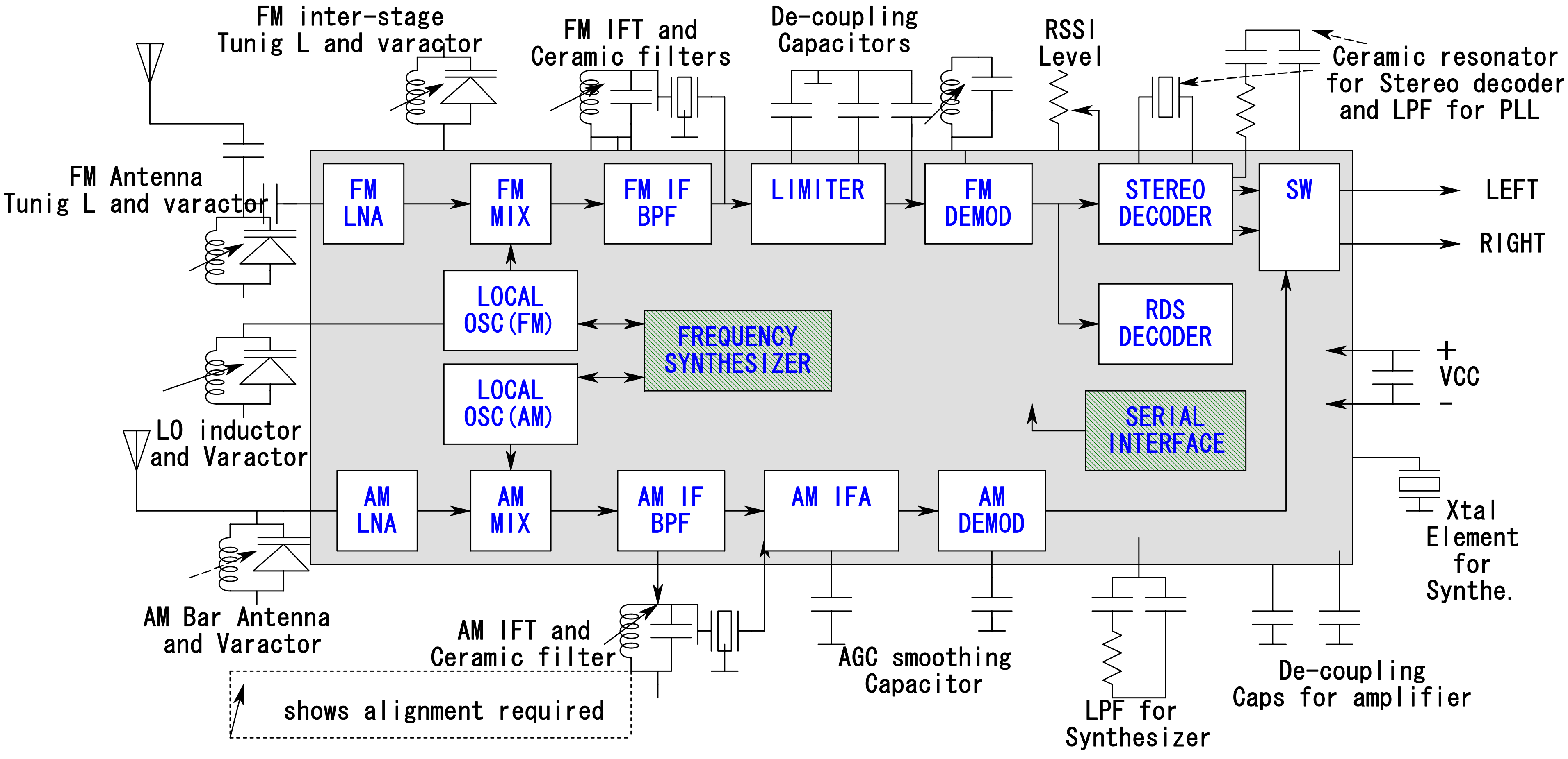
AM/FM Tuner for home use

12 adjustment points

Block Diagram of Current FM/AM tuner

TOKYO TECH
Pursuing Excellence

Large # of external components. They should be integrated on a chip.



Matsuzawa
& Okada Lab.

External parts used in existing IC

Large # of external components are needed due to analog signal processing.

External Parts	Blocks to be used
System	FM: Single conversion super heterodyne. IF=10.7MHz AM: Single or Double conversion super heterodyne IF=450KHz or 10.7MHz + 450KHz
Resistor	AGC, bias, LPF for PLL
Semi-fixed and Variable resistor	RSSI level alignment, volume control
Ceramic capacitor Small value capacitor	RF bypass, coupling, de-coupling
Electrolytic capacitor	AGC smoother, power-ground decoupling
Inductor	RF tuning, local oscillator, IF transformer, FM detector
Variable capacitance	RF tuning, Local oscillator
Analog filter	Noise canceller, LPF
Ceramic filter	FM and AM IF BPF for channel filter
Xtal Osc. element	System clock, Reference for PLL synthesizer
Total number of external parts	Home tuner and radio cassette tuner : around 165pcs Car tuner : 80 to 130pcs

Issues and conventional solutions of AM/FM tuner

Application of CMOS technology to AM/FM tuner looks very difficult, due to lower frequency and high dynamic range.

Lower frequency

AM: 522 KHz to 1710 KHz
SW: 2.3MHz to 26MHz
FM: 87.5 to 108 MHz

Larger Inductance and capacitance → **External components**

Serious 1/f noise → **Bipolar**

High dynamic range

AM: 14 dBuV to 126 dBuV
FM: 0 dBuV to 126 dBuV

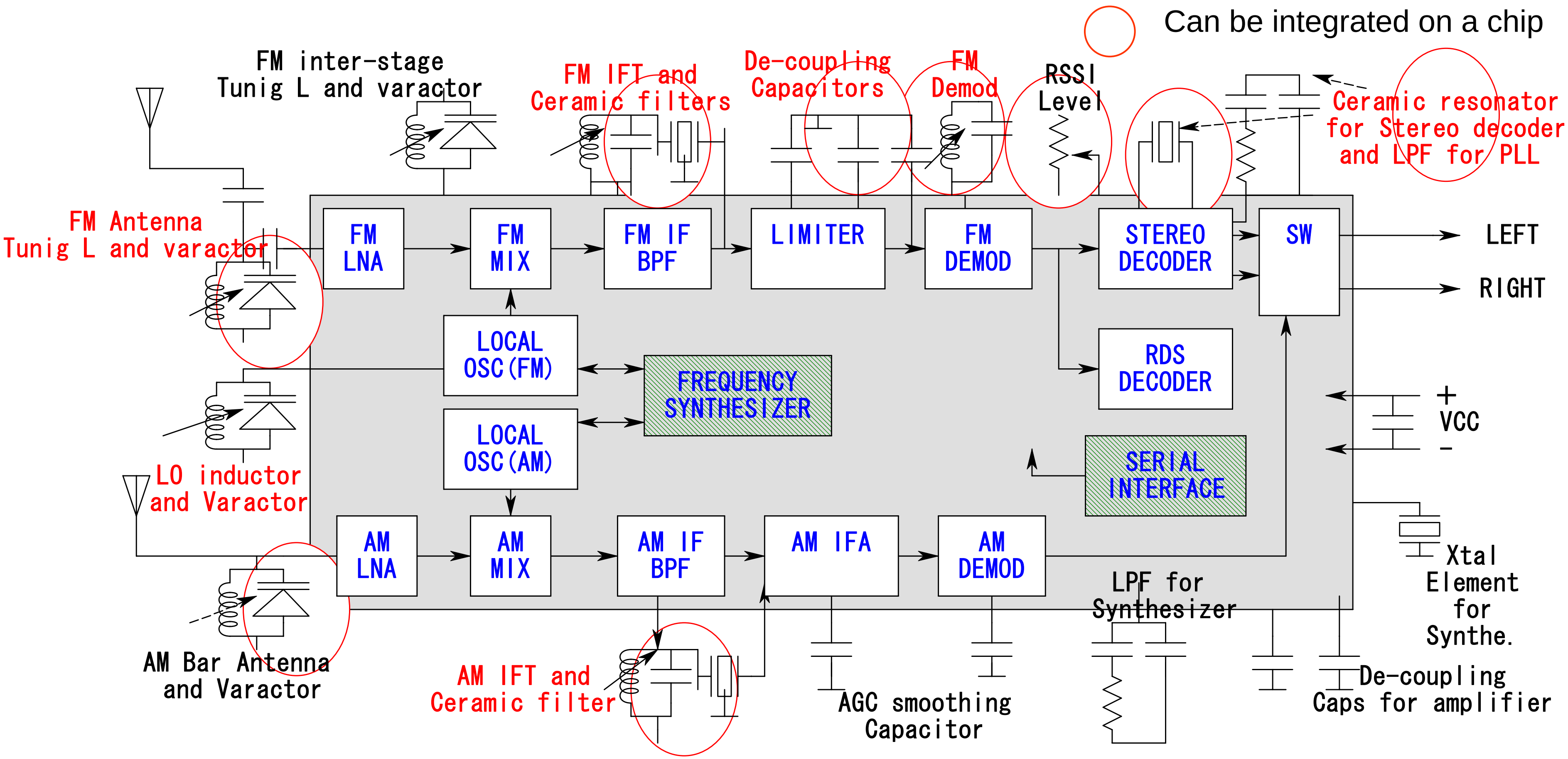
Sharp and fine filter → **External filters (Ceramic)**

High linearity ckt. → **External varactors**
Bipolar

1st trial by CMOS technology

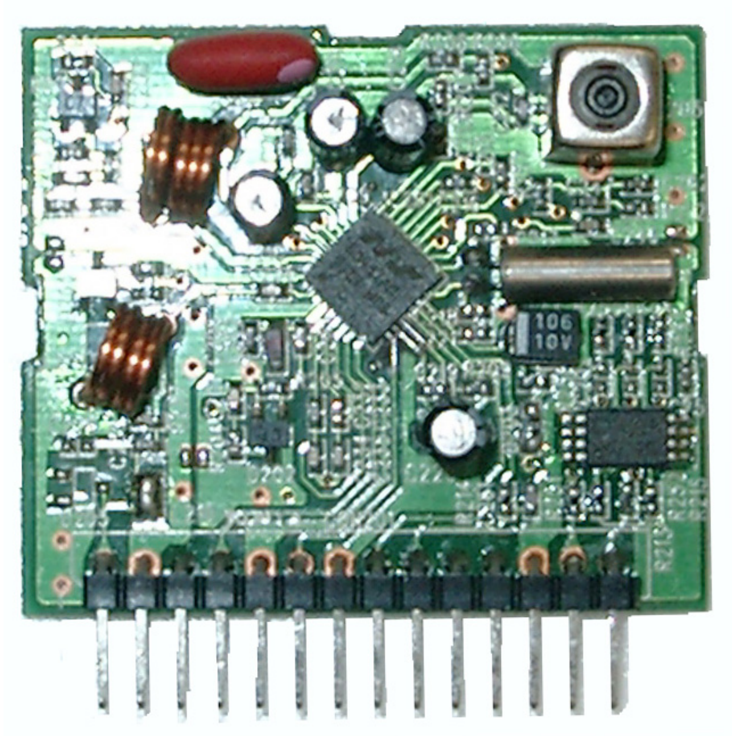
TOKYO TECH
Pursuing Excellence

1st trial to realize AM/FM tuner by CMOS technology, many external components should be reduced.



Result of analog-centric CMOS tuner

Characteristics is affected by process variation easily.
Element mismatch causes DC offset, noise, distortion, and low filter performance.
The reduction of # of external components is not attractive for users.



External components 187→ 69

Analog-centric CMOS tuner technology

TOKYO TECH Pursuing Excellence

1^{st} trial was analog-centric CMOS tuner technology.

Circuits have been replaced by CMOS, however still use analog technology. Thus it had many issues and many external components were still needed.

Parts	Methods for on-chip	Problems
AM/FM IF BPF	1. Low IF(a few hundred KHz) 2.Gm-C BPF with auto alignment, SCF	1.poor selectivity(-45dB), 2. SCF Switch noise 3. Center frequency shift by DC offset 4. Poor image rejection ratio (25 to 35dB)
FM Demodulator	Pulse count FM detector	Poor THD (0.5%)
Stereo Decoder	Multi-vibrator VCO, SCF filter	Large variation of free-run frequency Still need external LPF for PLL
RSSI Level adj.	Signal detector with DC compensation	Can't cover all process corner
Varactor	MOS varactor	Too much sharp C-V curve, distorted signal
AGC smoother	Time division charge and discharge	Needs large capacitor for low audio frequency
Capacitors	Stages Direct connection, use small value coupling capacitor	High impedance required, Difficult for low frequency

Issues and advanced solutions of AM/FM tuner

Lower frequency

AM: 522 KHz to 1710 KHz
SW: 2.3MHz to 26MHz
FM: 87.5 to 108 MHz

Larger Inductance and capacitance → **Digital filter, Mixer, PLL**
GHz OSC with divider

Serious 1/f noise → **PMOS**

Larger signal dynamic range

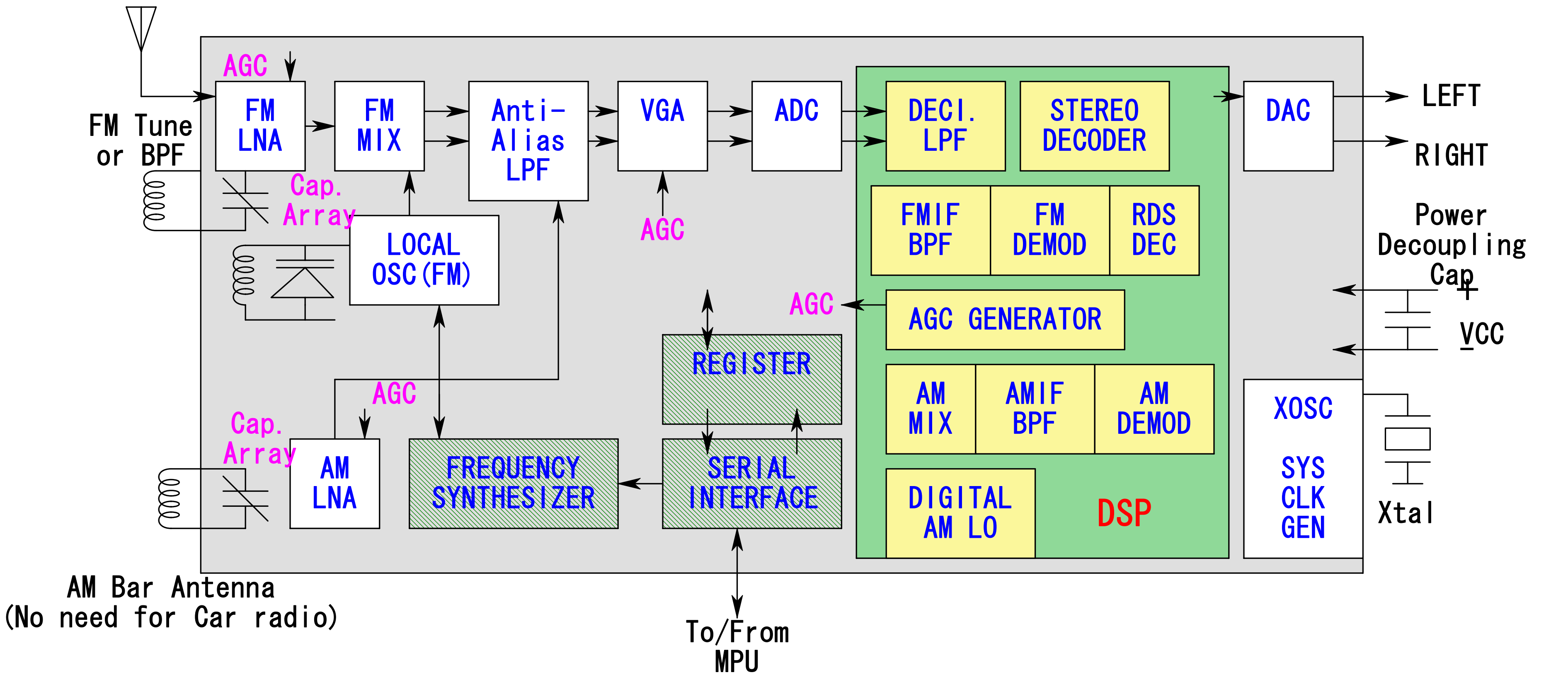
AM: 14 dBuV to 126 dBuV
FM: 0 dBuV to 126 dBuV

Sharp and fine filter → **Digital Signal processing**
With high resolution ADC
IF Freq. changed from
10.7 MHz to several 100 KHz

High linearity ckt. → **High resolution ADC**
Switch mixer
Watching desired and undesired signals

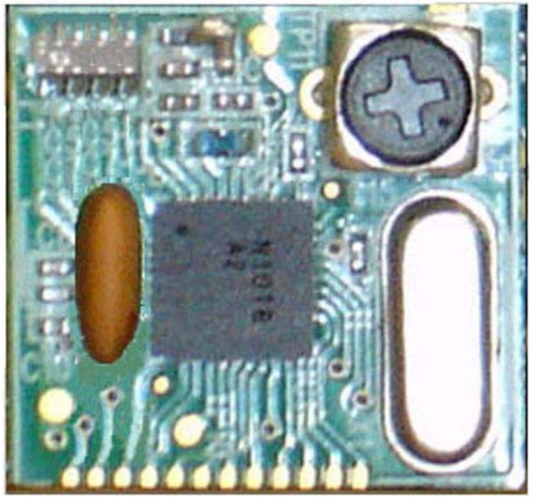
Advanced CMOS tuner

Digital-centric CMOS tuner has been developed.



Digital-centric CMOS tuner

One-chip CMOS tuner has been successfully developed.
It can attain high tuner performance and
can reduce the # of external components.
Furthermore it can realize no adjustment points.



Full CMOS one-chip solution

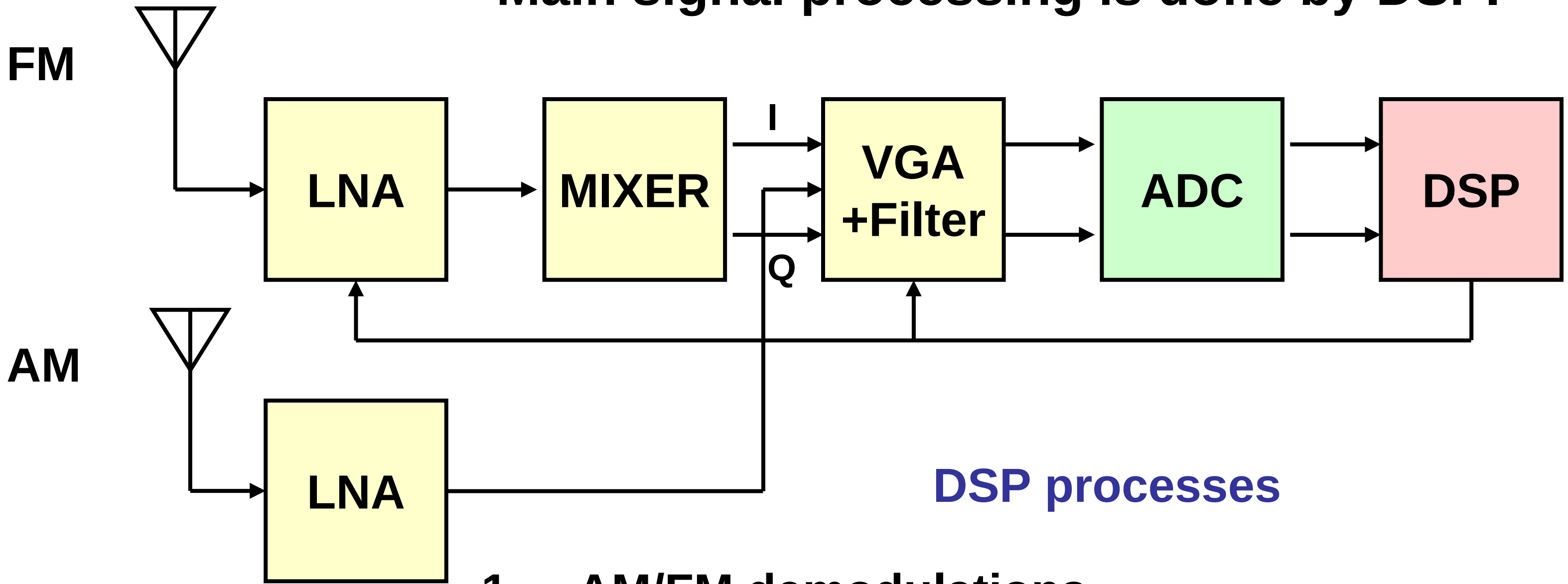
# of external components are 11

No adjustment points

Sensitivity: FM: 9dBuV, AM: 16dBuV
Selectivity: FM/AM >65dB
SNR: FM: 63dB, AM: 53dB
Stereo sep: 55dB
Image ratio: FM: 65dB, AM: Infinity
Distortion: FM: 0.09%, AM=0.25%

Digital-centric CMOS tuner technology

Main signal processing is done by DSP.



DSP processes

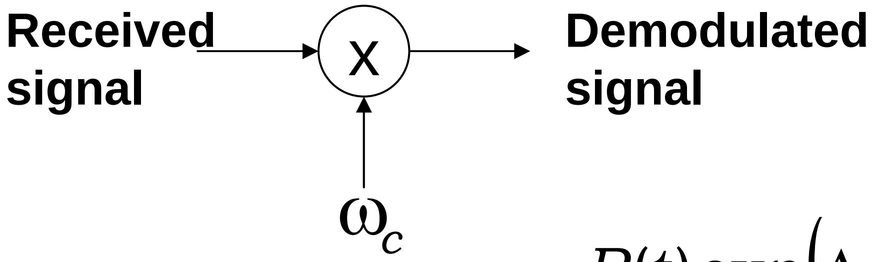
1. **AM/FM demodulations**
2. **Stereo decoder**
3. **AM mixer**
4. **Channel select filter**
5. **Support for image reject**
6. **Watch the signal revel and control gain of each stage**
7. **Parameter control and adjustment with MCU**

Demodulation of AM/FM signal

AM/ FM signals can be demodulated by simple arithmetic operations

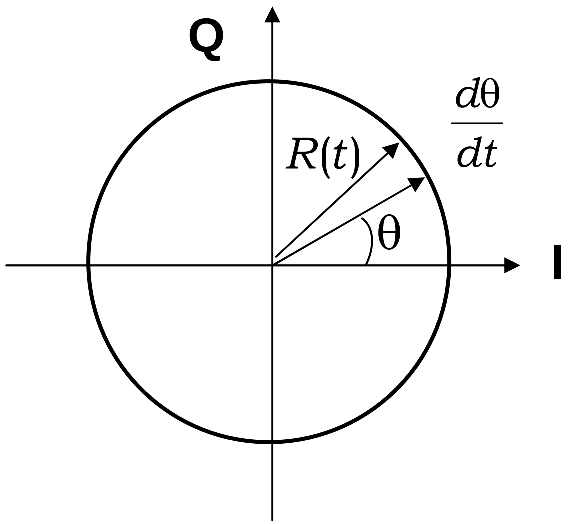
1) AM demodulation

$$\underline{\left[1+S(t)\right]\cdot\exp\left(j\omega_c t\right)}\times\underline{\exp\left(-j\omega_c t\right)}=1+S(t)$$



2) FM demodulation

$$R(t)\exp\left(\Delta j\omega t+jK_d\int m(\tau)d\tau\right)$$



$\Delta\omega$: *Frequency offset*

$R(t)$: *Amplitude variation*

$m(\tau)$: *Baseband signal to be recovered*

$$\theta=\Delta\omega t+K_d\int m(\tau)d\tau$$

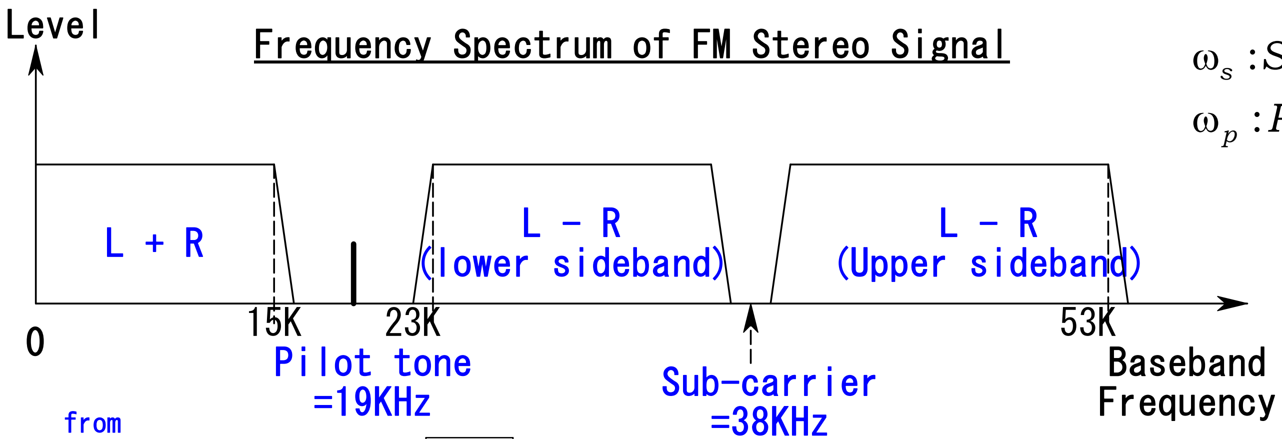
$$\boxed{\frac{d\theta}{dt}=\Delta\omega+K_d m(t)}$$

m(t) can be demodulated

Stereo decoder

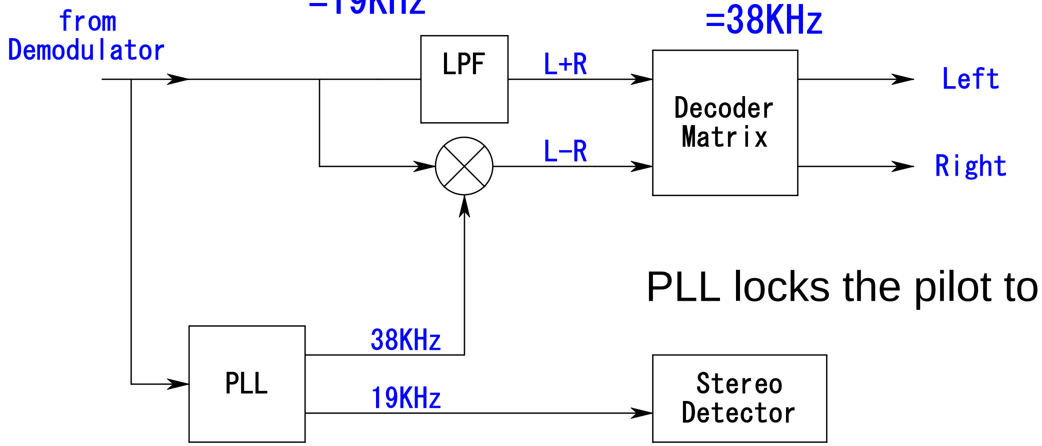
Te stereo signal can be reconstructed by numerical PLL, mixer, and filter.

$$S(t) = (L+R) + (L-R)\cos\omega_s t + K\cos\omega_p t$$



ω_s : $Sub-carrier = 38KHz$

ω_p : $Pilot\ tone = 19KHz$



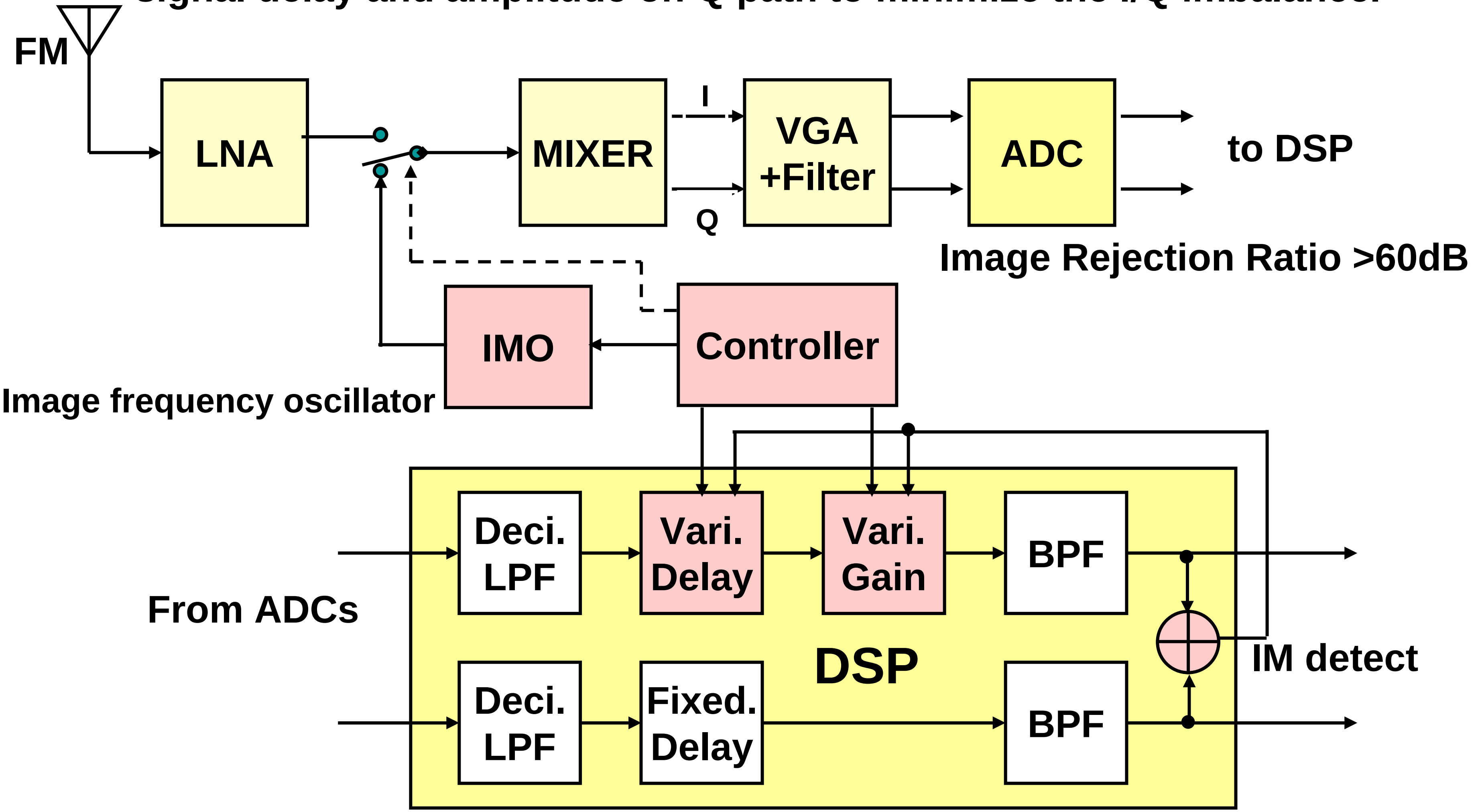
$$(L+R)+(L-R) = 2L$$

$$(L+R)-(L-R) = 2R$$

PLL locks the pilot tone and generates 38KHz for sub-carrier

Image rejection

The dummy image signal is generated by IMO and the controller controls signal delay and amplitude on Q path to minimize the I/Q imbalance.



Impact of components reduction

Reduced components	Reduction ratio	Impact on the Industry
Chip resistor	1／10 pcs or less	Components # will be reduced by more than 7 billion pcs per year.
Ceramic capacitor	1／10 pcs or less	Components # will be reduced by more than 15 billion pcs per year.
Electrolytic capacitor	1／10 ～ 1／20 pcs	In AV area estimated 3 billion pcs per year will decrease to less than 500 mil. pcs. Aluminum consumption is expected to decrease by 2 thousand ton per year.
Chip inductor	1／2 pcs or less （0～4pcs）	Components # will be less than half the # of existing pcs, but still some remain.
FM/AM Ceramic filter	0	Estimated 600 mil. pcs per year will be reduced to 0.
Varactor diode	0	In AV area, about 1.5 billion pcs per year will be reduced to 0.
PIN diode	0	In AV area, about 50 mil. pcs per year will be reduced to 0.
Intermediate-frequency transformer	0	About 1 billion pcs per year will be reduced to tens of millions pcs.
Bipolar IC for tuner	Incorporated into Full CMOS	Bipolar IC exclusive for RF is not necessary any more.
Printed board	1／6 pcs or less	
Tuner module	Unit manufacturers fix IC directly onto unit base	Tuner makers are not necessary any more.

＊Assuming that units manufactured per year are : 100 mil. units for car radios, 80 mil. units for home radios.

Feature of CMOS technology

- **Digital:**
  By Scaling theory

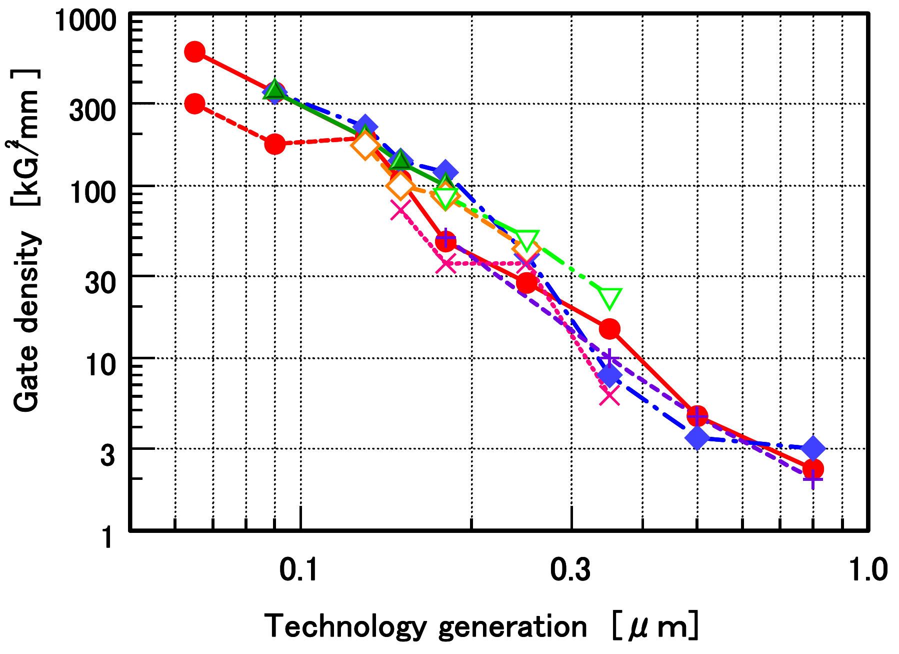
  - **Cost/transistor: 0.5x**
  - **Speed/ transistor:1.4x**
  - **Power: 0.5x**

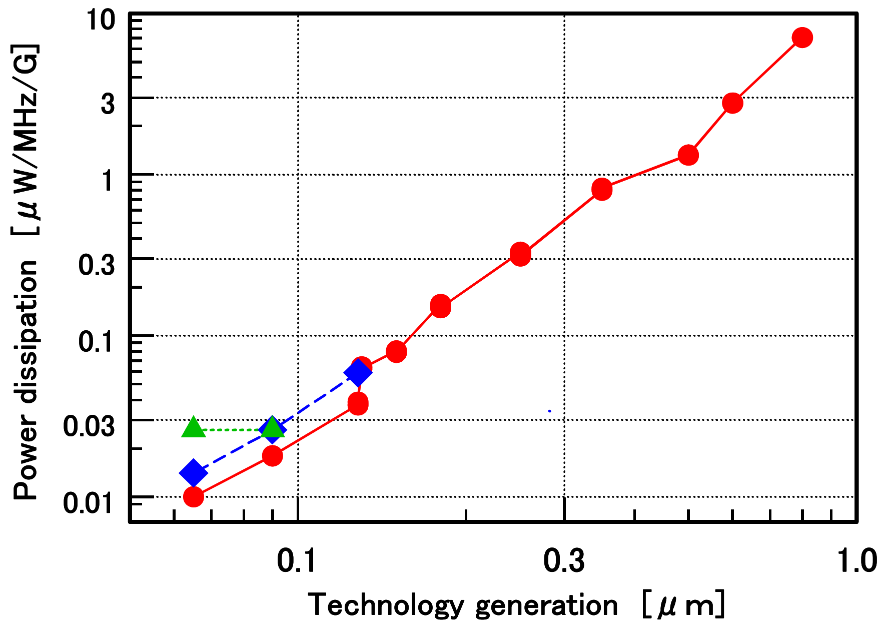
  For one technology generation advance

- **Analog:**
  - **f_T increase: 1.4x**
  - **Large mismatch, large PVT fluctuations**
  - **Low gm (1/3 vs. Bipolar)**
  - **Affected by digital noise seriously**

Integration and power dissipation trend

Integration level increases and power dissipation decreases with scaling





Matsuzawa & Okada Lab.

Feature of Analog CMOS technology

- **Pros**
  - **Can use switch and voltage controlled conductance**
  - **Smaller distortion**
  - **No carrier accumulation**
  - **Can use switched capacitor circuits**
  - **Can increase f_T by scaling**
  - **Easy use of complementally circuits**
  - **Easy integration with digital circuits**

- **Cons**
  - **Low g_m/I_{ds}**
  - **Larger mismatch voltage and 1/f noise**
  - **Lower operating voltage with scaling**
  - **Difficult to enable impedance matching**
  - **Easily affected by substrate**

Akira Matsuzawa, "Mixed Signal SoC Era," IEICE, Trans. Electron., Vol. E87-c, No. 6, pp. 867-877, June, 2004.

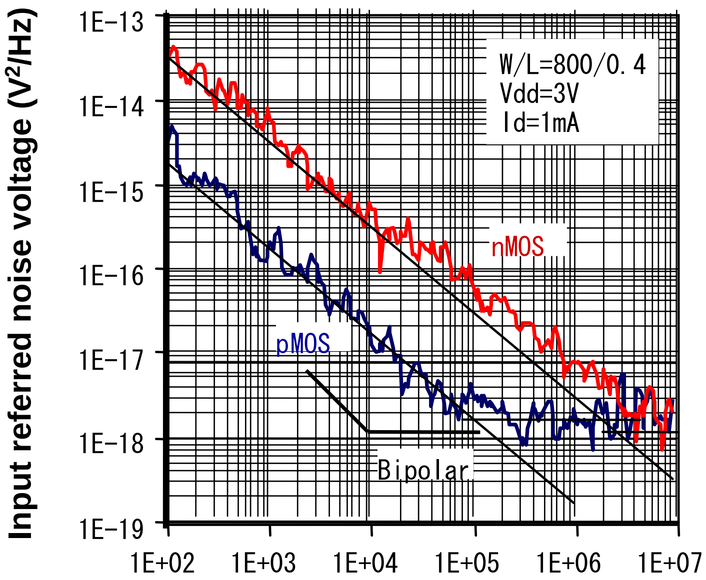
1/f noise issue in CMOS

1/f noise of MOS is much larger than that of bipolar.

For the lower 1/f noise, the larger gate area is needed.

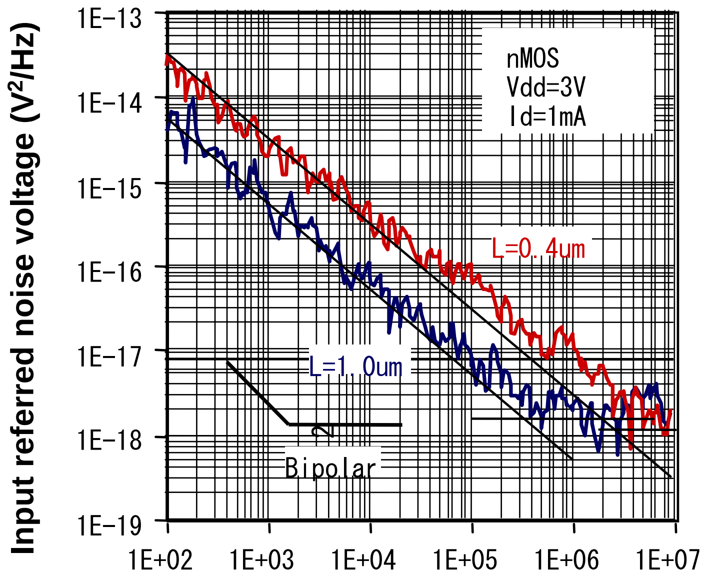
$$V_{nf}^2 = \frac{S_{vf}}{LW}\frac{\Delta f}{f}, \qquad S_{vf} \propto T_{ox}^2$$

Nch/Pch 0.4um



Frequency (Hz)

Nch 0.4um/1.0um



Frequency (Hz)

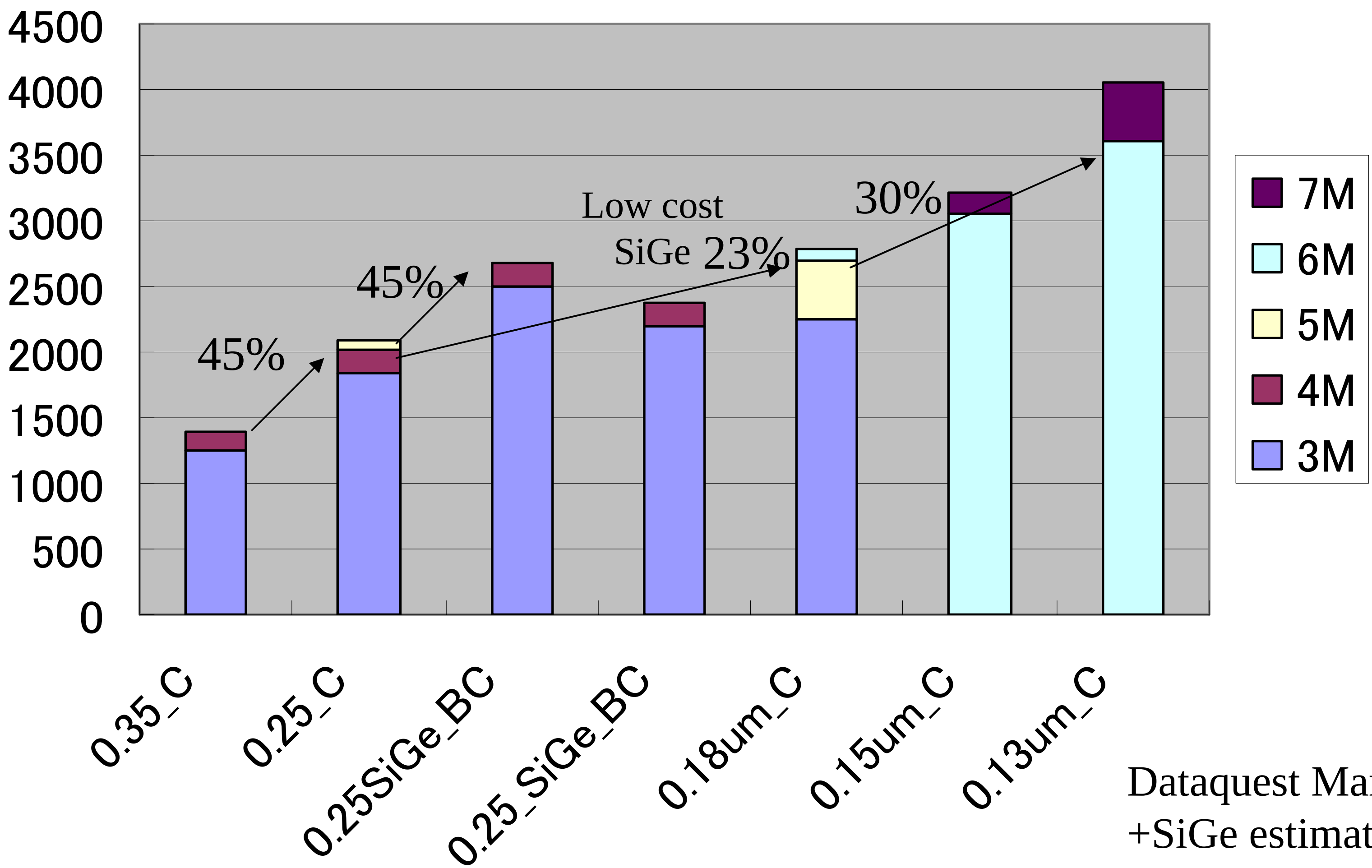
Why CMOS?

TOKYO TECH
Pursuing Excellence

- **Low cost**
  - **Must be biggest motivation**
  - **CMOS is 30-40% lower than Bi-CMOS**
- **High level system integration**
  - **CMOS is one or two generation advanced**
  - **CMOS can realize full system integration**
- **Stable supplyment and multi-foundries**
  - **Fabs for SiGe-BiCMOS are very limited.**
    → Slow price decrease and limited product capability
- **Easy to use**
  - **Universities and start-up companies can use CMOS with low usage fee, but SiGe is difficult to use such programs.**

Is CMOS cheaper?

Wafer cost of SiGe BiCMOS is 30-40% higher than CMOS at the same generation, however almost same as one generation advanced CMOS.

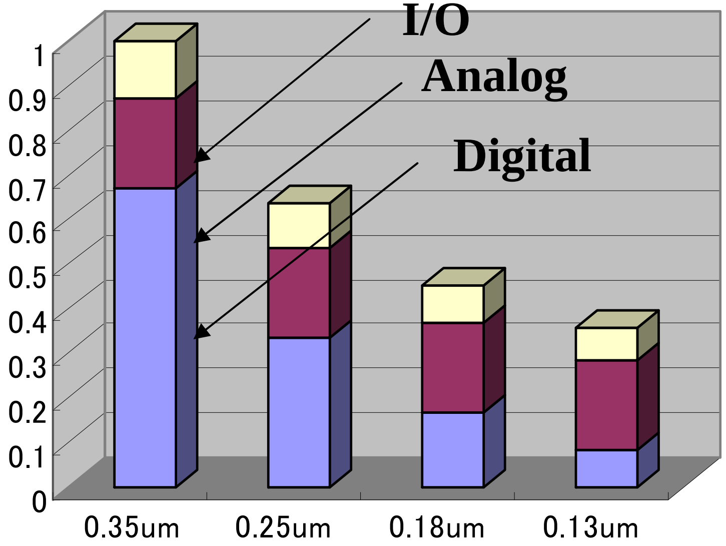


Dataquest March 2001
+SiGe estimation

Cost up issue by analog parts

Cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of cost of non-scalable analog parts.

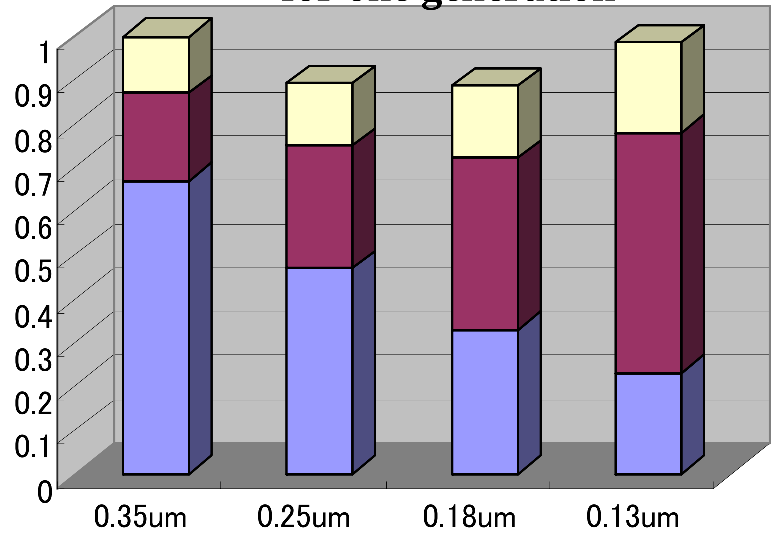
Large analog may be unacceptable.
Some analog circuits should be replaced by digital circuits



Chip area

（0.35um : 1）

Wafer cost increases 1.3x for one generation



Chip cost

Akira Matsuzawa, “RF-SoC- Expectations and Required Conditions,”
IEEE Tran. On Microwave Theory and Techniques, Vol. 50, No. 1, pp. 245-253, Jan. 2002

Technology trend in RF-CMOS LSI

Analog-centric RF CMOS will be replaced by digital-centric RF CMOS. High performance, low cost, stable and robust circuits, no or less external components, no adjustment points, and high testability are the keys. DSP and ADC will play important role.

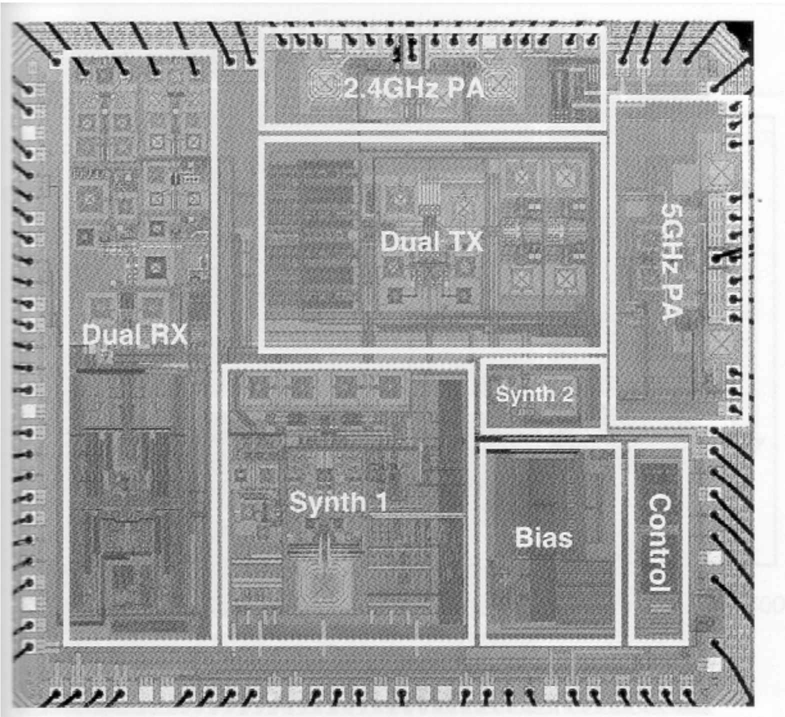
Analog-centric → **Digital-centric**

	Analog-centric	Digital-centric
Signal processing	Analog circuits Analog processing +External component	DSP+ADC + Small and robust analog ckts.
Adjustment	External	Digital on chip, no external
External components	Large #	No or less

Technology trend in RF CMOS LSI

Analog centric RF CMOS will be replaced by digital centric RF CMOS.

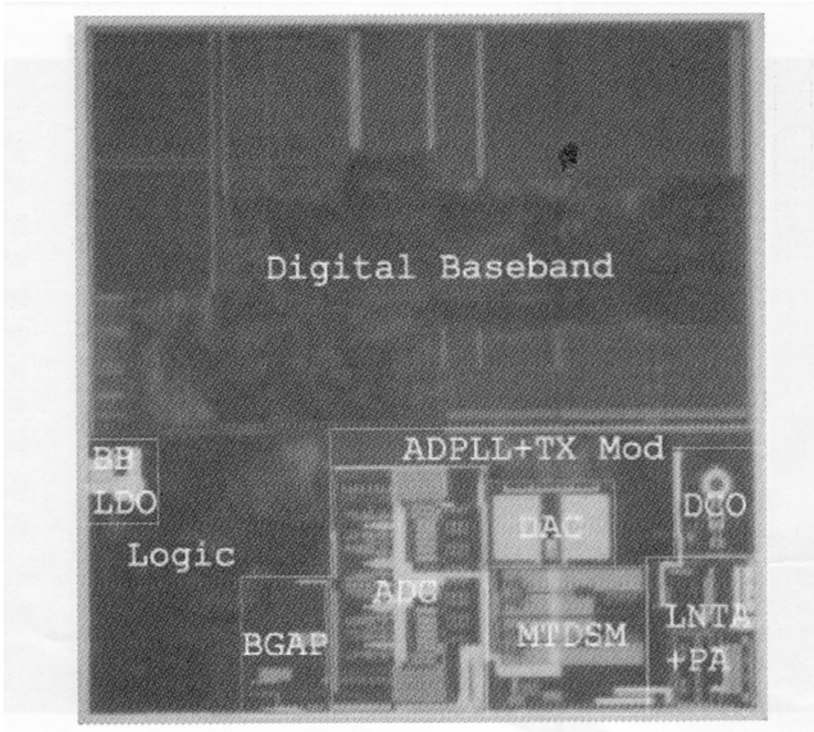
Wireless LAN, 802.11 a/b/g
0.25um, 2.5V, 23mm^2, 5GHz



5.4.7: Die micrograph.

M. Zargari (Atheros), et al., ISSCC 2004, pp.96

Discrete-time Bluetooth
0.13um, 1.5V, 2.4GHz



gure 15.1.7: Die micrograph of the single-chip Bluetooth transceiver.

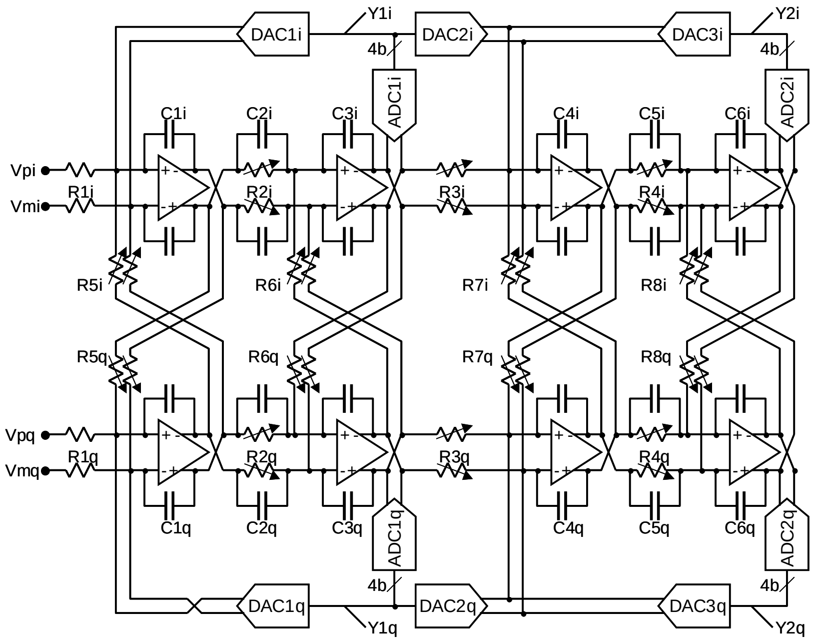
K. Muhammad (TI), et al., ISSCC2004, pp.268

Wide-band delta-sigma ADC

Wide band and high dynamic range delta-sigma ADC is the key for digital centric systems

90nm CMOS、BW=20MHz, DR(=SNR)=77dB, 50mmW, FoM=200fJ/conv.

L. J. Breems, et., al.
"A 56mW CT Quadrature Cascaded SD Modulator with 77dB in a Near aero-IF 20MHz Band.
ISSCC 2007, pp. 238-239.



Technology	90nm CMOS, 1P6M
Supply voltage	1.2V
Architecture	CT quadrature cascaded ΣΔ modulator (2-2, 4b)
Sampling frequency	340MHz
Bandwidth	20MHz @ 10.5MHz IF
Max. input voltage	1Vp (differential)
Dynamic range*	77dB (97dB @ 200kHz, 115dB @ 3kHz)
Peak SNR / SNDR*	71dB / 69dB
Image rejection	>55dB (for -1MHz input tone)
Active chip area	0.5mm^2
Power consumption	50mW (analog), 6mW (digital)
Figure-of-merit (FOM)	0.2pJ/conv. (FOM=P/(2^enob*2*BW))

(*1MHz input signal, signal bandwidth is 20MHz)

Trend of delta-sigma ADC

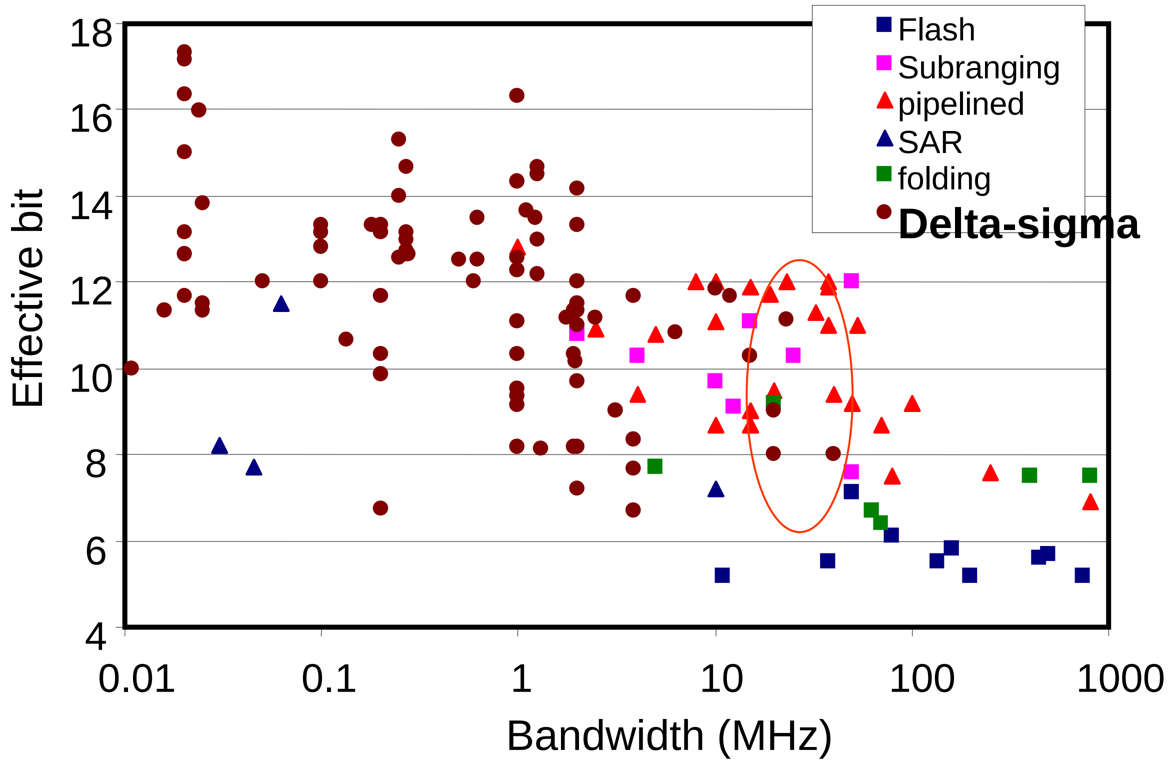
The bandwidth of sigma-delta ADCs has been increased up to 20MHz with effective resolution of about 12 bit.

Nyquist ADC:

$$SNR \propto CV_{sig}^2$$

Delta-sigma ADC:

$$SNR \propto CV_{sig}^2 \cdot M^{\alpha}$$



Conclusion

- **Radio tuners have not been replaced by CMOS technology in contrast to many other wireless systems; cellular phones and wireless LANs have been replaced by CMOS.**
  - Low frequency:
    - External large L and C, Filters
    - 1/f noise
  - High dynamic range:
    - External sharp and fine tuning filters
- **Analog-centric CMOS technology is not effective**
  - No attractive performance and affected by PVT fluctuation seriously.
  - Cost increase for further technology scaling
  - Still need large # of external components and adjusting points
- **Digital-centric CMOS technology must be right way**
  - High performance and very robust against PVT fluctuations
  - Further performance increase and cost reduction are expected by using more scaled technology
  - No or less external components and no adjustment points