INVITED PAPER *Special Section on Low-Power, High-Speed LSIs and Related Technologies*

Design Challenges of Analog-to-Digital Converters in Nanoscale CMOS

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SUMMARY This paper discusses issues in the design of analog-to-digital converters (ADCs) in nanoscale CMOS and introduces some experimental designs incorporating techniques to solve these issues. Technology scaling increases the maximum conversion rate, but it decreases the gain and the SNR. To maintain a high SNR level despite the low-voltage operation, the power consumption needs to be increased. Because of lowered supply voltages, the design of circuits based on operational amplifiers (OpAmps) has become more difficult. Designs without OpAmps have therefore received more attention. One way of realizing low-voltage pipeline ADCs is by using comparator-controlled current sources, instead of conventional OpAmps. Furthermore, successive approximation ADCs and sub-ranging ADCs do not require OpAmps and are therefore suitable for low-voltage operation. ADC designers are now searching for suitable architectures for future nanoscale CMOS processes.

key words: *analog circuits, integrated circuits, analog-to-digital converter, CMOS, low-power operation, low-voltage operation, technology scaling*

1. Introduction

Expectations on the performance of analog-to-digital converters (ADCs) have been continuously increasing along with the progress of digital systems. The performance of ADCs will determine digital systems' basic performance, such as data-rate, sensitivity, signal dynamic range, bit error rate, and power consumption. To realize a system with the lowest cost-per-performance, ADCs should be embedded in a system-on-a-chip (SoC). Unlike the progress of digital systems, the progress of analog systems can not be guaranteed with the scaling of the technology. This paper discusses the relationship between CMOS technology scaling and the performance of ADCs, as well as recent challenges in the design of ADCs.

2. Technology Scaling and Analog Performance

Recently, technology scaling has enabled the use of CMOS circuits in radio frequency applications, a domain previously reigned completely by bipolar transistors.

The peak cutoff frequency of MOS transistor, f_{Tmax}, is approximated by

$$f_{T\max} \approx \frac{v_{sat}}{2\pi L}, \tag{1}$$

where v_{sat} is the saturation carrier velocity and L is the channel length of the MOS transistor. The cutoff frequency is inversely proportional to the channel length and will reach about 200 GHz in a 65 nm technology. However, the most serious issue is currently the lowering of the operating voltage, which will be even more critical in future processes. According to the recent ITRS technology roadmap, the maximum operating voltage of around 1 V will be extended to the 45 nm technology [1]. This value is higher than that of the past ITRS technology roadmap, however, the realization of high SNR analog circuits is still difficult.

The SNR of a differential sample and hold circuit is

$$SNR = \frac{CV_{pp}^2}{4kT}, \tag{2}$$

where C is the sampling capacitor, V_{pp} the maximum differential voltage of a sinusoidal signal, k Boltzmann's constant, and T the absolute temperature. Because the SNR decreases with the decrease of the signal amplitude, a larger sampling capacitance is needed to maintain the same SNR at a lower operating voltage. This, however, leads to an increase of the power consumption or a decrease of the signal bandwidth.

The "headroom" issue in a low-voltage environment limits the number of transistors that can be stacked, and it also limits the gain that can be achieved.

Figure 1 shows a conventional operational amplifier (OpAmp) for pipeline ADCs. A four-transistor stack is needed to form a cascode circuit which is inevitable for realizing a high voltage gain. Furthermore, gain-boosting amplifiers are needed to further increase the gain.

The minimum drain-to-source voltage V_{ds} that keeps the transistor in the saturation region is V_{eff} $(= V_{gs} - V_T)$ and is conventionally fixed between 0.15 V and 0.2 V. The output

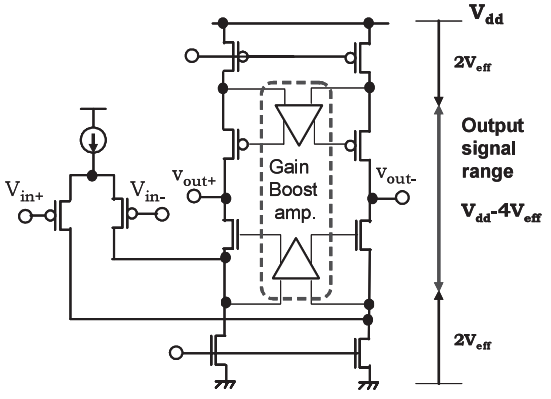

Fig. 1 Conventional OpAmp for a pipeline ADC.

Manuscript received October 19, 2006.

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DOI: 10.1093/ietele/e90–c.4.779

signal swing then amounts to $V_{dd} - 4\,V_{eff} \approx V_{dd} - 0.7$V.

Therefore, if we use an operating voltage of 1.0 V, the output signal swing is only 0.3 V, which is an unacceptably low signal swing for many applications. The use of high-gain OpAmps for scaled low-voltage devices becomes infeasible.

Additionally, with the lowering of the supply voltage, MOS switches will cause serious problems: CMOS switches have their source node connected to the input terminal and the on-resistance takes on the maximum value when the signal voltage is about half the operating voltage.

The effective gate voltage is $V_{eff} = \frac{V_{dd}}{2} - V_T - \Delta V_T$, where ΔV_T is the increase of the threshold voltage due to the back-gate effect. Thus, the effective gate voltage decreases rapidly along with technology scaling and the switch will not be turned on at low-voltage operation. Some gate-boosting techniques or back-gate control techniques will improve this issue, however, switches will remain the bottleneck for low-voltage operation.

Another issue is the reduction of the amplifier's gain caused by the reduction of the drain resistance. Figure 2 shows a plot of the Early voltage, V_A, of an NMOS transistor versus the drain-to-source voltage, V_{ds}, for several design rules and with the channel length being 10% larger than the minimum channel length. The drain resistance, r_{ds}, can be expressed as

$$r_{ds} = \frac{V_A}{I_{ds}}. \tag{3}$$

The intrinsic voltage gain, G_i, is

$$G_i = g_m \cdot r_{ds} = \frac{2\,V_A}{V_{eff}}, \tag{4}$$

where g_m is the transconductance and V_{eff} is the effective gate voltage. Therefore, a higher V_A would be required to obtain a higher gain; however, V_A decreases with transistor scaling. The maximum intrinsic gain of a 90 nm NMOS transistor is approximately 10, which is about three times lower than that of a 350 nm NMOS transistor. Furthermore, scaled devices require low-voltage operation and this results in the decrease of V_{ds} down to V_{eff}. At this voltage, V_A is about 1.0 V, independent of the design rule due to the imprecise boundary between the saturation region and the linear region. The design of high-gain amplifiers becomes more difficult with future CMOS generations.

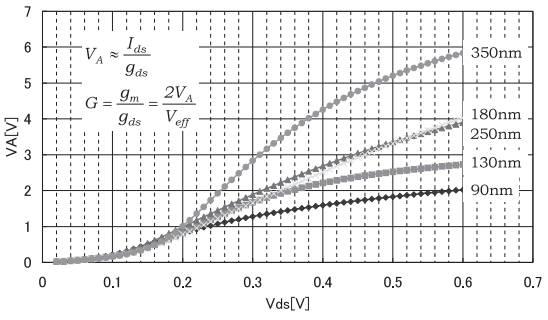

Fig. 2 V_A vs. V_{ds} for several design rules.

3. Technology Scaling and ADC Performance

Future cellular phone systems, as well as wireless LAN systems, require ADCs with conversion frequencies of several hundred MHz and resolutions of 10 bit to 14 bit. A strong candidate fulfilling such specifications is the pipeline ADC incorporating comparators and accurate switched-capacitor amplifiers.

Figure 3 shows plots of the conversion frequency versus the power consumption of previously published 10 bit, 12 bit, and 14 bit pipeline ADCs and, for comparison, some sigma-delta ADCs. Higher resolution ADCs generally consume more power than ADCs with lower resolution, and their maximum conversion frequency is lower. For 10 bit pipeline ADCs, the maximum conversion frequency is about 200 MHz and the lowest power consumption normalized by the conversion frequency is about 0.3 mW/MHz. Since ADCs are the most important analog core blocks for future wireless systems, this paper will discuss their fundamental performance limitation and make estimates with respect to the technology scaling.

A pipeline ADC consists of a cascade of unit amplifiers, of which one's equivalent circuit is shown in Fig. 4. It can be modeled with an input sampling capacitor, C_s, a feedback sampling capacitor, C_f, a load sampling capacitor, C_{OL}, which is a parallel connection of an input sampling ca-

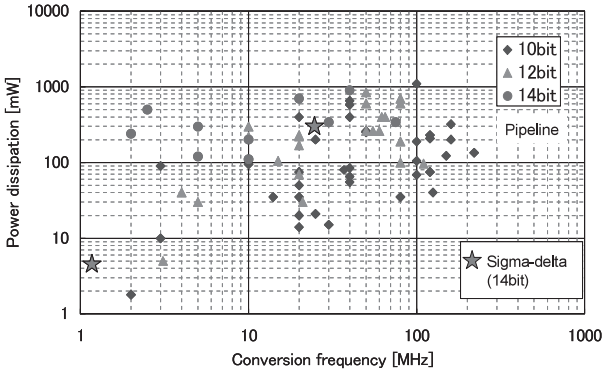

Fig. 3 Power dissipation vs. conversion frequency of previously published 10 bit, 12 bit, and 14 bit ADCs.

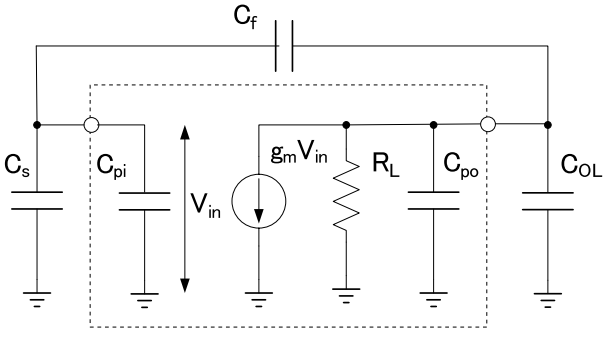

Fig. 4 Equivalent circuit model for a pipeline ADC.

pacitor and a feedback sampling capacitor in the next stage, a parasitic input capacitor, C_{pi}, a parasitic output capacitor, C_{po}, and the transconductance g_m [2]. Since in a conventional flip-around switched-capacitor circuit the input sampling capacitance, C_s, is the same as the feedback sampling capacitance, C_f, and the capacitances in the following stage are about half, the sampling capacitance, C_o, can represent these capacitances, i.e., C_s, C_f, and C_{OL}.

The closed-loop bandwidth can be derived as

$$GBW_{\_close} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)}. \quad (5)$$

The conversion frequency of the ADC is

$$f_c \approx \frac{3 \cdot GBW_{close}}{N}, \quad (6)$$

with N being the resolution. Thus, a higher closed-loop bandwidth, GBW_{close}, is needed for the higher conversion frequency.

The parasitic input and output capacitances, C_{pi} and C_{po}, depend on the design rule; for a constant V_{eff}, they are proportional to the operating current. If also the channel length, L, is kept constant, C_{pi} and C_{po} are additionally proportional to the drain current, I_{ds}, as is shown in the following equation.

$$C_{pi}, C_{po} \propto W \approx \frac{2L}{\mu C_{ox} V_{eff}^2} I_{ds}. \quad (7)$$

Thus, $C_{pi} = \alpha_{pi} \cdot I_{ds}$ and $C_{po} = \alpha_{po} \cdot I_{ds}$. With $g_m = \frac{2I_{ds}}{V_{eff}}$, Eq. (5) can be modified as follows:

$$GBW_{\_close} = \frac{I_{ds}}{2\pi C_o V_{eff}} \cdot \frac{1}{\left(2+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi} I_{ds}}{C_o}\right)}. \quad (8)$$

The coefficients of the parasitic input and output capacitances, α_{pi} and α_{po}, and the sampling capacitance, C_o, are decreasing with the design rule for an ADC with 10 bit resolution, as is shown in Table 1. These capacitances have been obtained by SPICE simulation for conventional foundry processes under the assumption that V_{eff} = 0.175 V, and the channel length being 1.1 times the minimum channel length. The coefficients are halved with every new technology generation.

Figure 5 shows the estimated maximum conversion frequency for 8 to 14 bit ADCs as a function of the sink current of the input MOS transistor in the first stage's OpAmp for the following design rules: 350 nm, 250 nm, 180 nm, 130 nm, and 90 nm.

Table 1 Design rules, capacitances, and signal swing.

DR (nm)	α_{pi} (fF/mA)	α_{po} (fF/mA)	C_o (fF@10b)	V_{pp} (V)
350	1034	892	20.5	5.2
250	662	832	43	3.6
180	475	340	114	2.2
130	249	168	216	1.6
90	94	95	553	1.0

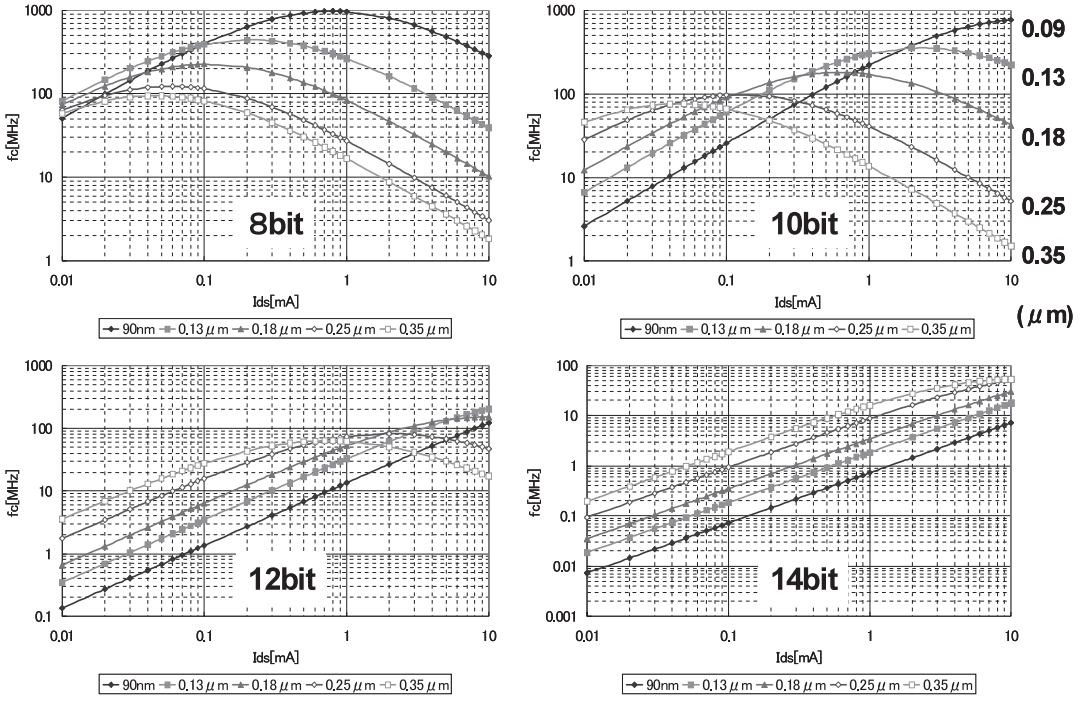

Fig. 5 Conversion frequency vs. operating current in the input stage for several resolutions and design rules.

The maximum differential signal voltage has been determined for each design rule by the voltage condition shown in Fig. 1.

As the input-referred thermal noise should be equal or less than the quantization noise to attain an SNR that is 3 dB lower than the ideal value, the following equation holds:

$$\frac{8 \cdot kT}{C_o} \leq \frac{V_{pp}^2}{12 \cdot 2^{2N}}, \tag{9}$$

C_o is obtained as follows:

$$C_o(\,pF) \geq 5.28 \times 10^{-7} \times \left(\frac{2^N}{V_{pp}}\right)^2 \tag{10}$$

The characteristic curve is convex and it describes the maximum conversion frequency for each sink current. In the region of the current being less than this value, the conversion frequency increases with an increase of the sink current; however, in the region of the current being larger than this value, the conversion frequency decreases with an increase of the sink current.

There are two reasons why this characteristic is exhibited. In the low-current region, g_m is proportional to the sink current, and the parasitic capacitances are smaller than the sampling capacitance. At around the peak, at least one of the parasitic capacitances becomes of the same order as the sampling capacitance. In the region of the current being larger than that value, both parasitic capacitances become larger than the sampling capacitance and the conversion frequency will decrease with an increase of the sink current.

The estimated performance curves exhibit interesting results in terms of the relationship between the ADC performance and the design rules. For the ADC with 8 bit resolution, the fastest realization in the low-current region can be realized in 130 nm CMOS, whereas 90 nm CMOS attains the overall highest conversion frequency. For ADCs with a resolution of 10 bit, 350 nm CMOS is faster than the other processes in the ultra-low current region. However, with an increase of the sink current, the processes with smaller design rules achieve a higher conversion frequency. In terms of both conversion speed and current consumption, the 350 nm CMOS process shows the best performance for ADCs with 12 bit and 14 bit resolution. For ADCs with a lower resolution, the sampling capacitance is smaller, and the transistors with smaller design rule can reduce the parasitic capacitances. However, in order to achieve a high resolution at a small signal swing, the sampling capacitance should be increased to keep the SNR high when using the transistors with small design rule. In this case, reducing the parasitic capacitances is not effective anymore.

Furthermore, pipeline ADCs with a higher resolution require a higher OpAmp gain. As the gain error, G_{error}, should be less than 1/4 LSB,

$$G_{error} \cong \frac{1}{G\beta} \leq \frac{1}{2^N}, \tag{11}$$

the required OpAmp gain needs to be

$$G\,(\mathrm{dB}) > 6N + 10, \tag{12}$$

where N is the ADC's resolution, G the open-loop gain, and β the feedback factor. The OpAmp of a 14 bit ADC, for example, requires a gain of at least 94 dB, a value which is very demanding to achieve in a 90 nm CMOS technology.

4. Design Challenges for High-Speed ADCs

Further performance improvements for pipeline ADCs seem very difficult, especially for high resolution ADCs. Several analog operations can be realized effectively with OpAmps, in particular analog pipeline operation. Moreover, the requirements on the mismatch of comparators, the essential part of an ADC, can become more relaxed. However, it becomes increasingly difficult to realize high performance OpAmps; due to technology scaling, gain, as well as signal dynamic range, decrease monotonically. Many chip designers are now looking for suitable conversion architectures for the nanoscale CMOS generation. The basic idea for this new design challenge is to remove the OpAmp. I will now present some development examples for future high speed ADCs.

4.1 Pipeline ADCs Using Comparator-Controlled Current Sources

One idea is to realize the virtual ground, which is an essential function of operational amplifiers, by a comparator-controlled current source as shown in Fig. 6 [3].

The comparator controls the current source as follows: if the node voltage V_x is negative, the output of the comparator activates the current source I_1 to charge the capacitors, and the node voltage V_x increases. As soon as the node voltage V_x becomes positive, the output voltage of the comparator will change the polarity to turn off the current. However, some voltage will appear on V_x due to the time delay of the circuit. A small current source I_2 should be activated and V_x will reach an ideal voltage. Despite this measure, a very small voltage will still remain. However, this residual voltage can be treated as an offset voltage that does not affect the conversion linearity in a pipeline ADC.

Comparators can use lower operating voltages than OpAmps, even 0.5 V operation is possible. The circuit con-

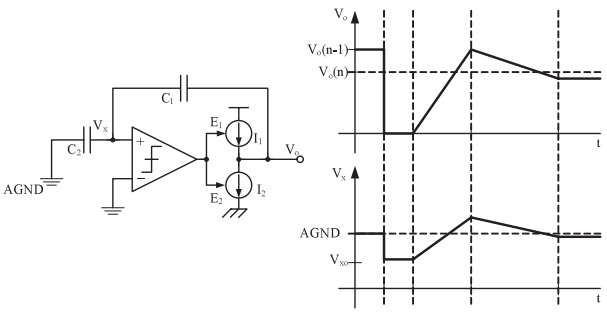

Fig. 6 Comparator-controlled current source.

struction of this comparator-controlled current source, however, is just the same as for conventional OpAmps, if some non-linear functions, such as hysteresis or latching action are not introduced.

A 10 bit, 8 MHz pipeline ADC has been developed by using comparator-controlled current sources. Its power consumption is 2.5 mW, and the resulting power/conversion frequency ratio is among the lowest, but not remarkably low [3]. Further optimizations leading to a better performance are however expected.

4.2 Successive Approximation ADCs

Another candidate is the successive approximation ADC (SA ADC) shown in Fig. 7. The required analog operations can be realized with only capacitors, switches, and a small number of comparators. The quiescent current, which is needed for the comparator, is very small or can be designed to be zero. Thus, the power consumption is, like in digital circuits, only determined by dynamic currents. The signal swing can be set larger than that of OpAmp-based designs; even full-swing operation is possible and the capacitance can be decreased. Thus, low power operation is expected.

The biggest issue is the operating speed; parallel schemes can, however, address this issue.

Figure 8 shows a 6 bit SA ADC array. Eight interleaved SA ADCs realize high conversion rates of 600 MHz in a 90 nm CMOS technology [4]. Simple circuits are suitable for scaled devices and can also benefit from technology scaling. Power consumption is only 10 mW, resulting in a low power/conversion frequency ratio of 17 μW/MHz, which is about one order of magnitude lower than that of conventional flash architectures.

Asynchronous operation, as presented in Fig. 9, is another technique to increase the conversion frequency [5]. The required settling time for each conversion step is different; conventionally, the required settling times for the MSB and MSB-1 bits are higher. Conventional SA ADCs use synchronous clocks with the period determined by the settling time required for the MSB conversion. This results in a non-optimal conversion frequency. Asynchronous operation with periods optimized for each conversion step, leads to higher conversion rates.

Furthermore, the redundant architecture using a radix number of 1.8, as shown in Fig. 10, can relax the required settling time. The ladder connection of capacitances decreases the total capacitance. In this figure, the following assumptions are made:

$$radix = 1 + \frac{\beta}{\alpha} \tag{13a}$$

$$\beta = 1 + \alpha \,||\beta \tag{13b}$$

This reduction of capacitance effectively increases the input signal bandwidth as well as the conversion rate and it reduces the power consumption.

The resolution is 6 bit, however, a high conversion rate of 600 MHz and very low power consumption of 5.3 mW have been measured with a 130 nm CMOS technology [5].

The SA ADC architecture is very conventional and it has been used for slow and low-power ADCs. However,

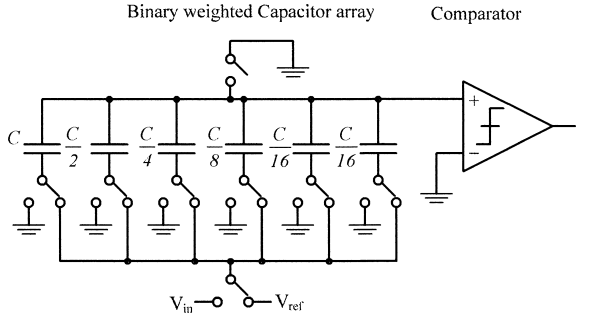

Fig. 7 Successive approximation ADC.

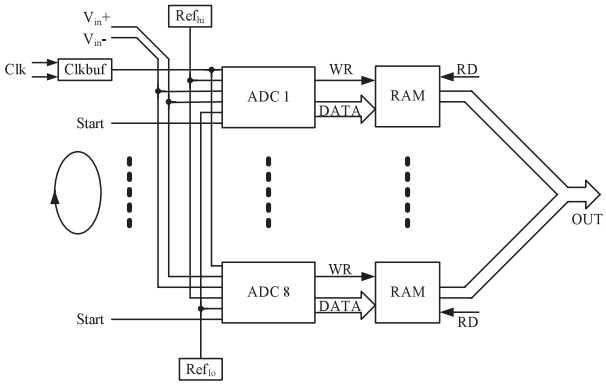

Fig. 8 Interleaved SAR architecture.

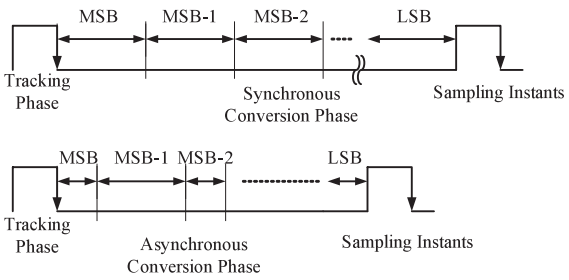

Fig. 9 Asynchronous operation.

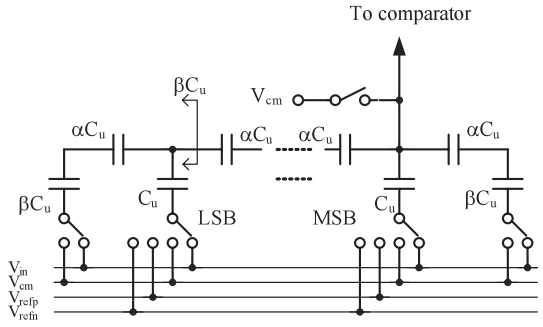

Fig. 10 Redundant architecture.

these design experiments revealed that this architecture has a high potential for low-power yet high-speed ADCs, and that this architecture is suitable for scaled CMOS technologies. Further design efforts will be made and substantial advances can be expected.

4.3 Sub-Ranging ADCs

Today, several technology revivals can be seen: some neglected designs show favorable characteristics in a new technology. The SAR ADC was one example, another one is the sub-ranging ADC shown in Fig. 11. Sub-ranging ADCs were one of the major converter architectures for video-rate applications from 1985 to 1995 [6]. However, in the past 10 years, pipeline ADCs have taken over this domain. The main reasons are that pipeline ADCs do not require low offset mismatch voltages for comparators and OpAmps, and they show a high scalability in conversion speed and resolution. Basically, the OpAmp design determines almost the whole ADC performance, i.e., circuit designers can concentrate mainly on the OpAmp design. In contrast, sub-ranging ADCs require very small mismatch voltages for the comparators. Furthermore, the design of the reference ladder and the switches greatly affect the ADC's performance. However, technology scaling decreases the time constant of reference circuits and comparators. Moreover, some design techniques can reduce the mismatch voltage of the comparators.

Figure 12 shows a proposed comparator that can reduce the offset-mismatch voltage by using a positive feedback technique [7]. The offset compensation error voltage is inversely proportional to the open-loop gain. The conventional open-loop gain of a single-stage amplifier without cascodes ranges from 20 dB to 30 dB, which is not high enough. Capacitor C_1 is introduced to form a positive-feedback circuit, and the positive-feedback ratio can be determined by C_1/C_2. A gain that is 12 times higher has been obtained by using this positive-feedback technique. A 12 bit ADC using this approach has been developed in 90 nm CMOS; the power consumption of 30 mW at 50 MHz conversion frequency, resulting in a power/conversion frequency ratio of 0.6 mW/MHz, is almost half of previously reported ratios. Furthermore, low-voltage operation of 1 V has been realized. This result demonstrates that the removal of OpAmps is an effective measure to reduce the operating voltage and a suitable method for designing circuits with nanoscale CMOS technologies.

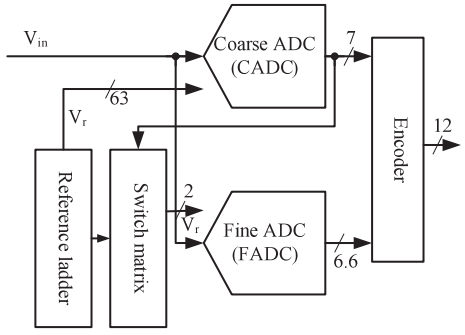

Fig. 11 Sub-ranging ADC.

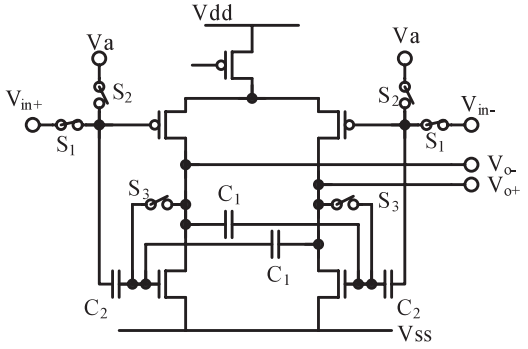

Fig. 12 Comparator with positive feedback.

5. Conclusion

Technology scaling increases the conversion rate, but it decreases the gain and the SNR. Because the SNR decreases along with the decrease of the signal amplitude, a larger sampling capacitance is needed to maintain the same SNR at a lower operating voltage. This, however, leads to an increase of the power consumption or a decrease of the signal bandwidth.

OpAmp-based designs become difficult and more attention is paid to non-OpAmp based designs in modern nanoscale CMOS technologies. Comparator-controlled current sources instead of conventional OpAmps are one possible candidate. Other candidates that do not require OpAmps and that are suitable for low-voltage operation are successive approximation ADCs and sub-ranging ADCs. ADC designers are now looking for suitable ADC architectures for nanoscale CMOS generations and some technology revivals have occurred.

Acknowledgments

The author thanks Mr. M. Miyahara, Dr. T. Kurashina, and Dr. M. Frey for useful discussions and for their technical support.

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