PAPER Special Section on Low-Power, High-Speed LSIs and Related Technologies

Analysis and Design of Direct Reference Feed-Forward Compensation for Fast-Settling All-Digital Phase-Locked Loop

Win CHAIVIPAS[†a)], ***Nonmember and*** **Akira MATSUZAWA**[†], ***Member***

SUMMARY A method for shortening of the settling time in all digital phase-locked loops is proposed. The method utilizes self monitoring to obtain the parameters necessary for feed-forward compensation. Analysis shows that by employing this technique both fast settling and good stability can be achieved simultaneously. Matlab and Verilog-AMS simulation shows that typical settling speed can be reduced to less than one tenth compared to a system without the feed-forward compensation, by merely employing the feed-forward compensation system. Further more a design example shows that this settling time can be decreased further to less than one fifteenth through design considerations when compared to a speed optimized phase-locked loop design system without direct reference feed-forward compensation.

key words: *all-digital phase locked loop, feed-forward, fast settling, frequency synthesizer*

1. Introduction

Phase-locked loops (PLL) are a standard choice when designing frequency synthesizers for wireless communication because of its ability to synthesize accurate frequency reference, its relatively low phase noise, and it's ability to allow switching characteristics of frequencies which are non-integer multiples of the reference frequency.

More recently all-digital phase locked loops (ADPLL) were reported which are capable of generating gigahertz level frequency references with low enough phase noise for wireless standards [1], [2]. However, weather dealing with all-digital phase-locked loops, or the traditional charge pump type, all phase-locked loops face a fundamental trade-off between the phase-noise of the synthesized frequency; it's settling characteristic, and the system's stability. Often, settling speed is traded for a lower phase noise and greater stability of the system. This can be problematic for systems which need fast frequency switching such as frequency hopping systems.

In this paper a technique for the speed-up of the frequency-synthesizer's settling based on direct feed-forward compensation of the input reference is proposed for all-digital phase locked loop systems. Key analysis will also be shown as to how this technique can relax the design trade-offs often faced in phase-locked loop based frequency synthesizer design between the system's stability and settling speed.

Manuscript received August 19, 2006.
Manuscript revised November 7, 2006.

[†]The authors are with the Department Physical Electronics, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.
a) E-mail: win_chaivipas@ssc.pe.titech.ac.jp

DOI: 10.1093/ietele/e90–c.4.793

Throughout this analysis, the terms voltage controlled oscillator (VCO) and digital controlled oscillator (DCO) are used almost interchangeably as they perform the same function in the traditional PLL and ADPLL and are the same from the system perspective. Care should be taken, however, to notice that while the VCO is controlled by voltage, DCO is controlled by input digital code.

2. Common Speed Enhancement Techniques

One of the most often studied means to speed up the PLL's settling time concerns special design or adjustment of the PLL's loop characteristics. Employment of feed-forward loop filters, or increases of charge pump current by adding multiple parallel charge-pumps are some examples. One typical method is to dynamically adjust the PLL's loop bandwidth [3], [4], either from the loop filer directly or by changing the gain of a certain element in the system such as the charge-pump. The main idea of this method is to adjust the PLL's loop bandwidth by adjusting the loop filter's bandwidth dynamically as shown in Fig. 1.

This system monitors the PLL's loop settling behavior, allowing a wider bandwidth when a frequency change has occurred. With a wider bandwidth the signal output from the loop filter allows faster change of the VCO's controlling voltage which speeds up settling. The loop's bandwidth is gradually decreased to allow better filtering of the VCO's controlling voltage to reduce the phase noise as the loop settles. The disadvantage of this system, or any which changes the loop's parameters, is the added difficulty in balancing the settling speed and stability of the system.

The system must be designed such that it is stable over a wide range of loop filter's bandwidth, allowing for error in the prediction of the loop's parameters and VCO gain in the case of bandwidth adjustment systems. Failing to do so will cause system instability. Other methods proposed the use of a non-linear element in the loop's filter [5], or using a binary search algorithm [6].

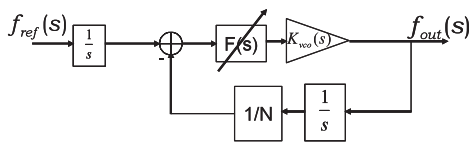


Fig. 1 Loop Bandwidth adjustment for faster settling.

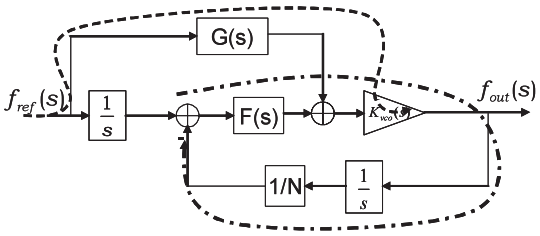


Fig. 2 Signal flow of a feed-forward PLL system.

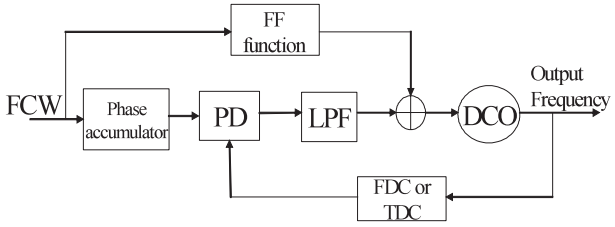


Fig. 3 Simplified block diagram of feed-forward compensated ADPLL.

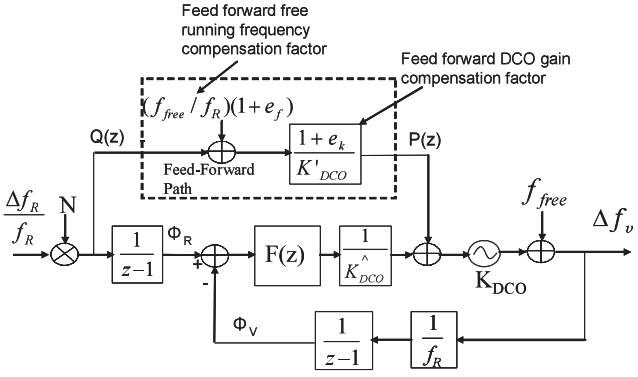


Fig. 4 Feed-forward compensated ADPLL mathematical model.

3. Direct Reference Feed-Forwarding

3.1 General Idea of Feed-Forward PLL

The idea of the feed-forward compensation is to, rather than attempting to adjust the loop-filter's characteristics, add a prediction signal directly from the reference into the VCO or DCO (digital controlled oscillator), bypassing the loop filter completely. This is shown in Fig. 2.

As seen from Fig. 2 adding a feed-forward path allows the signal to flow through an extra path when a frequency change has occurred. This is done while minimizing disturbance to the signal in the feed-back path.

It should be mentioned that although feed-forward systems are not new, they have not found much interest in phase-locked loop systems because of the difficulty and often impracticality of feed-forwarding a frequency value in the traditional charge-pump based synthesizers. The other only feed-forward architecture that the author is aware of for PLL based frequency synthesizers is that of Ref. [7]. The method presented however is impractical as it proposes two feed-forward signals to adjust both the divider and feed-forward signal to the VCO, in addition to the need to prefabricate the VCO for frequency measurement.

3.2 Proposed Feed-Forward Compensation

The proposed feed-forward compensation system is shown in Fig. 3. Although the system shown in the diagram is based on the phase-domain all digital phase-locked loop proposed in [2], it generally applies to any type of all-digital phase-locked loop.

Note that one major difference between the system in Fig. 2 and Fig. 3, is that the frequency divider $(1/N)$ is not in the feed-back path in Fig. 3 as in Fig. 2, and is instead replaced by a digital reference multiplier (N) at the reference input as shown in Fig. 4. In this figure FF function, PD, LPF and DCO refers to the feed-forward transfer function, digital phase detector (arithmetic adder), digital low-pass filter and digital controlled oscillator respectively. The FDC or TDC refers to the fact that the system can utilize either a frequency to digital converter or time to digital converter respectively. The mathematical model of the block diagram of Fig. 3 is shown in Fig. 4.

The mathematical model shown in Fig. 4 is similar to that of [2] with some added scaling factors in the feed-back path and the added feed-forward path. In Fig. 4, the signals $\Delta f_R/f_R$, N, Φ_R, Φ_v and Δf_v refers to the normalized input reference time stamp, frequency multiplication factor, reference integrated phase, output integrated phase, and output frequency respectively. The loop parameters $F(z)$, $K^{\wedge}{}_{DCO}$, K_{DCO}, f_R, and f_{free} refers to the loop filter's transfer function, the DCO gain normalization factor, DCO gain, reference frequency and the free running frequency respectively. The free running frequency of a DCO can be defined as the oscillation frequency of the DCO with zero input code for DCO. Observe that the proposed feed-forward transfer function (dashed box in Fig. 4), or the equivalent G(s) of Fig. 2 is related to it's input and output signals Q(z) and P(z) by in z-domain by (1).

$$P(z) = \left[Q(z) - \frac{f_{free}}{f_R} \cdot (1 + e_f)\right] \cdot \frac{1 + e_K}{K'_{DCO}} \tag{1}$$

The feed-forward element's parameter K'_{DCO} is equal to $K_{DCO}/K^{\wedge}{}_{DCO}$. Finally e_f and e_k refers to the normalized free running frequency's offset compensation error and normalized DCO gain compensation error factors. These value model the normalized error in the free-running frequency and DCO gain prediction. Note that e_f and e_k are design variables which set the allowable error in free-running frequency and gain prediction respectively. Achievable values will vary from system to system. For example if e_f and e_k are 0.01, and 0.02 respectively, this would mean that the designed system should be able to predict the free running frequency to within 1 percent and DCO gain within 2 percent. Note that these two values are not dependent on loop-parameters such as damping factor, and are determined by the accuracy of the system itself, in terms of the number

of bits, DCO non-linearity, frequency step size, the accuracy of the DCO free-running frequency and gain prediction method, which follows. In practice, simulation should be used to assist in predicting the practical value of e_f and e_k for the system.

Note that all values used in the feed-forward path are either known or can be obtained from the PLL's loop itself, making full use of the digital nature of ADPLL. Specifically, three parameters are needed to obtain the proposed feed forward path.

- f_R — the reference frequency
- f_{free} — the free running VCO frequency
- $K'_{DCO} = K_{DCO}/K^{\wedge}{}_{DCO}$ the gain of the DCO normalized by the DCO normalization factor $K^{\wedge}{}_{DCO}$

From these three values the feed forward free running frequency compensating factor f_{free}/f_R and the feed forward DCO gain compensation factor $1/K'_{DCO}$ can be obtained. The first element, the reference frequency f_R is a designer specified parameter and is known. The third element's dividing factor $K^{\wedge}{}_{DCO}$ or the DCO's normalization factor is also specified by the designer, and can be specified for example, to equal to the reference frequency f_R. This leaves two unknown parameters f_{free}, and K_{DCO}. The DCO' free running frequency can be obtained simply as shown in Fig. 5.

Here the input reference frequency $(\Delta f_R/f_R) \times N$, also called the frequency control word (FCW), and the feed forward free running frequency compensation factor f_{free}/f_R are set to '0.' The feedback path of the signal Φ_v is also broken from the loop. This can be done by simply disabling the adder as shown, or multiplexing in a '0' input into the adder. Next, the feed back phase accumulator is also reset to '0,' an accurate value of f_{free} can then be measured and recorded after one reference period by tapping $\Delta\Phi_v$. Note that the measured value will already be normalized by the reference frequency f_R so there is no need to divide the measured value of f_{free} again by f_R to obtain the desired feed forward free running frequency compensating factor.

The inverse of the normalized DCO gain $1/K'_{DCO}$ can be found by performing a frequency step and measuring the

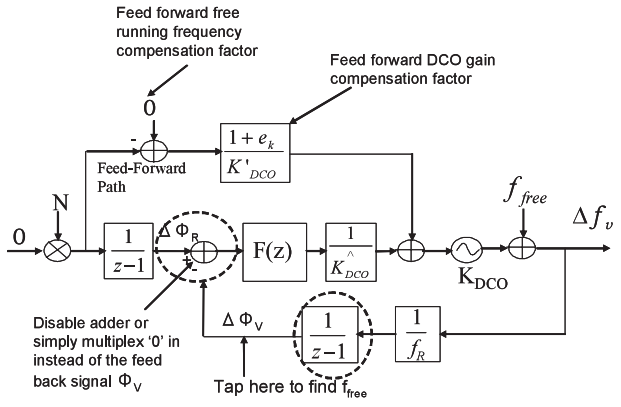


Fig. 5 Adjusting the loop to find f_{free}.

frequency control word of the DCO. When the frequency step is performed the output frequency is approximately the same as the input frequency control word $(\Delta f_R/f_R)\times N$. Two values of the DCO's control word (OTW, oscillator control word) and two values of the input frequency control words are obtained and the DCO's gain can be calculated, by calculating the slope between the two sets of points. A divider can be avoided by noting that the inverse of the frequency step $\Delta f_R/f_R$ can be pre-calculated [8].

4. Analysis

For comparative purposes, the transfer function of the ADPLL system without feed-forward path should be found. This can be found by utilizing the mathematical model shown in Fig. 4; however the feed-forward path is neglected. The transfer function of the ADPLL in Fig. 4 without the feed-forward path can be shown to be [9]

$$\Delta f_v = \frac{(N \cdot F(z) \cdot K'_{DCO})}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} + \frac{f_{free} \cdot (z-1) \cdot f_R}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \tag{2}$$

Where the parameters are as defined earlier. Examining this transfer function it is noted that the right hand side contains two terms. The first term on the right hand side of the equation reacts with any input reference frequency change $(\Delta f_R/f_R) \times N$. This term is the term that defines the characteristic transfer curve when the ADPLL is excited by an input reference frequency change represented by the code word of $(\Delta f_R/f_R) \times N$. The second term on the right does not react to any change in the input frequency control word. The second term merely reacts to the free running frequency of the synthesizer, however, after the initial power-up, it settles and is compensated by the loop and does not again react to any input frequency control word change. In general, the free running frequency f_{free} is neglected as the PLL is assumed to be linearized around locking and this free running frequency only serves as an offset to the system, but does not react to any change to the input frequency control word of the system.

Next the ADPLL in Fig. 4 is considered with an ideal feed-forward path. This is done by finding the transfer function of the ADPLL in Fig. 4 including the feed-forward path but ignoring the error factors e_f and e_k. This results in the transfer function

$$\Delta f_v \cdot \left(1 + \frac{F(z) \cdot K_{DCO}}{f_R \cdot (z-1) \cdot \hat{K}_{DCO}}\right) = \frac{\Delta f_R}{f_R} \cdot \frac{N \cdot F(z) \cdot K_{DCO}}{(z-1) \cdot \hat{K}_{DCO}} + \frac{\Delta f_R}{f_R} \cdot \frac{N \cdot K_{DCO}}{K'_{DCO}} - \frac{f_{free} \cdot K_{DCO}}{f_R \cdot K'_{DCO}} + f_{free} \tag{3}$$

The system in Fig. 4 was designed with a DCO normalization factor $K^{\wedge}{}_{DCO} = f_R$ substituting this into (3) results in

(4).

$$\Delta f_v = N \cdot f_R \cdot \frac{\Delta f_R}{f_R} \tag{4}$$

Note that the normalized reference $\Delta f_R/f_R$ is basically unity and provides only the timing, and the frequency multiplication factor $N = f_v/f_R$ or the ratio between the expected output frequency and input reference frequency. With these facts in mind (4) can be interpreted as stating that the output synthesized frequency will change instantly when a change in the reference frequency occurs, bypassing the loop all together.

In reality however, it is impossible to precisely predict the DCO's free running frequency f_{free}, and the DCO's gain present in the K'_{DCO} term. Several sources of the prediction error exist. First, it is impossible to exactly predict the characteristics of the DCO, as despite the fact that it is ideally a fully digital element (such as DCO's made from full digital components), most high frequency applications require high oscillation frequency and good phase noise characteristics of which dictates the core of the VCO to be an essentially analog element, such as a ring oscillator or LC oscillator, controlled digitally. Second, the fact that the system processes digital signals means that it inherently has finite resolution introducing quantization error into the system.

The error in estimating the DCO's gain and free running frequency can be modeled by the error factors e_k and e_f respectively. In the model in Fig. 4, these values are in normalized form. Analyzing Fig. 4 again, this time with the feed-forward path including the error terms e_k and e_f, and again setting $K^{\wedge}{}_{DCO} = f_R$ it is possible to arrive at

$$\Delta f_v = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R + \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \frac{e_k \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} - \frac{(e_k + e_f + e_f \cdot e_k) \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} f_{free} \tag{5}$$

The right hand side of (5) consists of 3 terms. The first term results from the part of the perfect feed-forward compensation of the change in the input reference and is the same as (4). The last term results from a combination of DCO gain and frequency prediction error factors e_f and e_k. This term is however, independent of the DCO's input reference's switching characteristics, and is similar to the second term on the right of Eq. (2). As it is only dependent upon the free running frequency which is constant, the PLL's loop will automatically compensate for this term at power-up automatically. After it is compensated for it will no longer affect any subsequent switches in the input reference frequency as in (2).

The error of the prediction of the DCO characteristics are exhibited through the second term only as indicated by the fact that it is proportional to the input reference change $N \times \Delta f_R/f_R$. Several factors can be interpreted by observing the second term of (5). First, it is only dependent upon the DCO's gain prediction error e_k and not on the DCO's free running frequency e_f. This means that even if the free running frequency is not estimated accurately, it does not affect the switching characteristic of the DCO during the frequency change. Second, the transfer function of the second term in (5) is similar to that of the first term in (2). In fact the characteristic function (denominator) of the first term in (2) is exactly the same as that of the second term in (5) independent of $F(z)$ the filter's transfer function. In general let

$$F(z) = K \frac{\prod_{i=1}^{m}(z - Z_i)}{\prod_{j=1}^{n}(z - P_j)} = \frac{K \cdot (z-Z_1) \cdot (z-Z_2) \cdots (z-Z_m)}{(z-P_1) \cdot (z-P_2) \cdots (z-P_n)} \tag{6}$$

Where 'K' is the gain of the filter and Z_i ($i = 1 \cdots n$) are the filter's zeros and P_j ($j = 1 \cdots m$) are the filter's poles respectively. Then substituting (6) into the first term of (2) and the first two terms of (5) will result in respectively (7) and (8)

$$\Delta f_v = \frac{\left(N \cdot K \cdot \prod_{i=1}^{m}(z-Z_i) \cdot K'_{DCO}\right)}{f_R \cdot (z-1) \cdot \prod_{j=1}^{n}(z-P_j) + K \cdot \prod_{i=1}^{m}(z-Z_i) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} \tag{7}$$

$$\Delta f_v = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \frac{(e_k+1) \cdot (z-1) \cdot f_R \cdot \prod_{j=1}^{n}(z-P_j) + K \cdot \prod_{i=1}^{m}(z-Z_i) \cdot K'_{DCO}}{(z-1) \cdot f_R \cdot \prod_{j=1}^{n}(z-P_j) + K \cdot \prod_{i=1}^{m}(z-Z_i) \cdot K'_{DCO}} \tag{8}$$

It is observed that the characteristic transfer function (denominator) of (7) and (8) are identical. Since the stability of a system depends on its characteristic transfer function, it can be concluded that the addition of the feed-forward path does not cause any instability problem to a system initially designed to be stable (all poles in the unit circle). This is in contrast to the speed up techniques which change the gain or bandwidth of the loop filter. In these cases the system must be designed such that it is stable for all gain and bandwidth combinations which will change during lock.

This stability advantage of the proposed feed-forward compensation method can be understood intuitively. Observe from Fig. 4 that the feed-forward path introduces a change to the system only once when the frequency reference change as it consists of only a scaling and offset factor as shown in (1). This initial prediction of the needed DCO control code to generate the desired output DCO frequency occurs only once every time the frequency reference is changed, essentially injecting a prediction offset into the system each time the frequency changes. This offset then remains stable after the input change, changing to the new predicted value in accordance with the reference. The feedback loop characteristic bandwidth or gain is not changed, as only a one time offset is injected into the system and remains stable.

The advantage of this fact is obvious; the system will

not become unstable even if a bad prediction value is injected in, as the added value will occur only once. A bad prediction value will only slow down the improvement in settling time and will not cause instability.

5. Settling Speed Improvement

To study the ability of the feed-forward compensation method's ability to improve the ADPLL's settling speed, a Matlab model was built based upon Fig. 4.

The reference frequency of 10 MHz was chosen and for simplicity the loop filter is a first order low-pass filter with one pole at origin and one zero, with a bandwidth of approximately 1 MHz. Two systems are compared one with and one without feed-forward compensation. The system with feed-forward compensation was modeled with a 1 percent error in DCO gain estimation as this value can readily be achieved [8].

The ADPLL system was switched between 5.2 GHz to 5.2235 GHz, a frequency step of 23.5 MHz. The resulting frequency step responses for a system without and with feed-forward compensation are shown in Fig. 6(a) and Fig. 6(b) respectively.

From the comparison between Fig. 6(a) and Fig. 6(b) it is clearly observed that the system with feed-forward compensation settles faster than the system without feed forward compensation. In addition it is observed that the overshoot of the system with feed-forward compensation becomes significantly smaller for reasonable predictions. The decreased dependence of overshoot on damping factor is another benefit of the direct reference feed forward compensation system.

It is interesting to study the dependence of settling speed on DCO gain estimation. The DCO gain estimation error is varied and the settling speeds of the DCO are shown in Fig. 7(a). Settling improvement factor, defined as the settling speed of ADPLL with no feed-forward divided by that of the system with feed-forward is shown in Fig. 7(b).

The ADPLL are considered settled when they have settled to within 10 ppm (part per million) of the desired final value. It is observed that at certain gain estimation error settling speed drastically improves. These thresholds are crossed when the prediction of the final value is close enough such that the ADPLL does not ripple over the settling limit.

The simulation in Fig. 8 shows the dependence of the feed-forward compensation's settling speed and improvement factor versus filter's damping factor. It is observed that the settling improvement factor increases dramatically in the vicinity of and over the damping factor of 1.

In particular, the jump in settling improvement factor near the damping factor of 0.7 is caused by the over-shoot of the ripple becoming smaller than the required settling er-

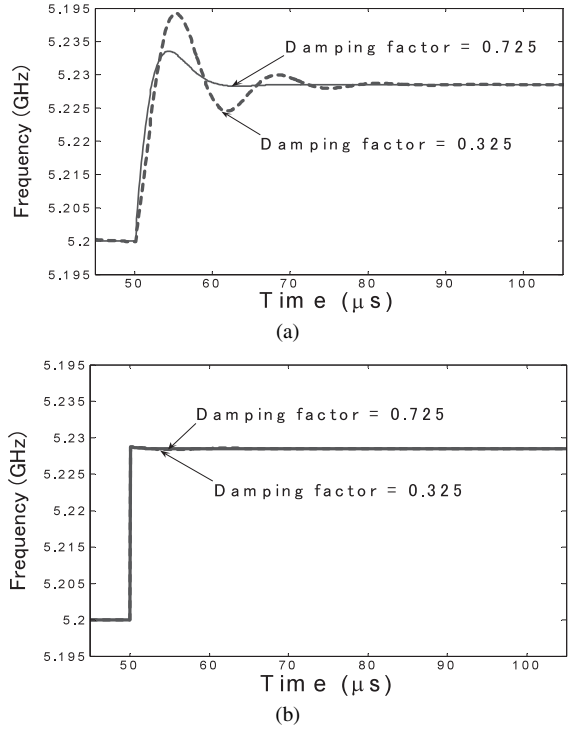


Fig. 6 (a) Frequency step response of an ADPLL without feed forward compensation. (b) Frequency step response of an ADPLL with feed forward compensation.

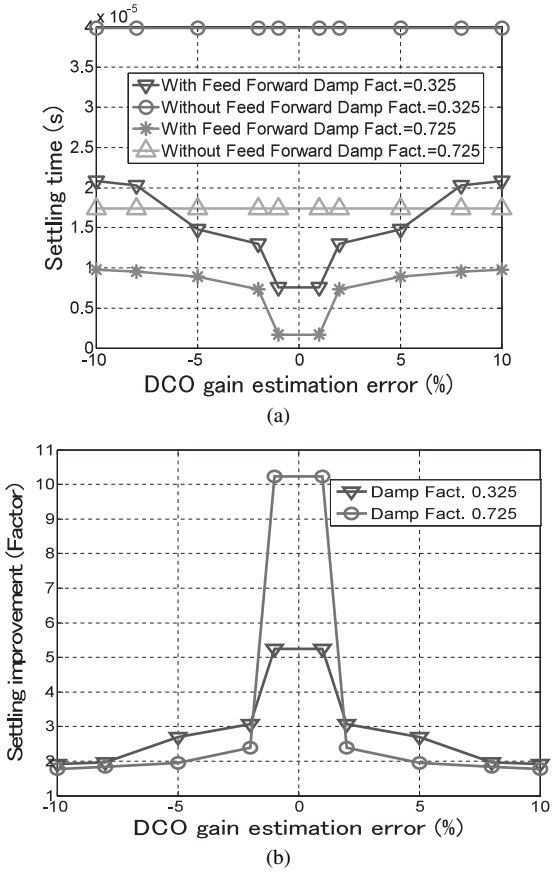


Fig. 7 (a) ADPLL settling time VS DCO gain estimation error. (b) Feed-forward ADPLL settling improvement factor VS DCO gain estimation error.

ror limit, as shown in Fig. 9 (drawn not to scale). The sudden jump in settling improvement factor can be observed by comparing the low damping factor and high damping factor systems with feed-forward as shown in Figs. 9(a) and (b). A damping factor of 0.7 can be compared to the higher damping factor system which causes the PLL to settle with smaller ripples caused by the remaining error due to the feed-forward miss prediction. If the ripple is small enough to be smaller than the threshold settling error, the system settles much faster since the period of the settling ripple is usually quite large due to low bandwidth of the PLL. The step improvement in the settling speed of the system without feed-forward in Fig. 8 can similarly be explained by the low and very low damping factor (t_{s2} and t_{s1} respectively) system as shown in Fig. 9(a). It should be mentioned that it is advantageous for the feed-forward to greatly improve settling speed near damping factor of 1 since most PLLs are usually designed with a damping factor close to 1 for stability reasons. A settling improvement factor of over 10 is achieved for a damping factor of 1. This means that the settling speed can be reduced to 1/10th that of the system without feed forward.

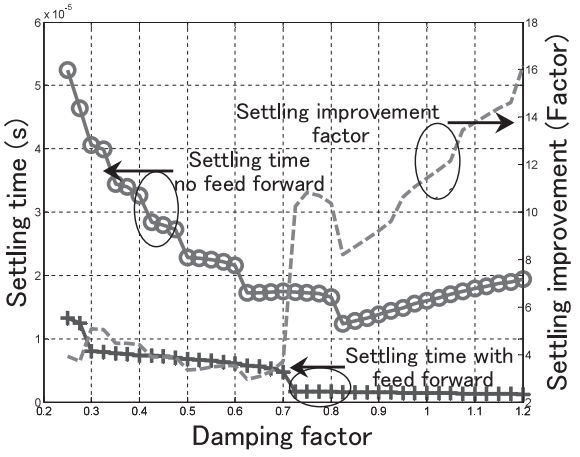


Fig. 8 Settling time and settling improvement factor VS damping factor for the feed-forward and regular ADPLL.

6. Feed-Forward Sample System

In Sect. 4 a general analysis of the feed-forward compensation system was shown and compared to the system without feed forward. In this section, a more specific analysis will be made to understand more deeply how the feed forward compensation works and how to optimize the ADPLL for feed forward compensation. First assume that a simple first order digital filter with one pole at the origin and one zero is used. The transfer function of this filter is defined as

$$F(z) = \frac{\alpha(z-1)+\rho}{z-1} \tag{9}$$

Substitute (9) into (2) neglecting the last term on the right and (5) neglecting the last term on the right (last terms are neglected as they do not contribute to step response). Solving the poles and zeros of these two equations results in (10) and (11) where (10a) and (10b) are the poles and zeros of the first term on the right of (2) and (11a) and (11b) are the poles and zeros of the first two terms in (5).

$$P_1 = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R - \sqrt{K'^2_{DCO}\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho},$$

$$P_2 = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R + \sqrt{K'^2_{DCO}\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho} \tag{10a}$$

$$Z_1 = \frac{\rho-\alpha}{\alpha} \tag{10b}$$

$$P_{FF1} = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R - \sqrt{K'^2_{DCO}\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho},$$

$$P_{FF2} = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R + \sqrt{K'^2_{DCO}\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho} \tag{11a}$$

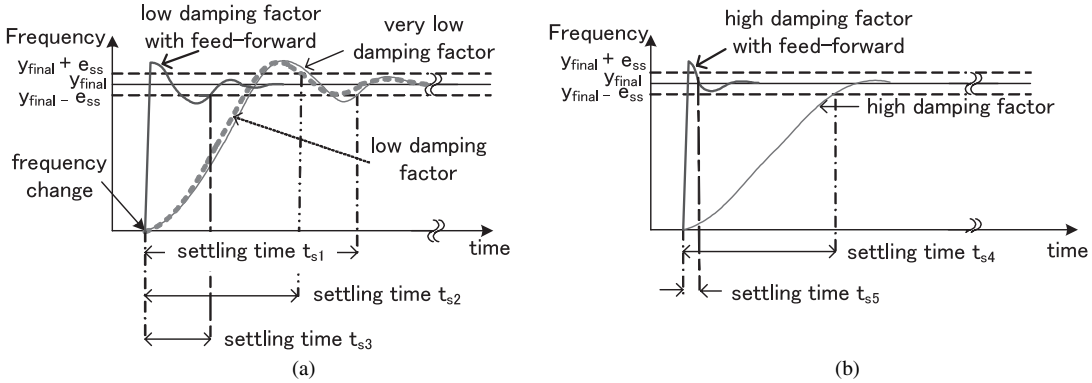


Fig. 9 PLL settling example. Low damping factor system with and without feed-forward shown in (a), and high damping factor systems shown in (b).

$$Z_{FF1} = -\frac{1}{2} \cdot \frac{1}{f_R(e_k+1)} \cdot [K'_{DCO} \cdot \alpha - 2 \cdot f_R(1+e_k) - \sqrt{K'^2_{DCO} \cdot \alpha^2 - 4 \cdot f_R \cdot K'_{DCO} \cdot \rho(e_k+1)}],$$

$$Z_{FF2} = -\frac{1}{2} \cdot \frac{1}{f_R(e_k+1)} \cdot [K'_{DCO} \cdot \alpha - 2 \cdot f_R(1+e_k) + \sqrt{K'^2_{DCO} \cdot \alpha^2 - 4 \cdot f_R \cdot K'_{DCO} \cdot \rho(e_k+1)}] \quad (11b)$$

Comparing (10a) and (11a) it is observed that the poles of the regular system without feed-forward is the same as that of the feed forward system as predicted earlier in Sect. 4. The zeros are changed, however. While the zero of the non-feed forward system is simple (10b), the zeros of the system with feed forward system has changed significantly from the original. Observe that as the K'_{DCO}'s gain prediction error e_k approaches 0 in (11b) the zeros of the feed-forward transfer function approaches the same location as the poles (10a) and (11a). This essentially means that the effect of adding the feed forward path into the ADPLL serves the effect of adding and modifying the zeros to cancel the poles of the loop. This pole cancellation is true in general for any type of filter as can be observed from (8). Error in DCO gain estimation then effectively results in the shift of these cancellation zeros from the ideal location of the poles of the system.

A model closely imitating hardware was designed in Verilog-AMS. The system with the feed forward path is shown in Fig. 10 based on the system in [2]. The system without the feed forward path is basically the same excluding the feed forward path. For simplicity almost all blocks work with 32 bit Integer and 32 bit fractional buses, though it is possible to lower the buses on several elements in the system in the real implementation. All 32 bit multipliers are truncated so that the output works with only the bottom 32 of the 64 output bits. This is possible due to the fact that the output range of these multipliers do not exceed the 32 bit range. The DCO is modeled as a digital to analog converter in cascade with a VCO. The VCO is controlled with an analog input for ease of monitoring, but outputs square waveforms in the digital domain for fast simulation. One major difference between this system and that of [2] is that in this system, all clocked blocks are clocked with a stable reference frequency of 10 MHz with no retiming. The TDC is used to measure the difference in the fractional part of the DCO and the reference clock not the error caused by retiming.

Settling times for frequency steps of 23.5 MHz and 100 MHz are shown in Fig. 11(a) and Fig. 11(b) respectively. Settling is defined as the output reaches 10 ppm of the final value. From Fig. 11(a) similar results are observed as the Matlab model both with the same frequency step at 23.5 MHz.

The settling speed improves significantly near the damping factor of 1 with, about 13 times speed improvement achieved for 1% DCO gain prediction error. Peak speed improvement factor of 37 times is achieved at the damping factor of 2. Settling speed improvement is not as large at small damping factors for the large 100 MHz step. The results of Fig. 11(b) shows improvement in settling speed at a much higher damping factors of nearly 1.5 and large improvements at damping factors near 2 with more than 35 times speed improvement. This results since, for high frequency steps, the same DCO gain estimation error produces a larger initial error at the frequency step. Higher damping factors produces much faster settling systems as in the under-damped systems error in prediction will not produce such a large ripple.

The damping factors in Figs. 11(a), (b) are termed "relative damping factor" since in the real implementation such as that modeled by Fig. 10, there is an unavoidable delay due to sampling in the feedback path, making the actual system third order. Normally the term damping factor only applies to second order systems. The damping factor here is an approximate of the second order system by neglecting one non-dominant pole.

Interestingly note that from Figs. 11(a), (b) if the designer is allowed to choose any damping factor freely equaling to or over 0.7 (for stability reasons), a settling improve-

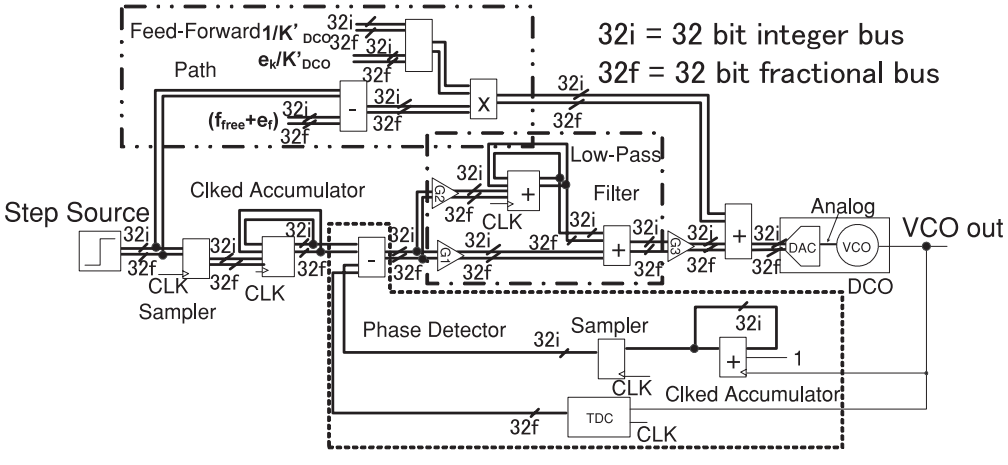
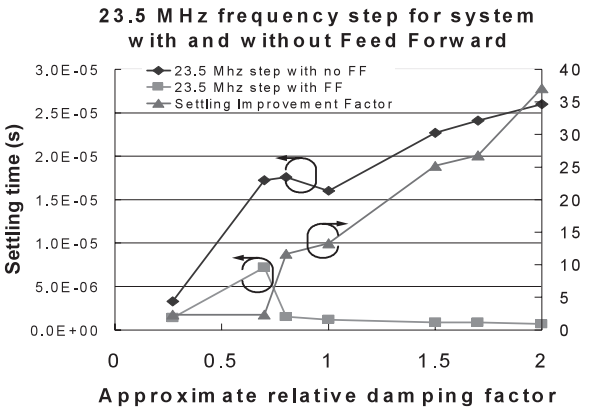
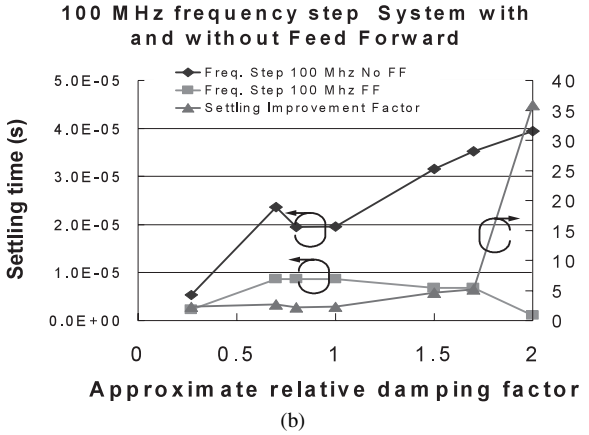


Fig. 10 Verilog-AMS model of Feed-Forward ADPLL.



(a)



(b)

Fig. 11 (a) Settling time and settling improvement of ADPLL with feed forward vs. damping factor for 23.5 MHz frequency step. (b) Settling time and settling improvement of ADPLL with feed forward vs. damping factor for 100 MHz frequency step.

ment factor of 24 times can be achieved for a feed-forward compensated system over the shortest achievable settling time of the ADPLL system without feed-forward compensation for the 23.5 MHz case, and 17 times speed improvement can be achieved for the 100 MHz frequency step case under the same condition.

It should also be noted that although the proceeding simulation results of 1% DCO gain prediction error; this is not a fixed condition and will vary from system to system. Simulations have shown, for example, that a relatively large settling improvement, of about 20 times can be achieved with 5% DCO gain prediction error, if the designer is allowed to increase the relative damping factor of the system to approximately 3.

The fact that feed-forward compensation is more effective at higher damping factors is an advantage, as a higher damping factor means a more stabilized system. This means that the system's stability improves with the settling time in the feed-forward compensation system as opposed to regular systems where a tradeoff between the two is necessary.

7. Conclusion

Direct reference feed-forward compensation is proposed as a settling speed enhancement method for ADPLLs. The method utilizes the ADPLL's digital nature to self-monitor and find parameters for feed-forward compensation. This technique was shown to be robust and does not add instability issues to the speed enhancement of the PLL's settling. Finally analysis shows the effect of gain estimation and simulation results confirm that a system with increased stability and faster settling speed can be achieved at the same time.

References

[1] A. Kajiwara and M. Nakagawa, "A new PLL frequency synthesizer with high switching speed," IEEE Trans. Veh. Technol., vol.41, no.4, pp.407–413, Nov. 1992.
[2] R.B. Staszewski and P.T. Balsar, "Phase-domain all-digital phase-locked loop," IEEE Trans. Circuits Syst. II, vol.52, no.3, pp.159–163, March 2005.
[3] J. Lee and B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control," IEEE J. Solid-State Circuits, vol.35, no.8, pp.1137–1145, Aug. 2000.
[4] I. Hwang, S. Lee, S. Lee, and S. Kim, "A digitally controlled phase-locked loop with fast locking scheme for clock synthesis," IEEE International Solid-State Circuits Conference, pp.168–169, Feb. 2000.
[5] S.M. Shahruz, "A low-noise and fast-locking phase-locked loop," Proc. American Control Conference, vol.3, pp.2407–2412, June 2003.
[6] J. Dunning, G. Garcia, J. Lundberg, and E. Nuckolls, "An all-digital phase-locked loop with 50-cycle lock time suitable for high-performance microprocessors," IEEE J. Solid-State Circuits, vol.30, no.4, pp.412–422, April 1995.
[7] B. Zhang and P. Allen, "Feed-forward compensated high switching speed digital phase-locked loop frequency synthesizer," Proc. ISCAS, vol.4, pp.371–374, June 1999.
[8] R.B. Staszewski, D. Leipold, and P.T. Balasara, "Just-in-time gain estimation of an RF digitally-controlled oscillator for digital direct frequency modulation," IEEE Trans. Circuits Syst. II, vol.50, no.11, pp.887–892, Nov. 2003.
[9] W. Chaivipas, A. Matsuzawa, and P.C. Oh, "Feed-forward compensation technique for all digital phase locked loop based synthesizers," Proc. ISCAS, pp.3209–3212, May 2006.

Win Chaivipas received the B.S. in Electrical Engineering from Sirindhorn International Institute of Technology Pathumthani Thailand and M.S. from Royal Institute of Technology Stockholm, Sweden in 2001 and 2003 respectively. He was an intern at National Electronics and Computer Technology Center, Thailand, where he studied DSPs and at Fujikura Ltd. Chiba, where he studied about manufacturing of flexible printed circuits and flip-chip bonding in during the summer of 2000. In 2003 he conducted research concerning automatic tuning of RF active filters at the Swedish Institute of Microelectronics and Optics Acreo, and was a research assistant at Sirindhorn International Institute of Technology in 2004. He is currently perusing his PhD at Tokyo Institute of Technology, Tokyo, Japan.

Akira Matsuzawa received B.S., M.S., and Ph.D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and Mixed Signal LSI technologies; ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, digital read-channel technologies for DVD systems, ultra-high speed interface technologies for metal and optical fibers, a boundary scan technology, and CAD technology. He was also responsible for the development of low power LSI technology, ASIC libraries, analog CMOS devices, SOI devices. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is a professor on physical electronics. Currently he is researching in mixed signal technologies; CMOS wireless transceiver, RF CMOS circuit design for SDR, and high speed data converters. He served the guest editor in chief for special issue on analog LSI technology of IEICE transactions on electronics in 1992, 1997, and 2003, the vice-program chairman for International Conference on Solid State Devices and Materials (SSDM) in 1999 and 2000, the Co-Chairman for Low Power Electronics Workshop in 1995, a program committee member for analog technology in ISSCC and the guest editor for special issues of IEEE Transactions on Electron Devices. Now he serves the chairman of Silicon Analog and RF committee, the vice chairman of Integrated Circuit and Devices on IEICE, the vice chairman of 177 committee on JSPS, IEEE SSCS elected Adcom and IEEE SSCS Distinguished lecturer. He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He is an IEEE Fellow since 2002.