PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

# The Effects of Switch Resistances on Pipelined ADC Performances and the Optimization for the Settling Time

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**SUMMARY** In this paper, we discuss the effects of switch resistances on the step response of switched-capacitor (SC) circuits, especially multiplying digital-to-analog converters (MDACs) in pipelined analog-to-digital converters. Theory and simulation results reveal that the settling time of MDACs can be decreased by optimizing the switch resistances. This switch resistance optimization does not only effectively increase the speed of single-bit MDACs, but also of multi-bit MDACs. Moreover, multi-bit MDACs are faster than the single-bit MDACs when slewing occurs during the step response. With such an optimization, the response of the switch will be improved by up to 50%.

***key words:*** *analog to digital converter, pipeline operation, switched capacitor amplifier, on resistance*

## 1. Introduction

Modern sub-micrometer CMOS processes facilitate the recent trend towards large system-on-a-chip solutions, which include not only digital circuitry but also an analog core on the same die. Such electronic systems on a single chip allow the reduction of the size of electronic equipment and their power consumption, which is important for both portable electronics as well as for telecommunication devices [1]. It is obvious that in such mixed-signal systems analog-to-digital converters (ADCs) become increasingly important. Especially pipelined ADCs have grown in popularity as they possess the ability to adapt their performance to various communication applications, such as digital television, WLAN, and ADSL, just to name a few. Commonly available pipelined ADCs are of 10–14 bits resolution and may have a conversion frequency of more than 10 MHz.

The key features of pipelined ADCs are a relatively high conversion frequency at low power consumption. It is commonly known that there is a trade-off between conversion frequency and power consumption. The conversion frequency is dominated by the response of the multiplying digital-to-analog converter (MDAC) as shown in Fig. 1. The MDAC consists of an operational amplifier (OpAmp), of capacitors and switches [2]. Because previous design methods for MDACs have assumed that switch resistances can be neglected, the conversion frequency was dependent on the response of the closed loop of the OpAmp only [3]. However, this simplification does not hold anymore for the implementation of MDACs in sub-micrometer, sub-volt CMOS processes, as the switches do not get driven by a sufficiently large voltage. Therefore, the influence of the switch resistance on the settling time of MDACs needs to be considered.

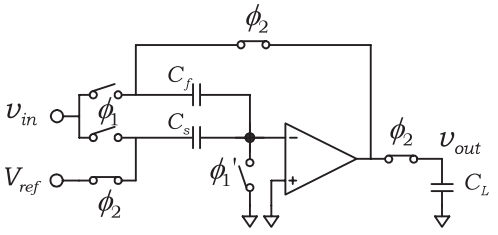


**Fig. 1** A pipelined ADC's multiplying digital-to-analog converter.

This paper confirms the influence of the switch resistance on the settling behavior of MDACs. To achieve a minimum settling time for the MDAC, switch resistances should be optimized consequently. This optimization may furthermore alleviate the trade-off between the conversion frequency and the power consumption. This paper is structured as follows: In Sect. 2, we describe an implementation of the MDAC and its equivalent circuit to be analyzed in this paper. In Sect. 3, we describe the step response of the MDAC and optimize the switch resistance mathematically. In Sect. 4, we describe the pole-zero analysis in order to understand why the MDAC's step response can be accelerated through switch resistance optimization. In Sect. 5, we investigate a relation between the multi-bit MDAC and its settling time. In Sect. 6, we end up with some conclusion.

## 2. Analytical Model of MDAC

### 2.1 MDAC Implementation

An implementation of the MDAC to be analyzed in this paper is given in Fig. 2. To simplify the analysis, we consider $M$ bits per stage of the MDAC ($M$=1, 2, 3, ...). In practice, $M$ bits per stage of the MDAC is implemented with redundancy (e.g., 1.5 bits per stage), but the assumption of $M$ bits per stage simplifies the explanation of our optimization method.

During the sampling phase, the analog input is sampled into the sampling capacitors $C_s$ and $C_f$. In the amplifying phase, $C_s$ is connected to the reference voltage $V_{ref}$, whereas $C_f$ forms the negative feedback loop around the OpAmp. $C_s$ and $C_f$ are given as multiples of the first stage's unit capacitance, $C_o$: $C_f = C_o$ and $C_s = mC_o$. The gain of the MDAC, $G_{MDAC}$, is given by

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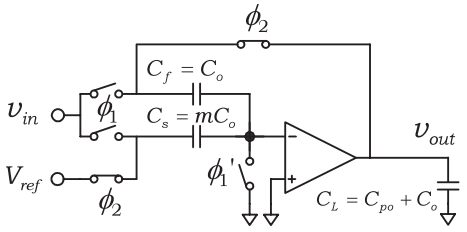


**Fig. 2** An MDAC used for analysis.

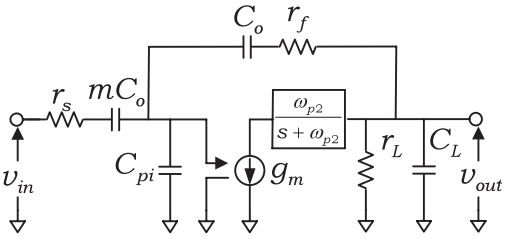


**Fig. 3** The equivalent circuit of the MDAC show in Fig. 2.

$$G_{MDAC} = 1 + m = 2^M \tag{1}$$

The capacitance of the output capacitor $C_L$ is

$$C_L = C_{po} + C_o \tag{2}$$

where $C_{po}$ is the parasitic output capacitance of the OpAmp and $C_o$ in (2) is sampling capacitor of the next stage.

We suppose that the switched OpAmp technique is used for decreasing the settling time and power consumption [4], [5]. Therefore sampling switch of the next stage is removed.

### 2.2 Equivalent Circuit of the MDAC

To obtain the transfer function of the MDAC, we consider an equivalent circuit of the MDAC as shown in Fig. 3. The equivalent circuit can be modeled using the sampling switch resistance $r_s$, the feedback switch resistance $r_f$, the parasitic input capacitance $C_{pi}$, the parasitic output capacitance $C_{po}$, the trans-conductance $g_m$, the output impedance $r_L$, and the second pole, $\omega_{p2}$, of the OpAmp.

To simplify the transfer function of the circuit shown in Fig. 3, we assume that $\omega_{p2}$ is greater than the open-loop unity gain bandwidth $\omega_u$, that $C_{pi} \ll C_o$, and $g_m r_L \gg 1$. The transfer function of the MDAC is given by

$$v_{out} = -\frac{s + z_1}{(s + p_1)(s + p_2)} v_{in} \tag{3}$$

with

$$z_1 = \frac{g_m}{C_o\left(-1 + g_m r_f\right)} \tag{4}$$

$$p_1 = \alpha - \sqrt{\alpha^2 - \frac{g_m}{mC_oC_L\left(r_s + r_f\right)}} \tag{5}$$

$$p_2 = \alpha + \sqrt{\alpha^2 - \frac{g_m}{mC_oC_L\left(r_s + r_f\right)}} \tag{6}$$

and

$$\alpha = \frac{mC_o\left(1 + g_m r_s\right) + C_L(m+1)}{2\,mC_oC_L\left(r_s + r_f\right)} \tag{7}$$

## 3. Switch Resistance Optimization

### 3.1 Step Response of the MDAC

The settling time of the switched capacitor amplifier is reduced by switch resistance optimization as shown in [6] and [7]. However, the relation between $r_s$ and $r_f$ is not shown; these analyses consider the effects of $r_s$ and $r_f$ only separately. We then show the optimum condition of switch resistance which decreases the settling time of the MDAC.

The step response of the MDAC is given by

$$v_{out} = -mV_{in}\left[1 - (\cosh\beta t + \gamma \sinh\beta t)\, e^{-\alpha t}\right] \tag{8}$$

with

$$\beta = \sqrt{\alpha^2 - \frac{g_m}{mC_oC_L\left(r_s + r_f\right)}} \tag{9}$$

and

$$\gamma = \frac{1}{\beta}\left(\alpha + \frac{1 - g_m r_f}{mC_L\left(r_s + r_f\right)}\right) \tag{10}$$

Equation (8) can be modified as,

$$v_{out} = -mV_{in}\left[1 - \frac{1}{2}(1+\gamma)\, e^{-(\alpha-\beta)t} - \frac{1}{2}(1-\gamma)\, e^{-(\alpha+\beta)t}\right] \tag{11}$$

Ringing does not occur in the step response if $\alpha$ and $\beta$ are positive real numbers. In this case, it is possible to conclude that $\alpha > \beta$ from (9), which leads to $\alpha - \beta > 0$ and finally $\alpha - \beta < \alpha + \beta$. Therefore the response stemming from the second term of (11) is slower than the response of the third term. In this case, the settling time given in (11) is mainly determined by the second term response.

Figure 4 shows the step response of (11) with the parameters given in Table 1. Each parameter assumes that the OpAmp designed using a $0.18\,\mu$m CMOS process. The main response and the second term response are described as a solid line and a broken line, respectively. The main response gradually approaches the response described by the second term, i.e. the second term of the response determines the settling time. Moreover, the step response in case of $r_f = 600\,\Omega$ is faster than $r_f = 400\,\Omega$.

### 3.2 Switch Resistance Optimization

We now optimize the switch resistance mathematically. The settling time of the MDAC is determined by the second term of (11), so the second term has to be minimized to decrease the settling time. If $(1 + \gamma) = 0$, the second term becomes 0. For $(1 + \gamma) = 0$, the switch resistance is given by

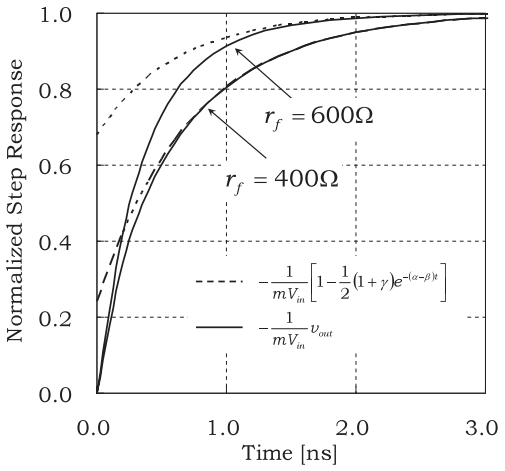


**Fig. 4** Step response of the MDAC.

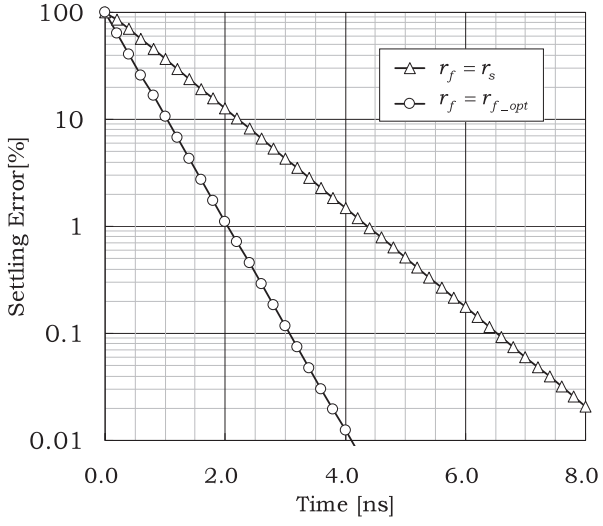


**Fig. 5** The settling error characteristics of the MDAC.

**Table 1** Model parameters.

| $r_s$ | $g_m$ | $m$ | $C_o$ | $C_{pi}$ | $C_{po}$ |
|---|---|---|---|---|---|
| 100Ω | 11.4mS | 3 | 1pF | 114fF | 270fF |

$$r_{f\_opt} = mr_s + \frac{(m+1)}{g_m} \tag{12}$$

In this case, (11) can be modified as

$$\begin{aligned} v_{out\_opt} &= -mV_{in}\left(1 - e^{-(\alpha+\beta)t}\right) \\ &= -mV_{in}\left(1 - e^{-\frac{g_m}{(m+1)C_L}t}\right) \end{aligned} \tag{13}$$

Figure 5 shows the settling error characteristics of the MDAC as a function of time for $r_f = r_s$ and $r_f = r_{f\_opt}$, with the parameters listed in Table 1. For $r_f = r_s$, the 1% settling error is reached after a 4.3 ns. By using the optimized resistances, $r_f = r_{f\_opt}$, the settling time can be lowered to 2.0 ns which corresponds to a 53% improvement in time reduction. This result demonstrates that the switch resistance optimization can effectively reduce the settling time.

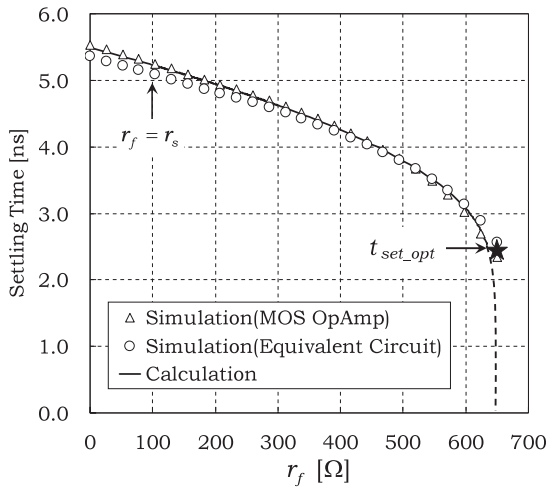


**Fig. 6** Settling time vs. resistance of the feedback-switch.

### 3.3 Settling Time of the MDAC

We now use (11) to obtain the settling time of the MDAC. In the region where $r_f < r_{f\_opt}$ holds, the settling time of the MDAC is determined by the second term of (11). In this case, the settling time $t_{set}$ is given by

$$t_{set} \approx \frac{1}{\alpha - \beta} \ln\left(\frac{1+\gamma}{2e_o}\right) \tag{14}$$

where $V_{err}$ is tolerance of the settling error and $e_o = V_{err}/V_{in}$.

If $r_f = r_{f\_opt}$, the settling time of the MDAC is determined by (13). The optimum settling time, $t_{set\_opt}$, is given by

$$t_{set\_opt} = \frac{(m+1)\,C_L}{g_m} \ln\left(\frac{1}{e_o}\right) \tag{15}$$

The settling time of the MDAC versus the feedback switch resistance $r_f$ is plotted in Fig. 6. Each parameter is shown in Table 1. The input-referred settling error margin is 0.1%. Figure 6 compares the calculation results — given by (14) and (15) — with the transistor-level simulation results (obtained with "Spectre") of the MDAC with MOS OpAmp shown in Fig. 2 and simulation results of the equivalent circuit shown in Fig. 3. The solid line in Fig. 6 is obtained from (14).

As a result, the calculation values corresponds to the simulation values within 5% for all cases of $r_f < r_{f\_opt}$. In this case, (14) describes the approximate value of the settling time. For $r_f = r_s$, the settling time is 5.2 ns. If $r_f = r_{f\_opt}$, the settling time obtained from (15) is 2.45 ns, the simulation value of the MDAC with MOS OpAmp and equivalent circuit are 2.35 ns and 2.56 ns, respectively. Therefore, by using the switch resistance optimization, the settling time of the MDAC has been improved by 50%.

To simplify the analysis, the following simulation results are given by simulation of the equivalent circuit.

## 4. Pole-Zero Analysis

### 4.1 Pole-Zero Behavior

In this chapter we analyze the system's pole-zero behavior in order to understand why the MDAC's step response can be accelerated through switch resistance optimization.

The location of the poles and zeroes is obtained through (4)–(6). For this analysis all parameters are listed in Table 1. The pole-zero location versus feedback switch resistance $r_f$ is shown in Fig. 7.

(a) $r_f < r_{f\_opt}$

In the region of $r_f$ less than $r_{f\_opt}$, since $z_1$ and $p_2$ are larger than $p_1$, $p_1$ becomes the dominant pole of the response. When $r_f$ approaches $r_{f\_opt}$, $p_1$ moves to a higher frequency and $z_1$ and $p_2$ move to a lower frequency, as is shown in Fig. 8(a).

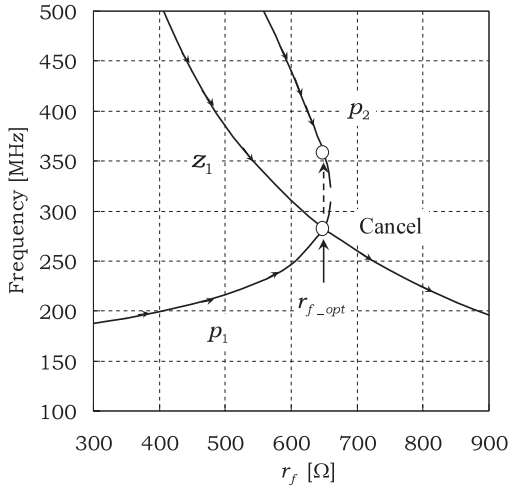


**Fig. 7** Pole-zero vs. resistance of the feedback-switch.

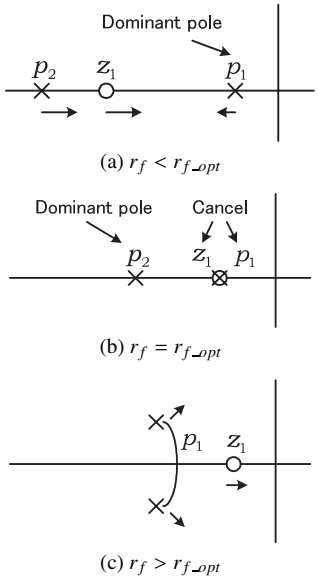


**Fig. 8** Pole-zero behavior.

(b) $r_f = r_{f\_opt}$

In case of $r_f = r_{f\_opt}$, $z_1$ and $p_1$ are at the same location. Thus, $z_1$ and $p_1$ cancel each other out and $p_2$ becomes the dominant pole as it is shown in Fig. 8(b). Therefore, the step response of the MDAC could be improved through the switch resistance optimization.

(c) $r_f > r_{f\_opt}$

In the region of $r_f > r_{f\_opt}$, $z_1$ is lower than $p_1$ and $p_2$. Therefore, a small overshoot appears in the step response. If $r_f$ is increased more and more, $p_1$ becomes the complex number as shown in Fig. 8(c), so the step response has a ringing. As a result, the settling time is increased.

### 4.2 Settling Time Improvement

In the following we will explain the property of the optimum settling time, $t_{set\_opt}$, and the method to make better use of the switch resistance optimization.

In case of $r_f = r_{f\_opt}$, pole-zero location are given by

$$p_{1\_opt} = z_{1\_opt} = -\frac{g_m}{\left(1 + g_m r_{f\_opt}\right) mC_o} \tag{16}$$

$$p_{2\_opt} = -\frac{g_m}{(m+1)\,C_L} \tag{17}$$

It is necessary to increase $p_{2\_opt}$ to improve the optimum settling time $t_{set\_opt}$. To increase $p_{2\_opt}$ without increasing the power consumption, $m$ or $C_L$ should be decreased. When a conventional architecture is used in the MDAC, $C_L$ is determined by the OpAmp's parasitic output capacitance, $C_{po}$, and the sampling capacitor of the following stage [2]. Generally, the sampling capacitor determines $C_L$. It is difficult to decrease the sampling capacitor since the sampling capacitor determines the SNR of the pipelined ADC [8]. However, when "loading free architecture" is used in the MDAC, $C_L$ becomes only $C_{po}$, so $C_L$ can be decreased drastically [9]. Therefore, the loading free architecture might be able to make better use of the switch resistance optimization. Note that for loading free architecture, this paper's analysis does not hold.

When $m$ is increased, the step response is slowed down because $p_{2\_opt}$ is decreased. However, since the gain of the MDAC is increased, the tolerance of the settling error is increased and $C_L$ is decreased. Therefore, $m$ does not influence the settling time so much considering these effects in case of small signal analysis. The detailed discussion is provided in the next section.

## 5. Settling Time of Multi-Bit MDAC

### 5.1 Multi-Bit MDAC

To investigate a relation between the multi-bit MDAC and its settling time, we assume that as follows [10],

1) Only the first stage MDAC is multi-bit per stage, other stage MDAC are 1 bit per stage.

**Table 2** Model parameter of the multi-bit MDAC.

| $r_s$ | $g_m$ | $m$ | $C_{pi}$ | $C_{po}$ |
|---|---|---|---|---|
| 100Ω | 11.4mS | $2^M$-1 | 114fF | 270fF |

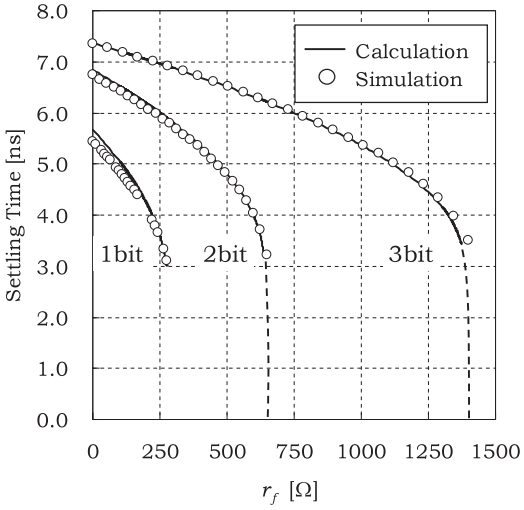


**Fig. 9** Settling time for 1–3 bit MDAC vs. resistance of the feedback switch.

2) The sampling capacitor of the first stage $C_{sa1}$ equals $(m + 1)C_o$. We assume that the digital error compensation technique is used [11], so $C_{sa1}$ is determined by required SNR. $C_{sa1}$ is constant value each multi-bit MDAC. In this analysis, $C_{sa1}$= 4 pF.
3) The sampling capacitor of the second stage $C_{sa2}$ equals $C_{sa1}$ divided by the gain of the first stage MDAC. $C_{sa2}$ equals $C_o$ since the gain of first stage is $(m + 1)$.
4) The input-referred settling error margin is 1 LSB of 12 bit resolution. It is constant value each multi-bit MDAC.
5) Each parameter is shown in Table 2.

### 5.2 Small Signal Analysis

First, we investigate the multi-bit MDAC's settling time when slewing does not occur during the step response. Figure 9 shows simulation results (obtained from the equivalent circuit shown in Fig. 3) of the settling times for 1 to 3 bit MDACs, as well as the settling times obtained from (14).

The calculated values agree with the simulation values within 5% for most cases of $r_f < r_{f\_opt}$. When $r_s$ and $g_m$ are constant, $r_{f\_opt}$ increases with the increase of $M$. Moreover, the sensitivity of $r_f$ to the settling time decreases with an increase of $M$. Because the MDAC's elements show some variability and its characteristics are input-voltage dependent, it is difficult to generally determine the optimal value for the switch resistances. Therefore, the multi-bit structure might be able to make better use of the switch resistance optimization.

Figure 10 shows the settling time as a function of $m$ in case of $r_f = r_{f\_opt}$. The calculation values correspond to

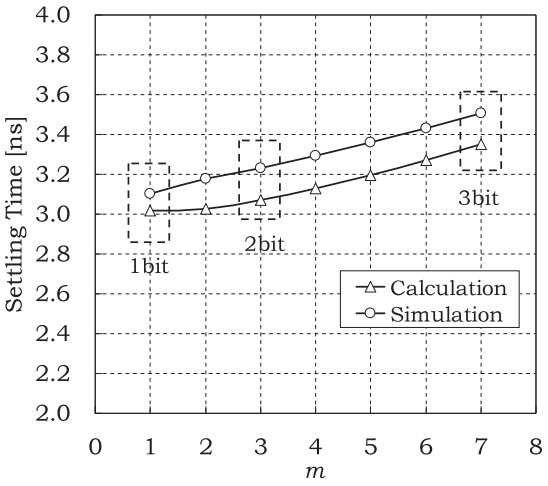


**Fig. 10** Optimum settling time vs. $m$ ($m = C_s/C_f$).

the simulation values up to within 5%. The settling time increases with an increase of $m$, e.g., the settling time is about 10% higher for $M$=3 bit compared to $M$=1 bit.

The following reasoning may reveal why multi-bit MDACs are slower than single-bit MDACs: the factor $(m + 1)$ of (15) increases the settling time, because the feedback factor is decreased with an increase of $m$. However, as the gain of the MDAC is increased, the tolerance of the settling-error is increased and $C_L$ is decreased. All these factors lead to a decreased settling time. If $C_{po}$=0, there is only the effect that tolerance of settling error is increased, so the settling time decreases with an increase of $m$. If $C_{po} \ll C_o$, the multi-bit MDAC is faster than the single-bit MDAC. In this analysis, since $C_{po}$ cannot be neglected, multi-bit MDACs are slower than single-bit MDACs.

### 5.3 Large Signal Analysis

We now investigate the relation between the multi-bit MDAC and its settling time when slewing occurs during the step response. Figure 11 shows simulation results for two cases: the settling time for a voltage controlled current source (see Fig. 3) without any current limitation, and the settling time with current limitation. In the following analysis, we assume that current limitation is 1 mA, output signal swing is 1 V and $r_f = r_{f\_opt}$.

In large signal analysis, slewing occurs in the single-bit MDAC because its load capacitance is larger. The settling time is 1.6 times larger than the settling time without current limitation. The settling time decrease with an increase of $m$ because the load capacitance in the MDAC decreases with an increase of $m$. Moreover, the feedback factor of the multi-bit MDAC is smaller than the single-bit MDAC, so slewing does not occur easily.

It is difficult to exactly calculate the settling time with slewing, but good approximations can be made. Figure 12 shows the outline chart of the step response with slewing and the step response without slewing.

The slew rate ($SR$) of the OpAmp is given by

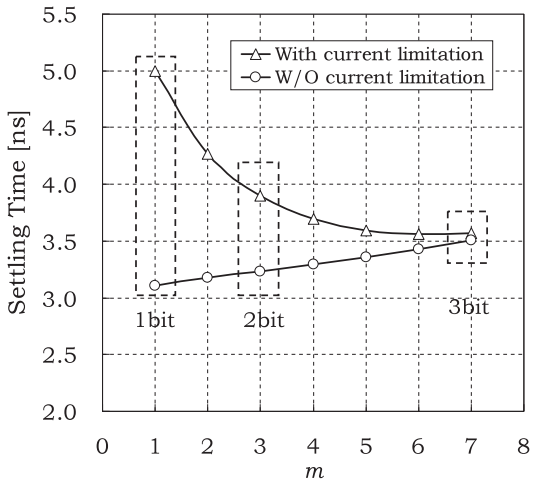


**Fig. 11** Settling time with slewing vs. $m$ ($m = C_s/C_f$).

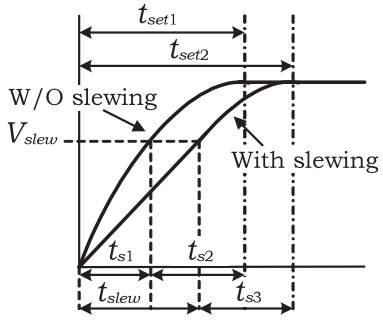


**Fig. 12** The outline chart of the step response with and without slewing.

$$SR = \frac{I_{bias}}{C_{eff}} \tag{18}$$

$$C_{eff} \approx C_L + \frac{C_s C_f}{C_s + C_f} \approx C_L + \frac{mC_o^2}{(m+1)\,C_o} \tag{19}$$

where $I_{bias}$ is the bias current of the input MOS transistor in the OpAmp and $C_{eff}$ is the total load capacitance of the OpAmp.

The settling time without slewing $t_{set1}$ is obtained from (15),

$$t_{set1} = \frac{(m+1)\,C_L}{g_m} \ln\left(\frac{1}{e_o}\right) \tag{20}$$

The time of the slope of step response without slewing equals to $SR$ is given by

$$g_m \approx \frac{2I_{bias}}{V_{eff}} \tag{21}$$

$$\frac{\partial v_{out\_opt}}{\partial t} = SR \tag{22}$$

$$t_{s1} = \frac{(m+1)\,C_L V_{eff}}{g_m} \ln\left[\frac{(m+1)\,C_L V_{eff}}{2\,mC_{eff} V_{in}}\right] \tag{23}$$

where $V_{eff}$ is the over drive voltage of the input MOS transistor in the OpAmp. We assume the step response with and without slewing are almost the same after the slewing has ended, $t_{s2}$ and $t_{s3}$ given by

$$t_{s2} = t_{set1} - t_{s1} \tag{24}$$

$$t_{s3} = t_{s2} \tag{25}$$

The output voltage when the slewing has ended can be given by

$$V_{slew} = -mV_{in}\left(1 - e^{-\frac{g_m}{(m+1)C_L}t_{s1}}\right) \tag{26}$$

We obtain $t_{slew}$ as the time slewing has ended,

$$t_{slew} = \frac{C_{eff}}{I_{bias}} V_{slew} \tag{27}$$

Finally, the settling time with slewing can be approximated as follow,

$$t_{set2} \approx t_{slew} + t_{s3} \tag{28}$$

The settling time with slewing is obtained from (28) and was plotted in Fig. 13. The values obtained by calculations agree with the simulation values to within 3%.

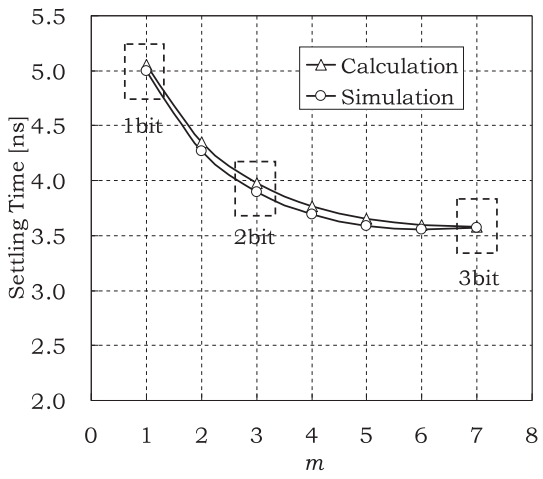


**Fig. 13** The settling time with slewing obtained from (29) vs. $m$ ($m = C_s/C_f$).

## 6. Conclusion

To design the optimum the MDAC in a pipelined ADC, the influence of the switch resistances on the settling time of the MDAC is investigated in this paper. The settling time of the MDAC is improved by determining the optimum on-resistance of the switches. The response of the switch is not given by a first-order response, but as a second-order response — an additional zero is generated by the switch resistance. The settling-time of the switch has been improved by 50% in the maximum by using pole-zero cancellation.

Moreover, the influence of the switch on the settling-time of a multi-bit MDAC was investigated. It is difficult to generally determine the optimal switch resistance, due to the high variability of the elements and the dependence on the input voltage. However, the settling time of the multi-bit structure is only marginally dependent on the switch resistance. The multi-bit structure decreases the settling time

of the MDAC and simplifies reaching the design specifications. In addition, it was shown that the settling time deteriorated seriously by slewing of the OpAmp. However, slewing rarely appears in multi-bit structures whose capacitive load is smaller than that of single-bit structures. Consequently, the multi-bit structure is more suited to reduce the settling time of MDACs.

It is shown that in the design of MDACs the properties of the switches need to be considered. The method of determining the optimum design as shown in this paper is attractive for the design of ADCs with a high conversion frequency and a high resolution.

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