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Digital Calibration Method for Binary-Weighted Current-Steering D/A-Converters without Calibration ADC

Yusuke IKEDA[†], *Nonmember and* **Akira MATSUZAWA**[†a)], *Member*

SUMMARY A new digital calibration scheme for a 14 bit binary weighted current-steering digital-to-analog converter (DAC) is presented. This scheme uses a simple current comparator for the current measurement instead of a high-resolution ADC. Therefore, a faster calibration cycle and smaller additional circuits are possible compared to the scheme with the high-resolution ADC. In the proposed calibration scheme, the lowest 8 bit part of the DAC is used for both error correction and normal operation. Therefore, the extra DACs required for calibration are only a 3 bit DAC and a 6 bit DAC. Nevertheless, a large calibration range is achieved. Full 14 bit resolution is achieved with a small chip-area. The simulation results show that DNL and INL after calibration are 0.26 LSB and 0.46 LSB, respectively. They also show that the spurious free dynamic range is 83 dB (57 dB) for signals of 24 kHz (98 MHz) at 200 Msps update rate.

key words: *digital-to-analog converter, digital calibration, self-calibration, high resolution*

1. Introduction

For telecommunication applications, digital-to-analog converters (DACs) with a resolution of 10–14 bits at a conversion rate of several hundred MS/s are required. To fulfill such challenging specifications, current-steering DACs are widely used at present. The resolution of a current-steering DAC is limited by the mismatch of the elements that compose the DAC's current sources. Therefore, in order to obtain a high resolution, it is necessary to control the mismatch of the elements by enlarging their area. However, by increasing their size the parasitic capacitances and the wiring capacitances are augmented and the DAC's resulting conversion speed may not satisfy the desired specifications at low power levels. Furthermore, increased area also means increased cost; the area of the current-steering DAC should therefore be kept small. A high speed, high resolution DAC can be achieved by means of applying a calibration scheme [1]–[5].

Calibration schemes can be classified into two categories: analog calibration and digital calibration. Digital calibration schemes can easily be applied to low supply voltage levels and to sub-micron processes.

This paper describes a digital calibration scheme. Digital calibration schemes measure the current value of each current source and — by means of digital signal processing — determine an appropriate value that will be added from a calibration DAC. To measure the values of each current source, the use of an accurate high-resolution sigma-delta analog-to-digital converter (ADC) has been proposed [1]–[3]. This additional sigma-delta ADC enlarges the die-area and therefore increases the cost of the chip. In addition, calibration schemes using a sigma-delta ADC are slow due to high over-sampling ratios. Such high over-sampling ratios are required to achieve a high resolution. (In [2] for example, the on-chip sigma-delta ADC's over-sampling ratio is 16384.)

To overcome these disadvantages, another scheme was proposed in [4] using current comparators instead of the high resolution ADC. In addition, this scheme chooses a binary-weighted structure; the binary-weighted DAC (as opposed to the thermometer-decoded DAC) is more suitable for digital calibration as there are fewer current sources that need to be measured; this reduces the die-area of the memory and shortens the calibration time. However, the calibration DAC is required at each current source of the MSB array in [4]. This scheme therefore also enlarges the total die area.

In this paper, a novel digital calibration scheme is proposed that is applied to the binary-weighted DAC. This scheme utilizes the LSB-part of the DAC for conversion as well as for calibration. Consequently, the DAC's total die area is only marginally increased, and nevertheless high resolution is achieved. Although it is challenging to obtain a good dynamic linearity at high frequencies using a binary weighted DAC [6] (which is however more suitable for digital calibration), the dynamic properties of the DAC can be greatly improved with the help of a conventional return-to-zero circuit [2], [5]. To prove the effectiveness of a DAC with such a calibration scheme, the circuit was realized in a 0.18 μm CMOS process.

The paper is structured as follows: after this brief introduction, the calibration algorithm is discussed in detail in Sect. 2. Simulation results are presented in Sect. 3. The comparison with other digital calibration schemes is described in Sect. 4. Finally, the paper ends with some conclusions in Sect. 5.

2. The Calibration Scheme

The architecture of the proposed digitally calibrated DAC is shown in Fig. 1. The calibration circuitry is segmented into the following parts: "MAINDAC" (consisting of a 6 bit "MSBDAC" and an 8 bit "LSBDAC"), "CALDAC" (3 bit),

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[†]The authors are with Tokyo Institute of Technology, Tokyo, 152-8552 Japan.
a) E-mail: matsu@ssc.pe.titech.ac.jp

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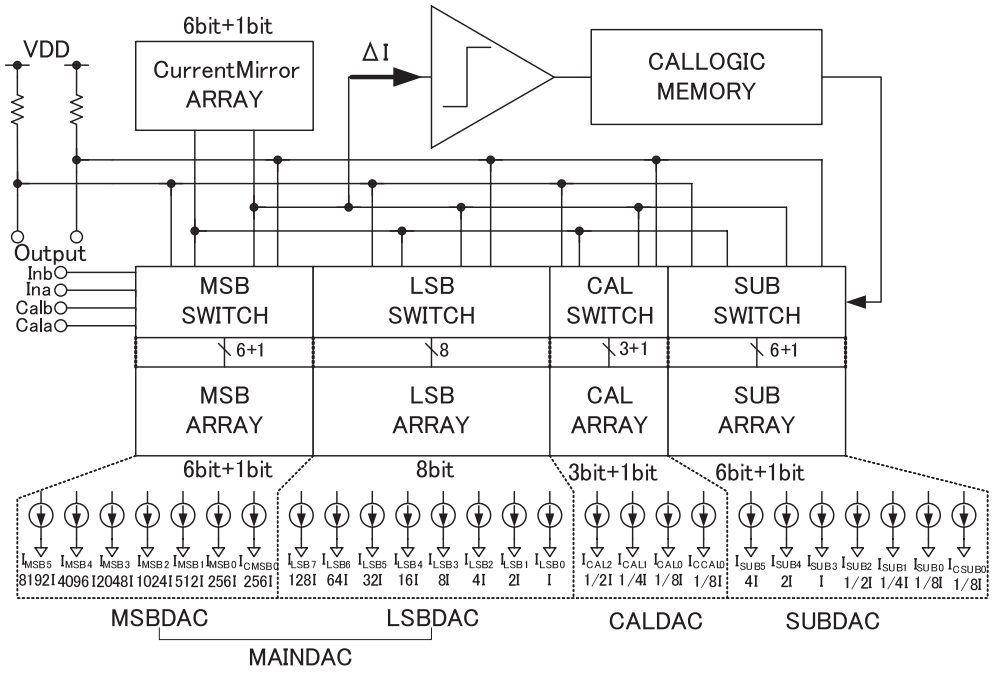

Fig. 1 Block diagram of the proposed calibrated DAC.

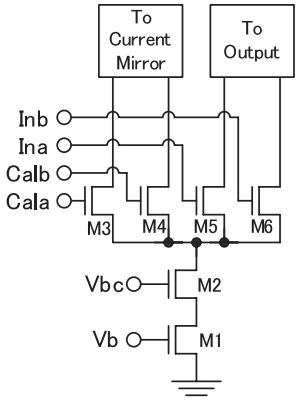

Fig. 2 The current source and the switches.

"SUBDAC" (6 bit), the current mirror array (6 bit), the current comparator, and the calibration logic. Each DAC is composed of the current-source array and the switches.

The current values in Fig. 1 indicate the nominal currents, with the MAINDAC's LSB current being I. The MSB array, the CAL array, the SUB array, and the current mirror array each need to have one additional dummy current source, which is of the same current value as each array's lowest current. All current sources and current mirrors are composed of conventional low voltage cascodes.

The current-source and the switches are shown in Fig. 2. M1 and M2 compose the current source and M3, M4, M5 and M6 are the switches. During calibration, either "Cala" or "Calb" is "high" and the others are "low." During normal conversion, either "Ina" or "Inb" is "high" and the others are "low."

The MSB array will be self-calibrated. In the proposed self calibration scheme, the MSB dummy current source (I_{CMSB0}) is calibrated before the 6 bit MSB current sources (I_{MSB0}–I_{MSB5}).

The MSB dummy current calibration is called "SUB Calibration," and the 6 bit MSB currents calibration is called "MSB Calibration." The deviation of the MSB dummy current from its nominal value ($256I$) is δ_0, and the deviations from the nominal values for the 6 bit MSB currents are from the lowest value to the highest δ_1, δ_2, δ_3, δ_4, δ_5 and δ_6. The calibration flow described in Fig. 3 is as follows: in a first step, the proposed digital calibration method obtains the digitized value of the error current through the calibration current source using a current comparator. Next, this value and an input value are processed in digital operation. Hence the obtained value controls the DAC for conversion and the DAC for calibration. Finally, the output value is calibrated.

2.1 Sub Calibration

The MSB dummy current source (I_{CMSB0}) has nominally the same current as the sum of the LSB array and the CAL array ($I_{\mathrm{LSBs}} = 256I$). However, due to mismatch, the current sources are different in practice.

During "Sub Calibration," the error current of I_{CMSB0}, δ_0, will be determined.

The current error measurement method is similar to the scheme in [4], but some details as explained below are different. I_{CMSB0} is compared with I_{LSBs}, the sum of the LSB array and the CAL array, using the current mirrors and the current comparator. δ_0 can be obtained as a 6 bit digital value by a 6-step successive approximation process utilizing SUBDAC, the current comparator output and the calibration

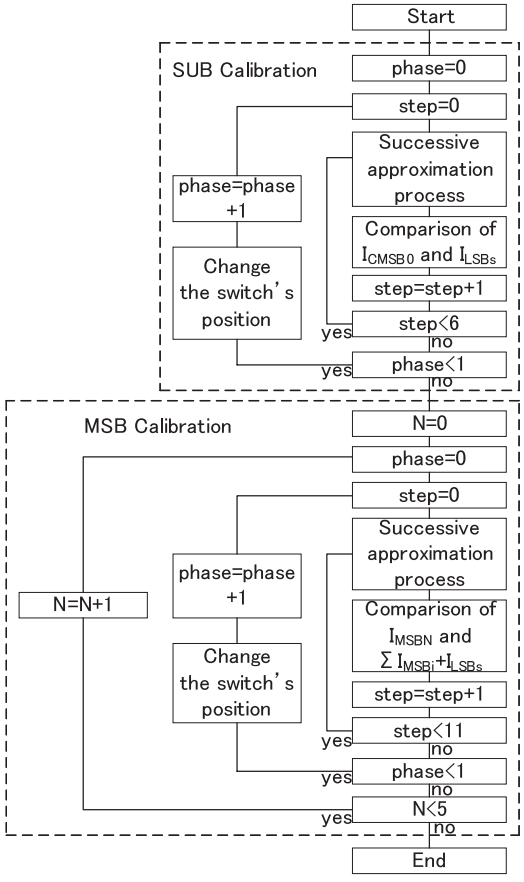

Fig. 3 The calibration flow.

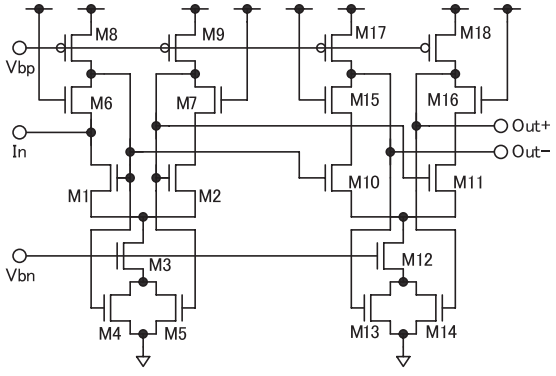

Fig. 4 The current comparator.

logic. Because current mirrors are used, the current comparator's inputs do not need to be of very low impedance, but it is still preferable. The current comparator circuit is depicted in Fig. 4. A common-gate stage is used as the input-stage of the current comparator. The drains of M6 and M8 determine the voltage at the gate of M1; this leads to a voltage-current feedback. Thanks to this feedback structure, the current-comparator has a very low input impedance. M4 and M5 introduce common-mode feedback. Both the current comparator and the current mirrors can operate at a precision of 14 bits.

The simplified Sub calibration circuit is shown in Fig. 5. For the measurement, the position of the switch is changed twice, once for phase A and once for phase B. By using two measurement results, δ_0 is obtained independently of the current comparator offset (I_{offset}) and the current mirrors' mismatch (m) as shown in Eq. (3). δ_0 is stored in a register. During normal operation, the error current of I_{CMSB0} can be cancelled out with the correct switching of SUBDAC.

$$\begin{cases} 1:(1+m)=(I_{\text{CMSB0}}+I_{\text{SUBA+}}):(I_{\text{LSBs}}+I_{\text{SUBA-}}+I_{\text{offset}}) \\ (1+m):1=(I_{\text{CMSB0}}+I_{\text{SUBB-}}+I_{\text{offset}}):(I_{\text{LSBs}}+I_{\text{SUBB+}}) \end{cases} \tag{1}$$

$$\begin{cases} (1+m)(I_{\text{LSBs}}+\delta_0+I_{\text{SUBA+}})=I_{\text{LSBs}}+I_{\text{SUBA-}}+I_{\text{offset}} \\ (1+m)(I_{\text{LSBs}}+I_{\text{SUBB+}})=I_{\text{LSBs}}+\delta_0+I_{\text{SUBB-}}+I_{\text{offset}} \end{cases} \tag{2}$$

$$\begin{aligned} \delta_0 &\cong -\frac{(I_{\text{SUBA+}}-I_{\text{SUBA-}})-(I_{\text{SUBB+}}-I_{\text{SUBB-}})}{2} \\ &\cong -\frac{I_{\text{SUBA}}-I_{\text{SUBB}}}{2} \end{aligned} \tag{3}$$

2.2 MSB Calibration

After "SUB Calibration," the 6 bit MSB current source array will be calibrated. At first, the error current of the lowest MSB bit current (δ_1) will be obtained. The lowest MSB current (I_{MSB0}) is compared with I_{CMSB0} using the current mirrors and the current comparator. Then, SUBDAC operates to cancel out δ_0. δ_1 is obtained as a 11 bit digital value by an 11-step successive approximation process utilizing LSBDAC (8 bit) and CALDAC (3 bit) which are controlled by the current comparator output and the calibration logic. The simplified MSB calibration circuit for I_{MSB0} is shown in Fig. 6. The measurement is done twice, once in phase A and once in phase B as in the case of "Sub Calibration."

$$\begin{cases} 1:(1+m)=(I_{\text{MSB0}}+I_{\text{CALA+}}):(I_{\text{LSBs}}+I_{\text{CALA-}}+I_{\text{offset}}) \\ (1+m):1=(I_{\text{MSB0}}+I_{\text{CALB-}}+I_{\text{offset}}):(I_{\text{LSBs}}+I_{\text{CALB+}}) \end{cases} \tag{4}$$

$$\begin{cases} (1+m)(I_{\text{LSBs}}+\delta_1+I_{\text{CALA+}})=I_{\text{LSBs}}+I_{\text{CALA-}}+I_{\text{offset}} \\ (1+m)(I_{\text{LSBs}}+I_{\text{CALB+}})=I_{\text{LSBs}}+\delta_1+I_{\text{CALB-}}+I_{\text{offset}} \end{cases} \tag{5}$$

$$\begin{aligned} 2\delta_1 &\cong -\{(I_{\text{CALA+}}-I_{\text{CALA-}})-(I_{\text{CALB+}}-I_{\text{CALB-}})\} \\ &\cong -(I_{\text{CALA}}-I_{\text{CALB}}) \end{aligned} \tag{6}$$

In the next phase, the error current of the second lowest MSB current (δ_2) will be obtained. The second lowest MSB current (I_{MSB1}) is compared with the sum of I_{LSBs} and I_{MSB0}, then δ_2 is obtained as an 11bit digital value by 11-step successive approximation process and using δ_1 which was determined before. The simplified MSB calibration circuit for I_{MSB1} is shown in Fig. 7.

$$\begin{cases} 1:(1+m)=(I_{\text{MSB1}}+I_{\text{CALA+}}):(I_{\text{MSB0}}+I_{\text{LSBs}}+I_{\text{CALA-}}+I_{\text{offset}}) \\ (1+m):1=(I_{\text{MSB1}}+I_{\text{CALB-}}+I_{\text{offset}}):(I_{\text{MSB0}}+I_{\text{LSBs}}+I_{\text{CALB+}}) \end{cases} \tag{7}$$

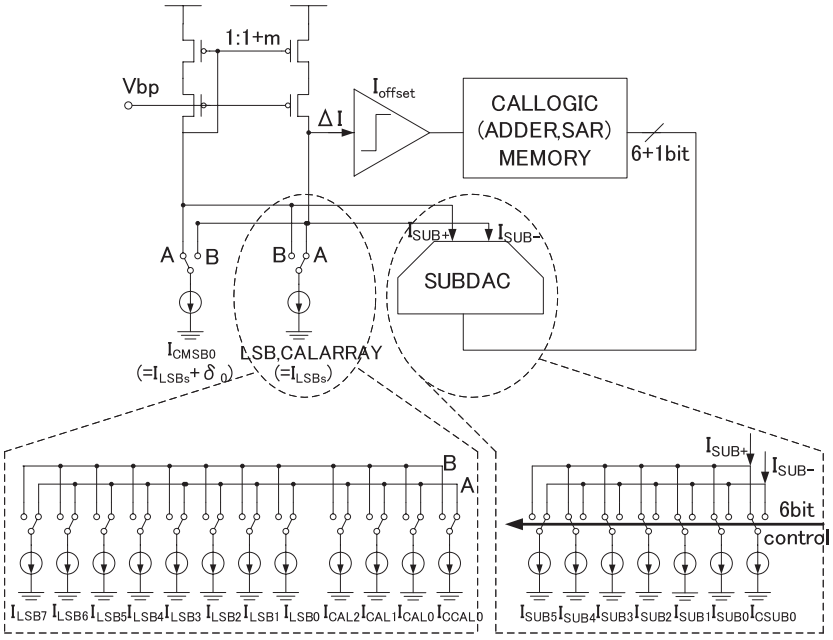

Fig. 5 SUB calibration circuit.

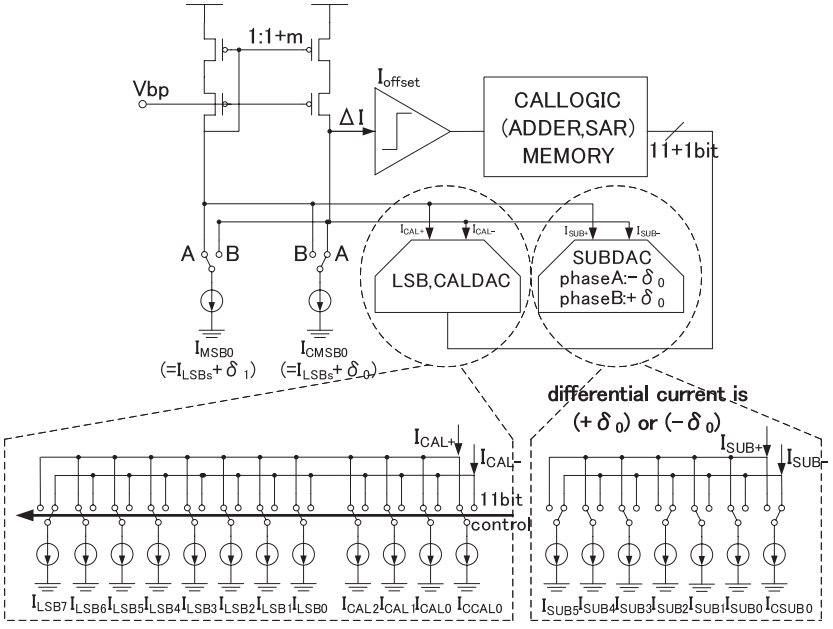

Fig. 6 MSB calibration circuit for I_{MSB0}.

$$\begin{cases}(1+m)(2I_{LSBs}+\delta_2+I_{CALA+})=2I_{LSBs}+\delta_1+I_{CALA-}+I_{offset}\\(1+m)(2I_{LSBs}+\delta_1+I_{CALB+})=2I_{LSBs}+\delta_2+I_{CALB-}+I_{offset}\end{cases} \tag{8}$$

$$\begin{aligned}2\delta_2 &\cong 2\delta_1-\{(I_{CALA+}-I_{CALB-})-(I_{CALB+}-I_{CALB-})\}\\&\cong 2\delta_1-(I_{CALA}-I_{CALB})\end{aligned} \tag{9}$$

In the same way, the error current of the other MSB current sources can be determined with an 11-step successive approximation process and with the previously determined error currents for the lower MSBs, as shown in Eq. (12).

$$\begin{cases}1:(1+m)=(I_{MSBN}+I_{CALA+}):\\\quad\left(\sum_{i=0}^{N-1}I_{MSBi}+I_{LSBs}+I_{CALA-}+I_{offset}\right)\\(1+m):1=(I_{MSBN}+I_{CALB-}+I_{offset}):\\\quad\left(\sum_{i=0}^{N-1}I_{MSBi}+I_{LSBs}+I_{CALB+}\right)\end{cases} \tag{10}$$

$$\begin{cases} (1+m)(2^N I_{\mathrm{LSBs}} + \delta_{N+1} + I_{\mathrm{CALA+}}) \\ \quad = 2^N I_{\mathrm{LSBs}} + \sum_{i=1}^{N} \delta_i + I_{\mathrm{CALA-}} + I_{\mathrm{offset}} \\ (1+m)\left(2^N I_{\mathrm{LSBs}} + \sum_{i=1}^{N} \delta_i + I_{\mathrm{CALB+}}\right) \\ \quad = 2^N I_{\mathrm{LSBs}} + \delta_{N+1} + I_{\mathrm{CALB-}} + I_{\mathrm{offset}} \end{cases} \tag{11}$$

$$\begin{aligned} 2\delta_{N+1} &\cong \sum_{i=1}^{N} 2\delta_i - \{(I_{\mathrm{CALA+}} - I_{\mathrm{CALB-}}) - (I_{\mathrm{CALB+}} - I_{\mathrm{CALB-}})\} \\ &\cong \sum_{i=1}^{N} 2\delta_i - (I_{\mathrm{CALA}} - I_{\mathrm{CALB}}) \end{aligned} \tag{12}$$

2.3 During Normal Operation

The architecture for the normal conversion is shown in Fig. 8. Every MSB array error current is stored in a register. Other than in a conventional DAC, where the 8 bit DAC can produce output currents from 0 to 255I, this converter's 8 bit LSB ranges from 0 to 511I. This is because the MSB dummy current source is used for the 8 bit LSB conversion. If the MSB array current sources have no error, 8 bit LSB will range from 128I to 383I. Therefore, the MSB array can be calibrated in the large range of $-128I$ to $+128I$.

In the proposed calibration architecture, the format of the digital input has to be converted into "two's complement" format because digital signal processing is performed. The relation between the DAC digital format and twos complement format is given in Table 1. The DAC inputs are divided into the 6 bit MSB data and the 8 bit LSB data. The 6 bit MSB data is used as the input to the six MSB switches and six selectors. If the Nth selector's input is 0, the Nth selector's output is 0, and if the Nth selector's input is 1, the Nth selector's output is $2\delta_N$. All six selectors' outputs are 11 bit digital data. The LSB data is changed to 11 bit data by adding 3'b000 to the lowest 3 bits. Then, the format of LSB data is converted to twos complement. They are added to six selector's outputs and the format of its result (12 bit) is again converted back to the DAC format. The converted 12 bit data is used for the MSB dummy switch (1 bit), the LSB switches (8 bit) and the CAL switches (3 bit) from most significant bit to lowest. Either $+\delta_0$ or $-\delta_0$ is used as

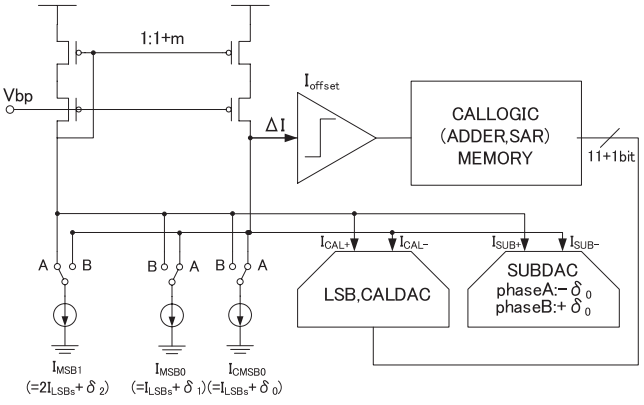

Fig. 7 MSB calibration circuit for I_{MSB1}.

Table 1 The relation of the format.

decimal value	DAC format	twos complement
8'd−128	8'b00000000	8'b10000000
8'd−127	8'b00000001	8'b10000001
～	～	～
8'd0	8'b10000000	8'b00000000
～	～	～
8'd126	8'b11111110	8'b01111110
8'd127	8'b11111111	8'b01111111

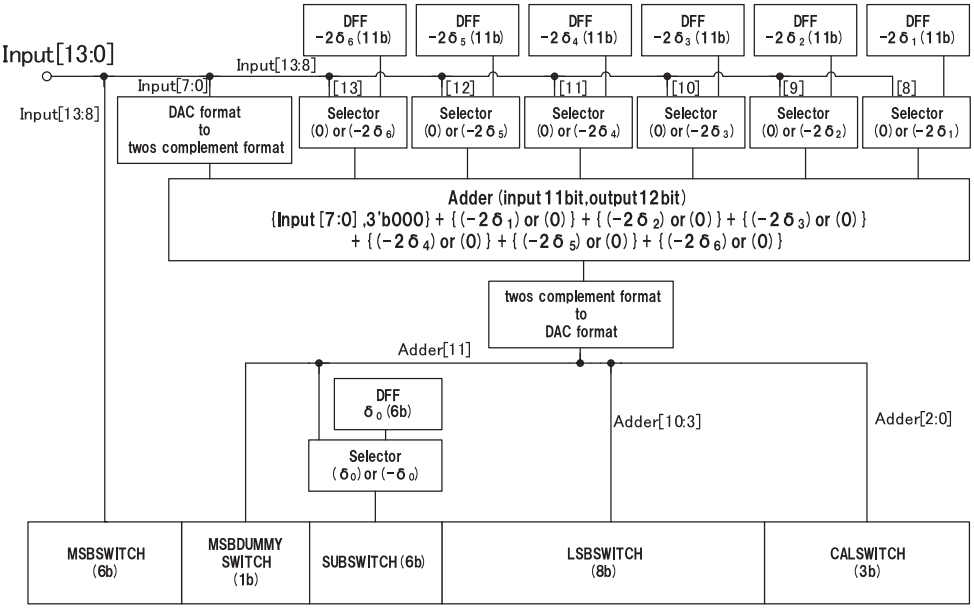

Fig. 8 Block diagram during normal conversion.

the input of the SUB switches (6 bit) depending on the MSB dummy switch.

Because all the error currents are added in the current correction, they should be digitized with at least two extra bits compared to LSBDAC. If they are digitized too coarsely, the quantization errors are accumulated and cause a large INL. Therefore, CALDAC should have the smallest current within the range of the LSB of LSBDAC and CALDAC together.

For this reason, MSBDAC is calibrated to 1/8 LSB and CALDAC is decided to be of 3 bit resolution. In the conventional calibration, a large calibration range leads to a large CALDAC area at the cost of a small calibrated MSBDAC area. However, in the proposed scheme, 8 bit LSBDAC is used for the current correction and the large calibration range (11 bit) is realized by CALDAC with only 3 bit resolution.

MAINDAC (LSBDAC) is used for current correction in addition to the normal conversion by adding input data (8 bit LSB data) to the error currents of 6 bit MSB array. Although the proposed digital calibration method requires the extra parts CALDAC, SUBDAC as well as the MSB dummy current source, the increase in area for this large calibration range is actually very small. The area of the current sources of CALDAC is only about 1/256 of the area required for the current sources of LSBDAC and 1/16 of the area for SUBDAC. The area of the MSB dummy current source is only about 1/64 of that of MSBDAC. To achieve 14 bit linearity without any calibration, the total current source area would be increased 128 times.

In the scheme of [4], the current correction was realized thorough the bias voltage of the current source. Therefore, each of the calibrated current sources needs a calibration DAC. This leads to the increase of the number of the calibration DACs. On the other hand, in this proposed calibration scheme the current correction is done at the output node. Because the error currents are merged in the digital domain and LSBDAC is used for the error correction, the additional calibration DAC area is very small.

3. Simulation Results

The proposed self-calibration architecture is realized in a 0.18 μm CMOS technology; the supply-voltage is 1.8 V. The simulations have been done using Verilog-AMS. The transistor-level models were used for all analog circuits such as the current sources, the switches, the current mirrors, and the current comparator in the simulation. On the other hand, the Verilog functional models were used for the digital circuits related to calibration. Mismatch currents were added based on Monte Carlo simulations.

The results of the Monte Carlo simulations are shown in Fig. 9. The standard deviation of the unit current of LS-

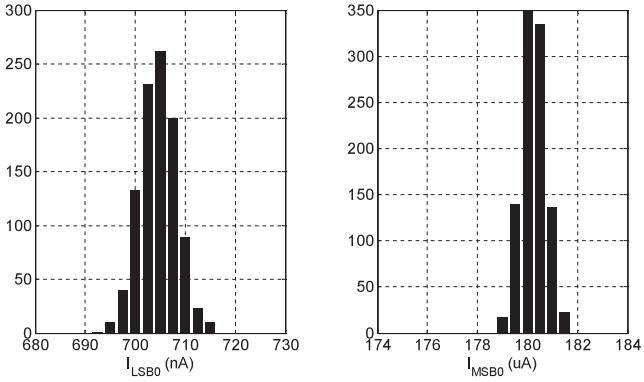

Fig. 9 The results of the Monte Carlo simulations of the current source.

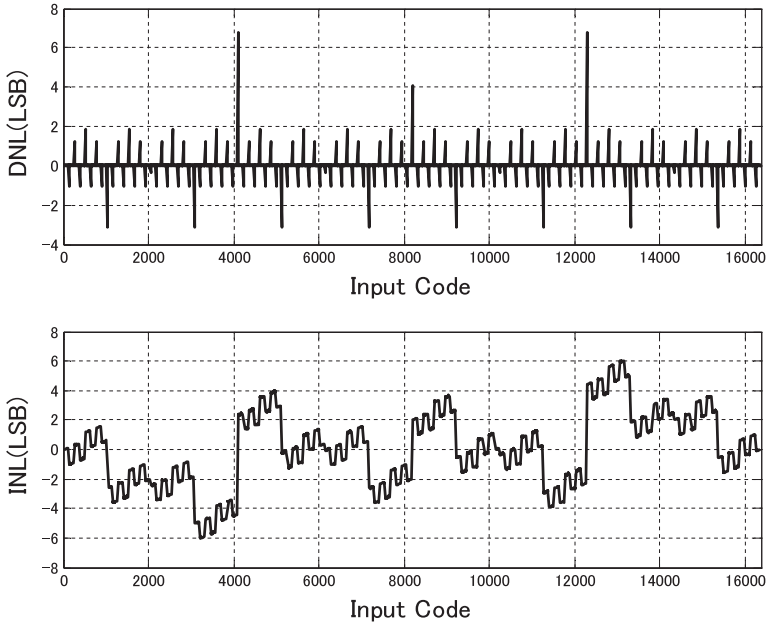

Fig. 10 DNL and INL profiles before calibration.

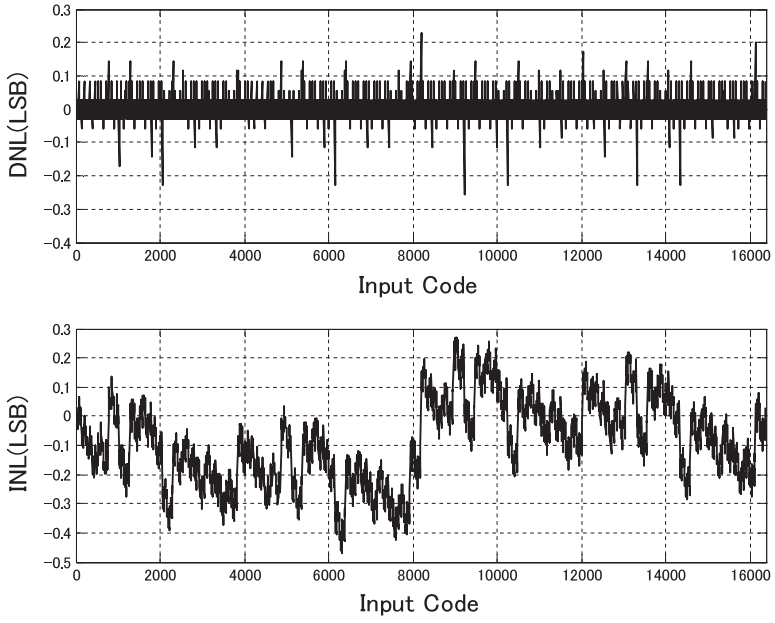

Fig. 11 DNL and INL profiles after calibration.

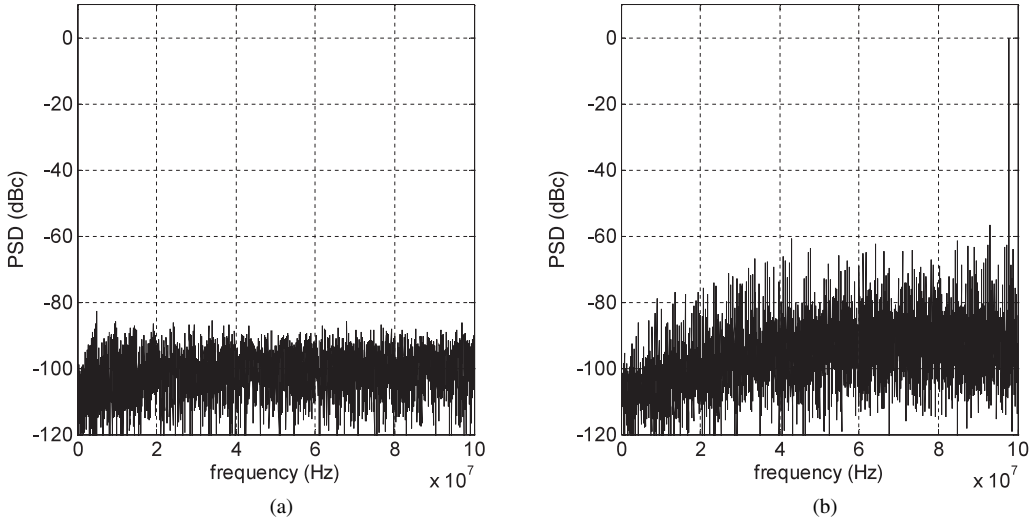

Fig. 12 Output spectrum with an input signal frequency of (a) 24 kHz, (b) 98 MHz.

BDAC ($=\sigma(I_{LSB0})/I_{LSB0}$) is 0.00522, and the standard deviation of the unit current of MSBDAC ($=\sigma(I_{MSB0})/I_{MSB0}$) is 0.00269.

DNL and INL profiles before calibration are presented in Fig. 10. DNL and INL before calibration are 6.80 LSB and 6.02 LSB, respectively. The linearity degrades in the codes where the MSB dummy switch and MSB array switches change due to current mismatches. Figure 8 shows that the linearity before calibration achieves only about 10 bit resolution. After calibration, DNL and INL are reduced to 0.26 LSB and 0.46 LSB, as shown in Fig. 11. The results indicate that the linearity improves by the proposed digital calibration architecture and 14 bit level is achieved. Figures 12 and 13 show the output spectrum after calibration at 200 Msps update rate for 24 kHz and 98 MHz input signal frequencies, respectively. The SFDR of the DAC are 83 dBc at 24 kHz and 57 dBc at 98 MHz. The SFDR performance degrades by the glitches and the feedthrough of the switches. However, by adding a simple return-to-zero circuit to the output of the DAC, the SFDR could be improved significantly.

4. Comparison with Other Digital Calibration Schemes

The comparison of the proposed digital calibration architecture with other digital calibration techniques is shown in Table 2. Using a current comparator for current error measurements, as is done in this scheme, leads to a small area and low cost compared to other schemes using ΣΔ-ADCs. In addition, the extra DACs required for calibration are only

Table 2 Comparison of digital calibration.

Reference	CAL ADC	CAL DAC	Memory	MSBbit	CALbit	Area	Power	Max. Update Rate
[1]	Off Chip 16bit Σ Δ ADC	8bDAC+6bDAC	8 × 63	6b	8b	0.1mm^2	16.7mW @100Msps	180MSps
[2]	On Chip Σ Δ ADC	12bDAC	12 × 15	4b	12b	11.8mm^2	180mW @100MSps	200MSps
[3]	On Chip Σ Δ ADC	8bDAC × 16	8 × 16	4b	8b	2.88mm^2	105mW	150MSps
[4]	Current Comparator	6bDAC × 4	6 × 4	4b	6b	1mm^2	20mW	100MSps
This Work	Current Comparator	3bDAC+6bDAC	11 × 6	6b	11b	0.7mm^2	21mW (analog)	200MSps (simulation)

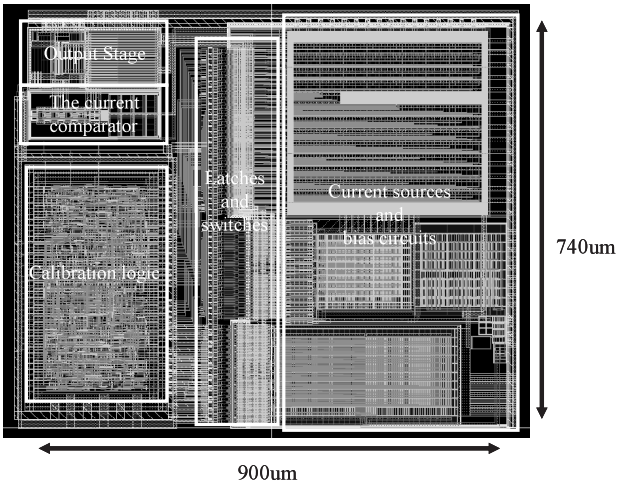

Fig. 13 The proposed calibrated DAC layout.

the 6 bit "SUBDAC" and the 3 bit "CALDAC," which are smaller than what the other groups use. The DAC reported in [1] has a smaller die area, however, it needs an off chip 16 bit ΣΔ ADC.

Both the 6 corrected current sources ("MSBbit") and the 11 bit calibration range ("CALbit") are large. Therefore, the area of "MAINDAC" can also become smaller. The proposed calibrated DAC area is estimated carefully from layout and synthesis as shown in Fig. 13. This small area leads to low power consumption and fast sampling rate.

5. Conclusions

A new digital calibration scheme for a current-steering DAC has been proposed. This scheme has been applied to a binary-weighted DAC which is — due to the minimal number of current-sources — most suitable for a fast digital calibration. Because this scheme uses a simple current comparator for the current measurement instead of a high-resolution ADC, a fast calibration cycle was attained and the additional circuitry could be kept minimal. Furthermore, using the LSB part of the DAC for both the error correction scheme as well as for the normal conversion, leads to a minimal increase of die-area. The additional circuits required for the digital calibration are only a 6 bit DAC and a 3 bit DAC. Nevertheless, the calibration range is large compared to other calibration techniques described in the literature: from −128 LSB to +128 LSB.

Simulation results have revealed that the proposed digital calibration scheme can be used to achieve full 14 bit static accuracy. Before calibration, DNL and INL are 6.80 LSB and 6.02 LSB, respectively. After calibration, both DNL and INL are greatly improved to 0.26 LSB and 0.46 LSB, respectively.

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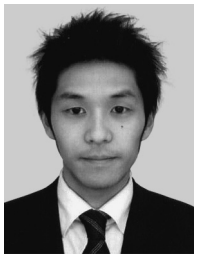

Yusuke Ikeda received the B.E. degree in Electrical and Electronic Engineering from Tokyo Institute of Technology, Japan, in 2005. He is currently studying toward the M.E. degree in Physical Electronics Engineering from Tokyo Institute of Technology. His research interests include the design of analog CMOS integrated circuits.

Akira Matsuzawa received B.S., M.S., and Ph.D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and Mixed Signal LSI technologies; ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, digital read-channel technologies for DVD systems, ultra-high speed interface technologies for metal and optical fibers, a boundary scan technology, and CAD technology. He was also responsible for the development of low power LSI technology, ASIC libraries, analog CMOS devices, SOI devices. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is a professor on physical electronics. Currently he is researching in mixed signal technologies; CMOS wireless transceiver, RF CMOS circuit design, data converters, and organic EL drivers. He served the guest editor in chief for special issue on analog LSI technology of IEICE transactions on electronics in 1992, 1997, 2005, and 2006, the vice-program chairman for International Conference on Solid State Devices and Materials (SSDM) in 1999 and 2000, the Co-Chairman for Low Power Electronics Workshop in 1995, a member of program committee for analog technology in ISSCC and the guest editor for special issues of IEEE Transactions on Electron Devices. He has published 26 technical journal papers and 48 international conference papers. He is co-author of 10 books. He holds 34 registered Japan patents and 65 US and EPC patents. He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He is an IEEE Fellow since 2002.