

A 0.05-mm² 110- μ W 10-b Self-Calibrating Successive Approximation ADC Core in 0.18- μ m CMOS

[†]Yasuhide Kuramochi, ^{††}Akira Matsuzawa, and [†]Masayuki Kawabata

[†] Advantest Laboratories Ltd.
48-2, Matsubara, Kamiyashi, Aobaku,
Sendai, Miyagi, Japan
yasuhide.kuramochi@jp.advantest.com

^{††}Department of Physical Electronics
Tokyo Institute of Technology
2-12-1, O-okayama, Meguroku, Tokyo, 152-8552, Japan
matsu@ssc.pe.titech.ac.jp

Abstract - We present a 10-bit 1-MS/s successive approximation analog-to-digital converter core including a charge redistribution digital-to-analog converter and a comparator. A new linearity calibration technique enables use of a nearly minimum capacitor limited by kT/C noise. The ADC core without Digital blocks has been fabricated in a 0.18- μ m CMOS process and consumes 110 μ W at 1.8 V power supply. With the calibration it achieves 9.0-dB improvement of SNDR and 23.3dB improvement of SFDR. The measured SNDR and SFDR are 51.1 dB and 69.8 dB respectively.

I. INTRODUCTION

Successive approximation resistor type analog-to-digital converter (SAR ADC) enables the implementation of a low power, small area, highly flexible ADC. As for the speed of high resolution SAR ADC, improvements in technologies make it possible to use SAR ADC for Applications around several tens of megahertz. For higher frequency Applications, parallel architectures like a interleaved ADC are used. Additionally high integration of digital circuits enables complex calibration for ADCs. Therefore the interleaved ADCs have been applied to many mixed-signal systems. However parallel architectures need large area. Usable area in a LSI limits the speed of interleaved ADC. So the area of a unit ADC must be reduced for high frequency applications. This paper presents a very small size (0.05mm²) ADC core using a simple self-calibration technique.

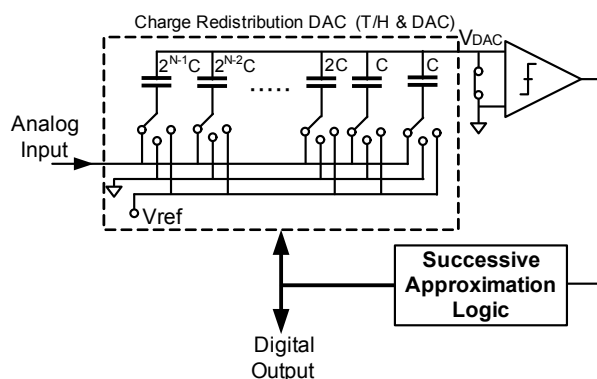


Fig. 1. Successive Approximation A/D Converter

II. CIRCUIT DESIGN

A. Charge Redistribution D/A Converter

A conventional SAR ADC is shown in Fig.1. The ADC is composed of a simple capacitive DAC, a comparator and successive approximation logic. Because no components with large static currents like an opamp are used, a low power ADC can be realized easily. As for the area, the capacitive DAC is dominant. To shrink the area of the ADC, the total capacitor must be decreased as much as possible. However the minimum capacitor of the DAC is decided by a kT/C noise limit. As shown in Fig.2, a desired Signal-to-Noise Ratio (SNR) of the SAR ADC decides the value of the DAC output capacitors. Therefore the total capacitor of the DAC should be designed to be a minimum capacitance that the SNR allows. Using a binary N-bit DAC, 2^N capacitors are needed. So the capacitance of a unit capacitor must be small [1]. A low resolution ADC (6 bits) using SAR technology has been used to realize a small ADC (0.06mm² with digital) [2]. Also Ref [2] applied a technique like a C-2C DAC. This C-2C type DAC with series capacitors can realize a small area. A N-bit DAC model composed of series and parallel binary capacitors is shown in Fig.3. It is divided in unit DACs that have one series capacitor and parallel binary capacitors. The total number of capacitors depends on the number of parallel capacitors in the unit DAC. Its relationship between parallel capacitors and DAC resolution is indicated in Fig.4. Thus a DAC with $k=2$ and $k=3$ parallel capacitors is effective in solving the area problem. If MIM capacitors are used as series capacitor, a linearity error caused by a bottom capacitance should be considered. The error of the bottom capacitor depends on the total capacitors at node "A". The large parasitic capacitance at the node is desirable. In this paper, 3 bits parallel ($k=3$) capacitors are used. As shown in Fig.5, the main DAC is composed of 10 bits resolution. The unit capacitor size is 20fF and the full scale voltage is 2.2Vpp (differential). The total capacitance at the comparator input node becomes 320*2 fF(differential).

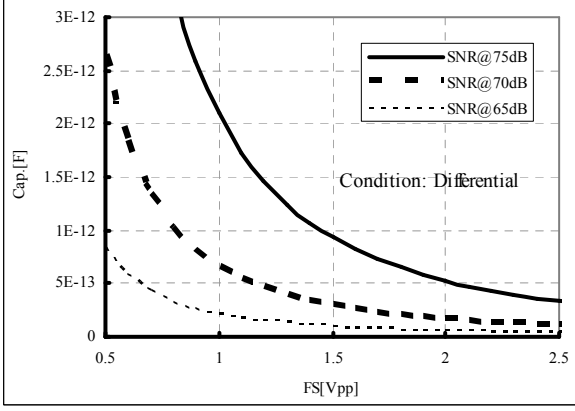


Fig. 2. Minimum Capacitance at the Input Node of a Comparator

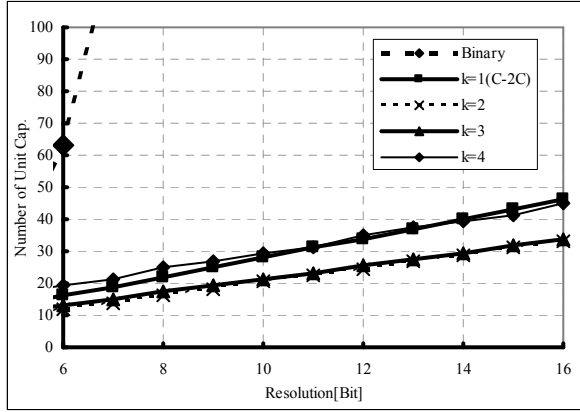


Fig. 4. The Number of Capacitors for a Charge Redistribution DAC

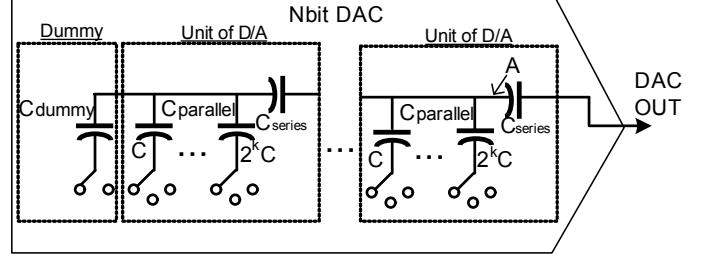


Fig. 3. N bit D/A Converter with Series Capacitor

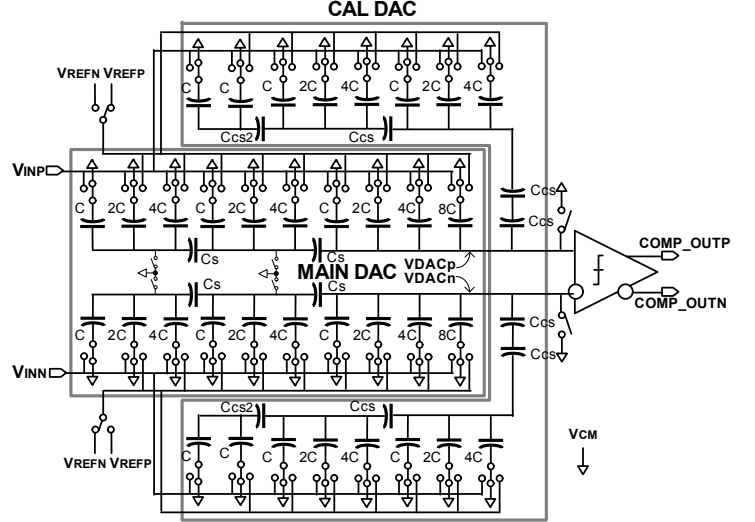


Fig. 5. Small Size Successive Approximation A/D Converter Core (Charge Redistribution D/A Converter and Comparator)

B. Calibration

Minimizing the unit capacitance and the total capacitance at the comparator input, will cause the mismatch error that is proportional to $1/W$ and the sensitivity to parasitic elements to increase in contribution considerably. However, in this paper, the dummy capacitors that are aligned around the capacitors of the DAC are removed, to shrink the area of the ADC. Linearity problems are solved with a calibration.

One calibration technique is reference voltage tuning using resistor ladder, shown in [3], [4]. Another technique is the use of capacitive calibration DAC [5]. This technique has a characteristic of low power. This section describes a new calibration technique using a capacitive DAC.

The calibration DAC (CAL DAC) is shown in Fig.6. This CAL DAC is connected to the output of the MAIN DAC. In this paper, the range of calibration is designed from -16LSB to 16LSB with 1/4LSB Step. The calibration system and its operation are shown in Fig.6. The measurements of capacitor mismatches error are executed (Fig.6 (a)). In this phase, the measurement controller block sets up the main DAC to output the error caused by mismatch error of capacitors. The errors

are measured by the CAL DAC operating as SAR ADC. Then the measured data are written to the cal memory. The data are called by the main SAR logic and the errors of the main DAC are calibrated by the CAL DAC (Fig.6 (b)). The detail of measurement sequences are as follows. First all capacitors are discharged to the common voltage, V_{CM} . Then, shown in Fig.7 (a), all the capacitors of the main DAC are connected to V_{CM} . Next, the CAL DAC operates like a SAR ADC and searches the offset voltage, V_{OFFSET} . The next phase is the measurement of the linearity error. Figure 7(b) shows that of k^{th} bit error, ΔC_{k_err} . In this case, the output voltage of the DAC is expressed as follows.

$$V_{DAC} = \frac{\{2C_k + C_{eq(k+1-N)}\} \cdot V_{CM}}{\{2C_k + C_{eq(k+1-N)}\} + \Delta C_{k_err} + C_{cal}} + \frac{(\Delta C_{k_err} \cdot V_{REF_CAL} + C_{cal} \cdot V_{REF_CAL})}{\{2C_k + C_{eq(k+1-N)}\} + \Delta C_{k_err} + C_{cal}} \quad (1)$$

Then the V_{DAC} approximates the V_{CM} with the SAR algorithm. The calibration data can be obtained as follows.

$$V_{REF_CAL} = V_{REFN}, \quad C_{cal} = \Delta C_{k_err} \quad (2)$$

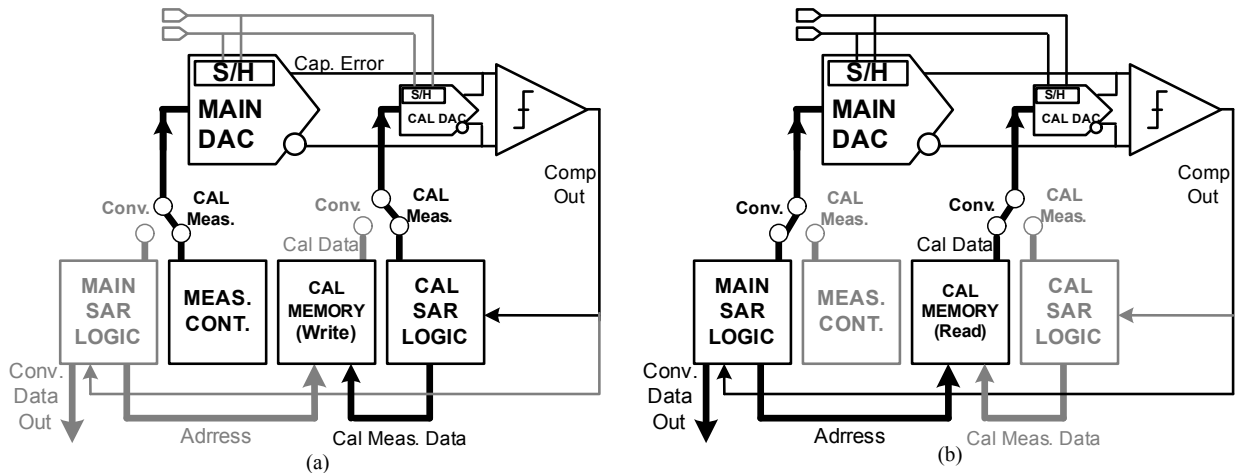


Fig. 6. System Configuration (a) Calibration Mode (b) Conversion Mode

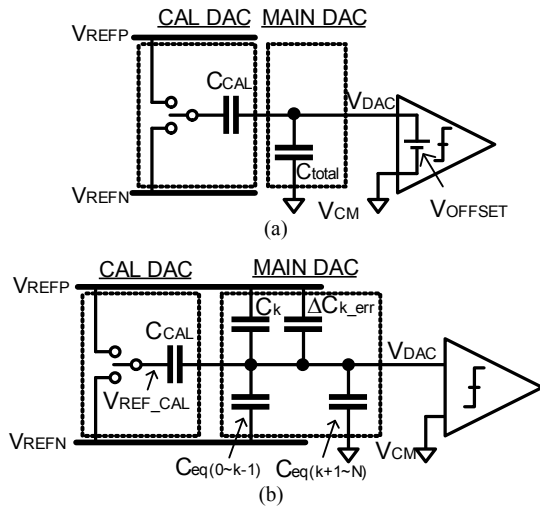


Fig. 7. Error Measurement (a) Comparator Offset (b) Linearity

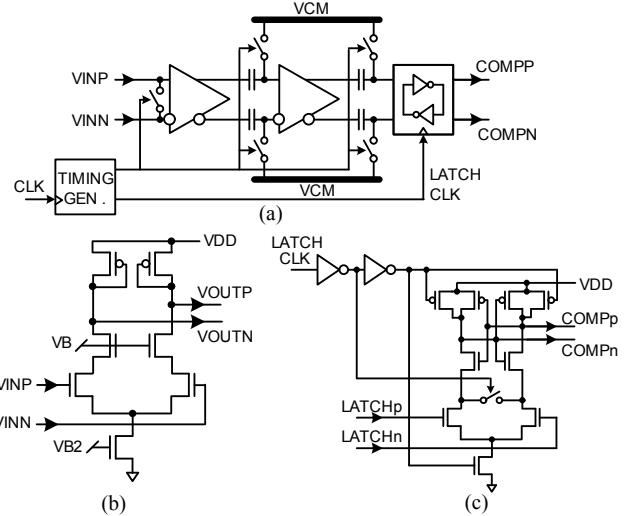


Fig. 8. Latched Comparator (a) Whole Circuit (b) preamplifier (c) latch

where $V_{CM} = (V_{REFP} + V_{REFN})/2$, $C_k = C_{eq(0-k-1)}$. Note that $C_{eq(k+1-N)}$ is the equivalent capacitance from C_{k+1} to C_N , $C_{eq(0-k-1)}$ is the equivalent capacitance from C_0 to C_{k-1} and C_k is the capacitance of k^{th} bit. With the same process, the calibrations are executed from k^{th} bit to N^{th} bit. In this paper, the upper 6 bits are calibrated. The measurement data duplicate between k^{th} bit and $(k+1)^{th}$ bit. Therefore these data are calculated and separated beforehand and written to the cal memory.

C. Comparator

The comparator and its components are shown in Fig. 8. The comparator is composed of two preamplifiers (Fig. 8 (b)) and a latch (Fig. 8(c)). Each preamplifier employs output offset cancellation. The timing generator generates the latch clock and the reset clock to minimize the propagation delay of the comparator. The preamplifier has PMOS diode loads and cascode connection to decrease the mirror capacitance and to isolate the input from the output. Some conventional latches generate a large kickback noise when the latch goes to the ON or OFF state. The kickback noise influences the output of the preamplifier, especially in the OFF state. To decrease the differential mode noise, the drain of the differential pair is

connected first. Then the latch turns to OFF state. Using this technique, the differential noise is suppressed effectively. With the simulation it achieves 86% noise improvement. This is suitable for a high speed ADC. The propagation time is designed to become less than 240ps (1/2 LSB input).

D. Control Logic

The SAR logic of the conversion cycle is the conventional SAR algorithm. The total number of clock cycles is 12 clock cycles (1 Sample, 11 Conversion). The control logic is needed to be flexibly programmable. So the SAR logic, the calibration logic, memory and other control circuits are composed with an off chip FPGA (Altera EP1K10). In this system, the conversion speed depends on the speed of the FPGA. In consideration of on chip implementation, only a 6x8 bits memory, SAR logic and one 8 bits Adder are needed. They occupy a very small area. If the digital circuits are implemented on a chip, this SAR ADC is expected to operate at 28MS/s according to SPECTRE simulation.

III. MEASUREMENTS RESULTS

The ADC chip was fabricated in a 0.18 μm CMOS process. The die photograph and Layout of the ADC is shown in Fig. 9. The active area of the ADC is 95 μm x 550 μm . With 12MHz system clock (1MS/s), the ADC consumes 110 μW . The calibrated ADC exhibits an SNDR and SFDR (@Nyquist) of 51.1dB and 69.8dB, respectively, as shown in Fig. 10 and Fig.11. With the calibration it achieves 9.0-dB improvement of SNDR and 23.3-dB improvement of SFDR. Though the CAL DAC has calibration resolution under 1 LSB, the SNDR for low-frequency input signal is 52.3dB. The accuracy is limited by underestimated comparator noise and gain. Finally, the measurements are summarized in Table I.

IV. CONCLUSION

A small size SAR ADC core has been presented that uses an internal small CAL DAC to achieve desensitization to mismatch for capacitors. The calibration technique enables to use a nearly minimum capacitor limited by kT/C noise. Using the capacitive type SAR ADC in the conversion and the calibration, extremely low power (110 μW) and small size (0.05mm²) can be realized.

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TABLE I
SUMMARY OF MEASUREMENTS

Process	0.18 μm , 1 poly, 6metal CMOS
Resolution	10bits
Active Area	95 μm x 550 μm
Sampling Rate	1MSps
Analog Power	110 μW @1.8V
SNDR @nyquist	51.1dB
SFDR @nyquist	69.8dB

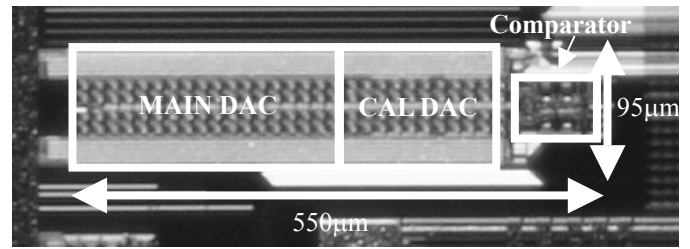


Fig. 9. Die Photo and Layout

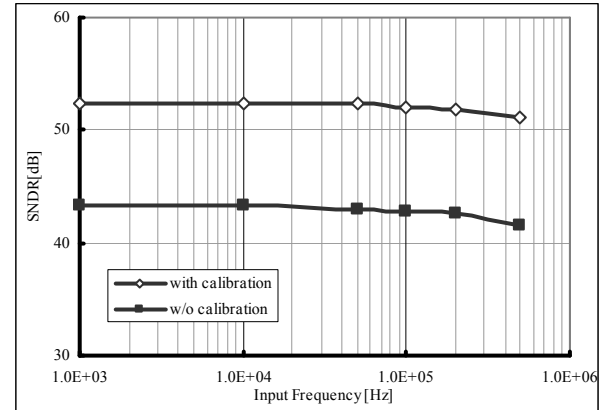


Fig. 10. Measured SNDR versus Input Frequency

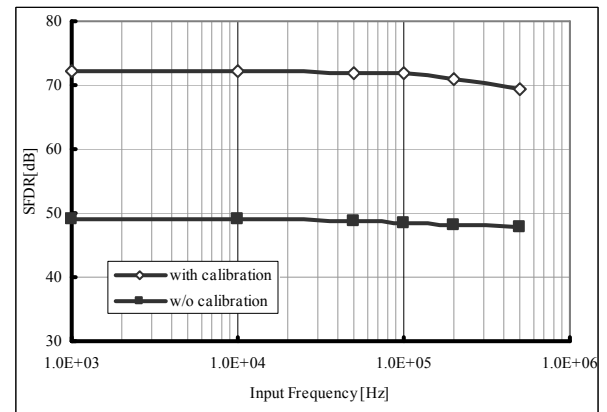


Fig. 11. Measured SFDR versus Input Frequency