A 0.05-mm^2 110-µW 10-b Self-Calibrating Successive Approximation ADC Core in 0.18-µm CMOS

Yasuhide Kuramochi[1,2], Akira Matsuzawa[2], and Masayuki Kawabata[1]

1 Advantest Laboratories Ltd., Miyagi, Japan
2 Tokyo Institute of Technology , Tokyo, Japan

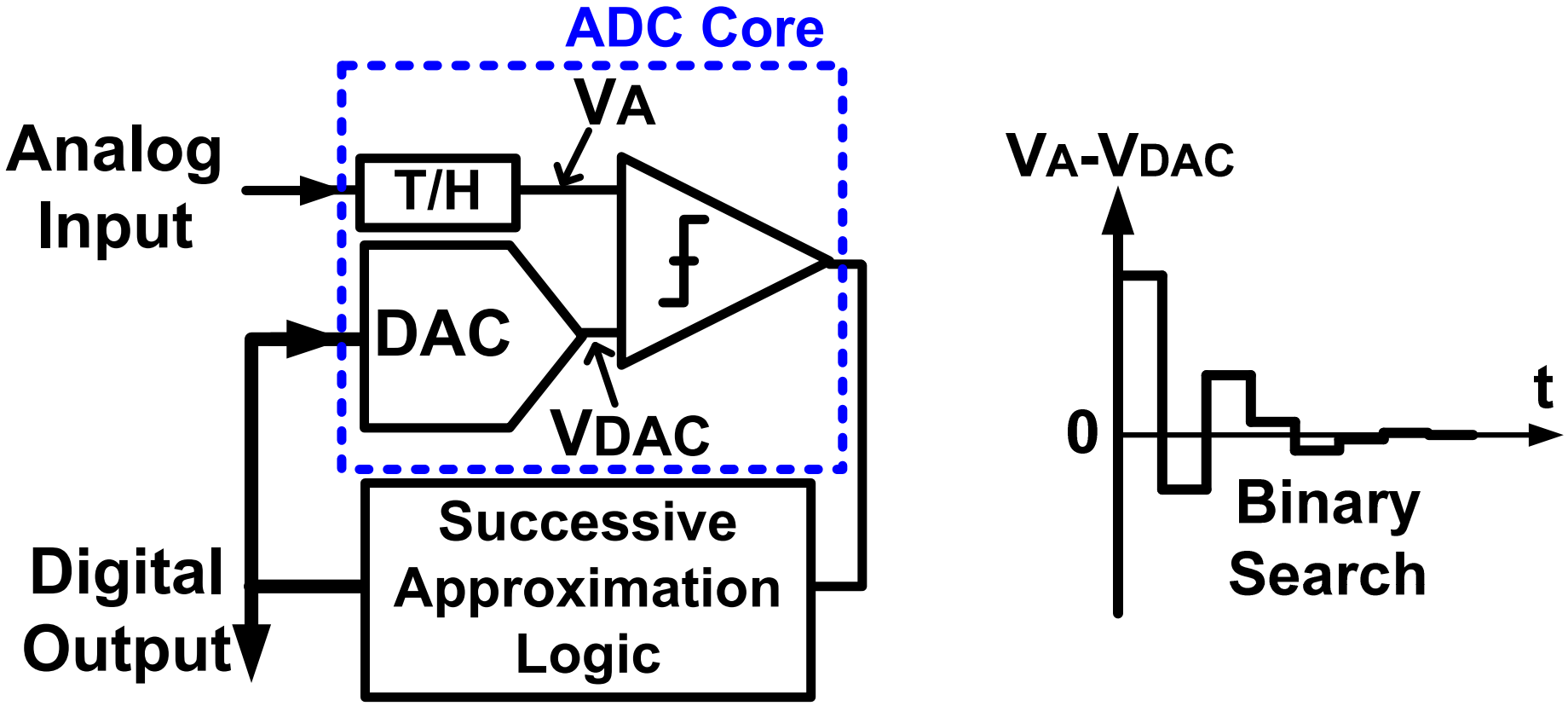
ADVANTEST®

Matsuzawa & Okada Lab

Outline

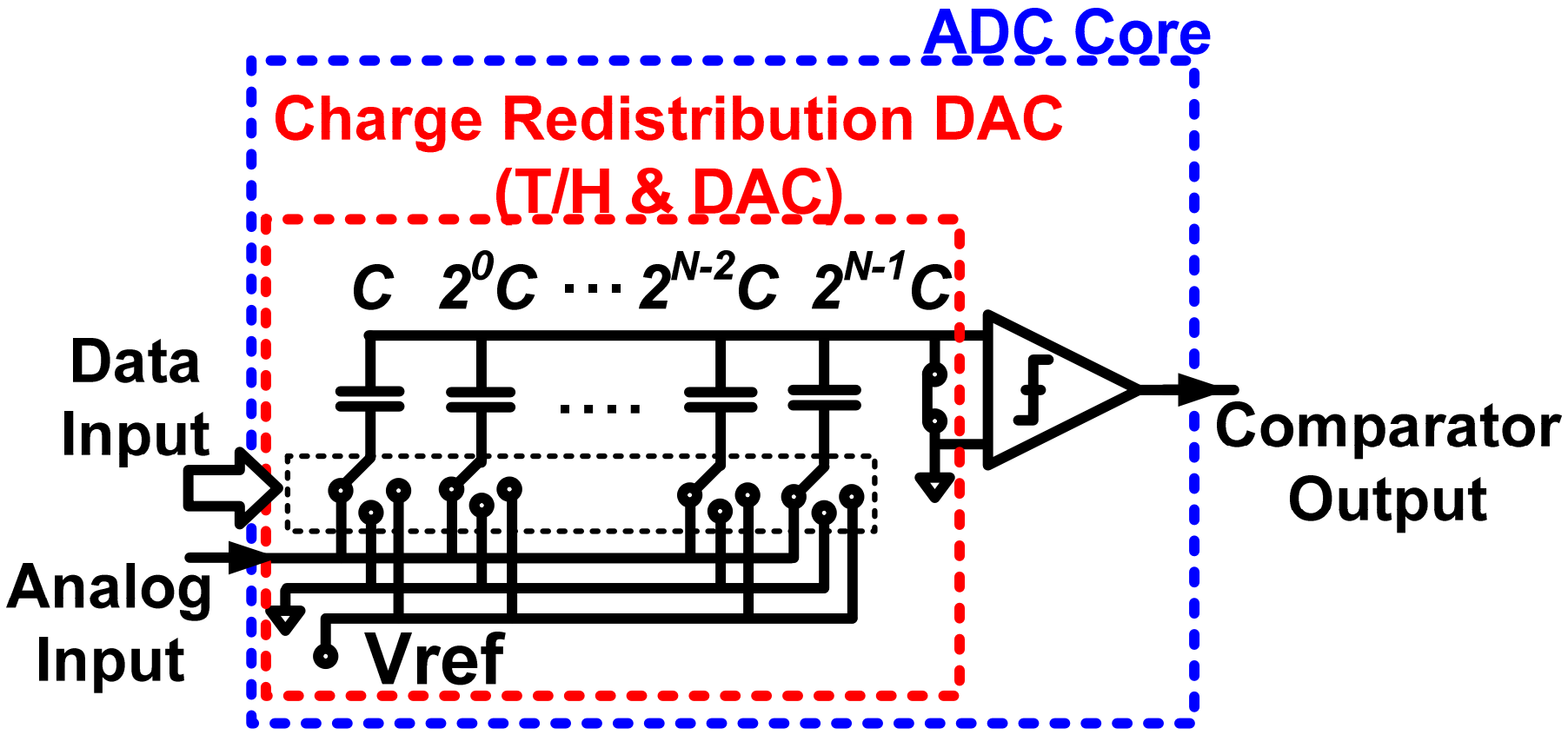
- **Background**
- **ADC core architecture**
- **Calibration system**
- **Measurement results**
- **Conclusions**

SAR ADC



- SAR=> Small, low power, wide input range
  => Suitable for BIST

Charge Redistribution DAC

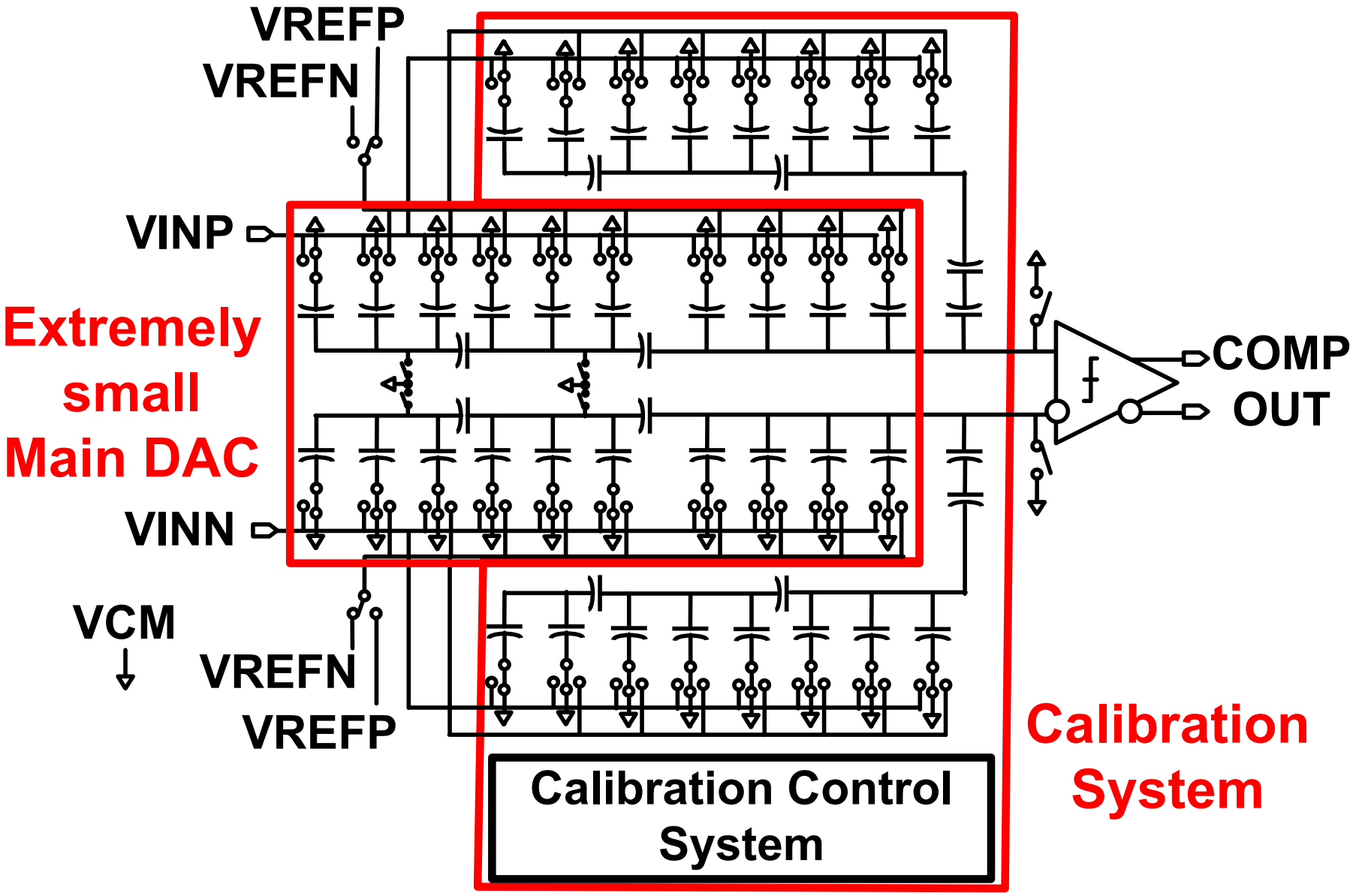


- Capacitive DAC area is dominant in ADC core
- DAC architecture should be chosen to be as small as possible

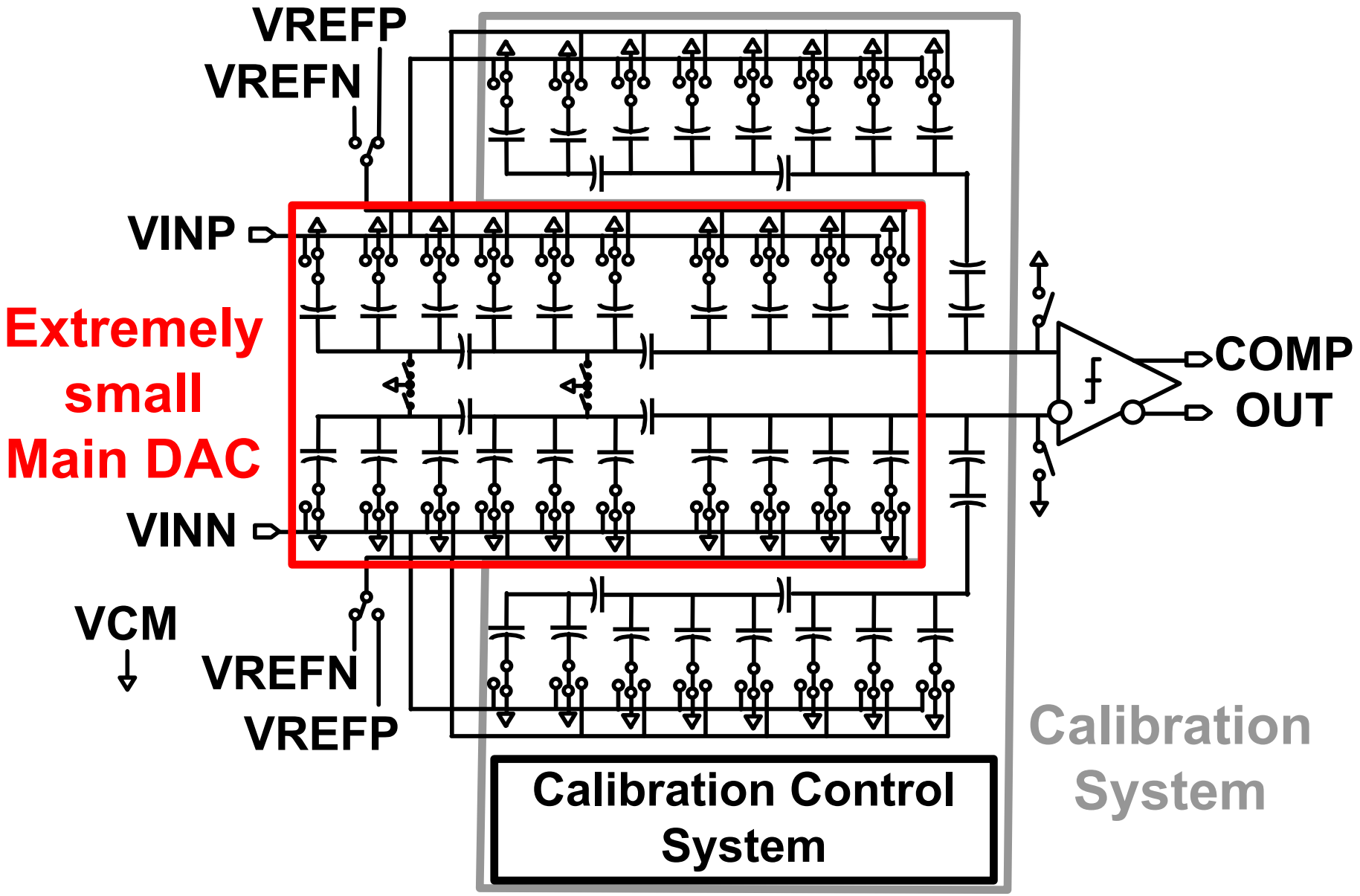
Outline

- Background
- **ADC core architecture**
- Calibration system
- Measurement results
- Conclusions

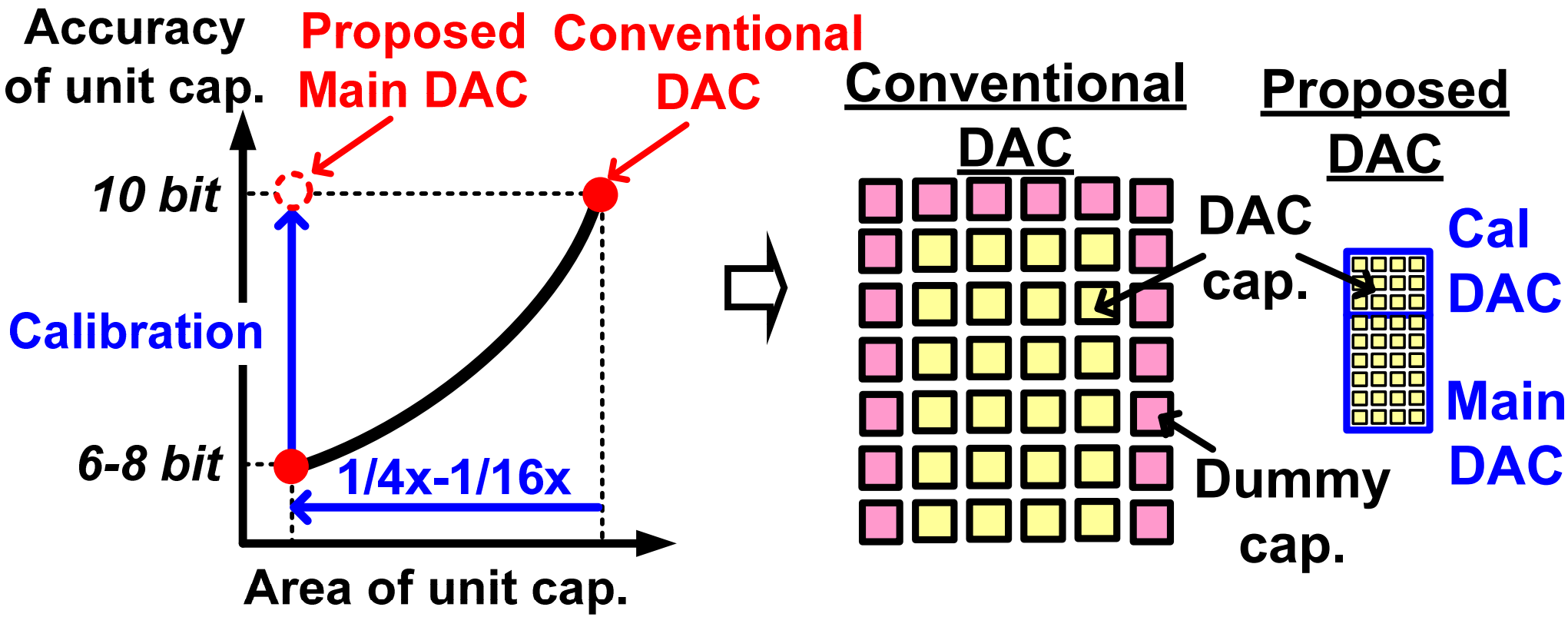
Proposed ADC Core Circuitry



ADC Core Circuitry

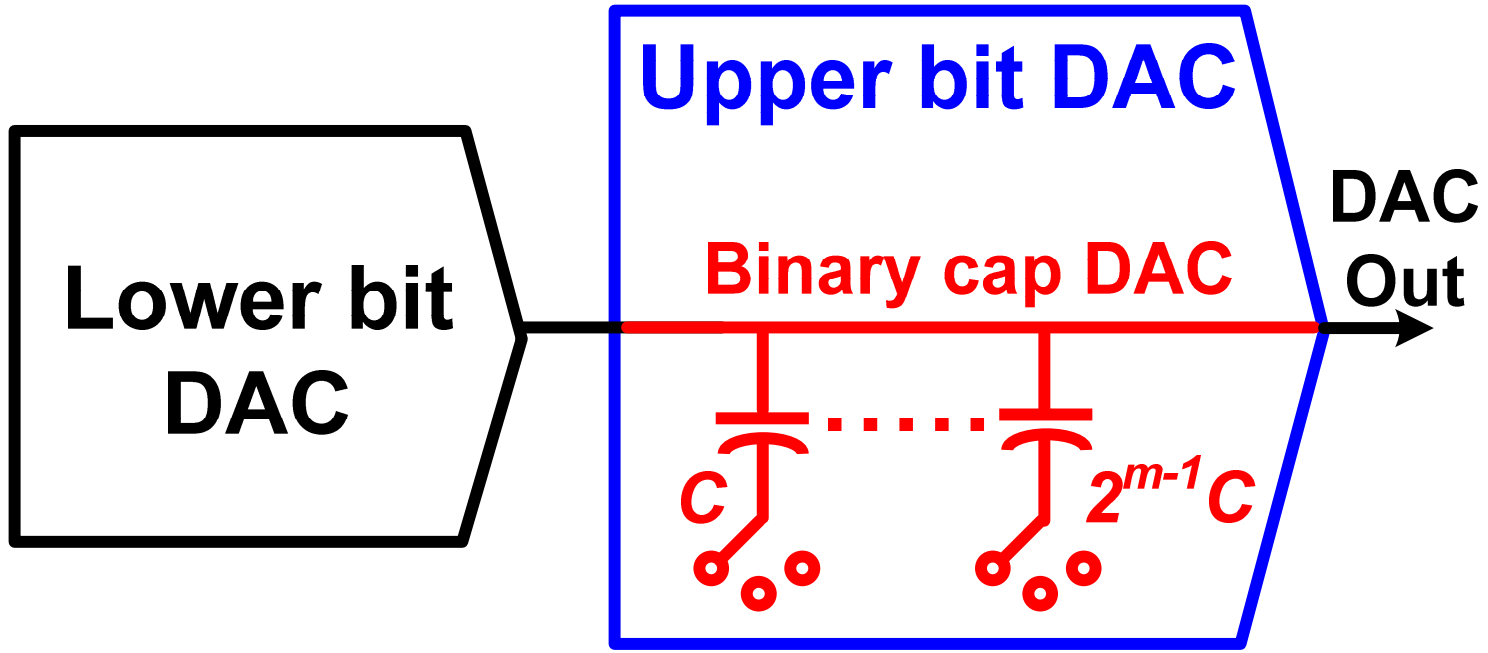


Realizing Small DAC



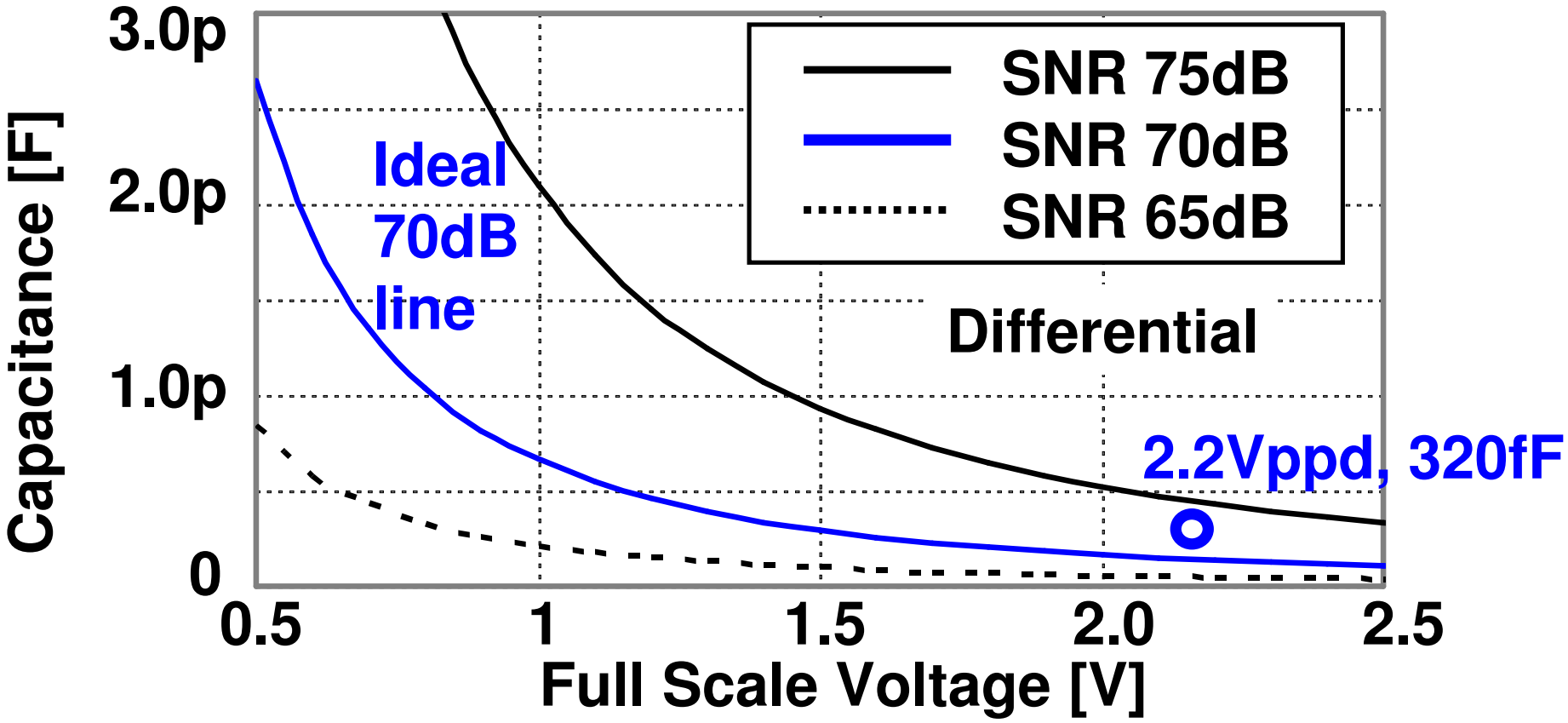
- Decreasing the area of DAC
  => Small unit capacitor: *C*=20fF
  No dummy capacitor around DAC
  => Calibration is inevitable for small DAC

Upper Bit DAC Architecture



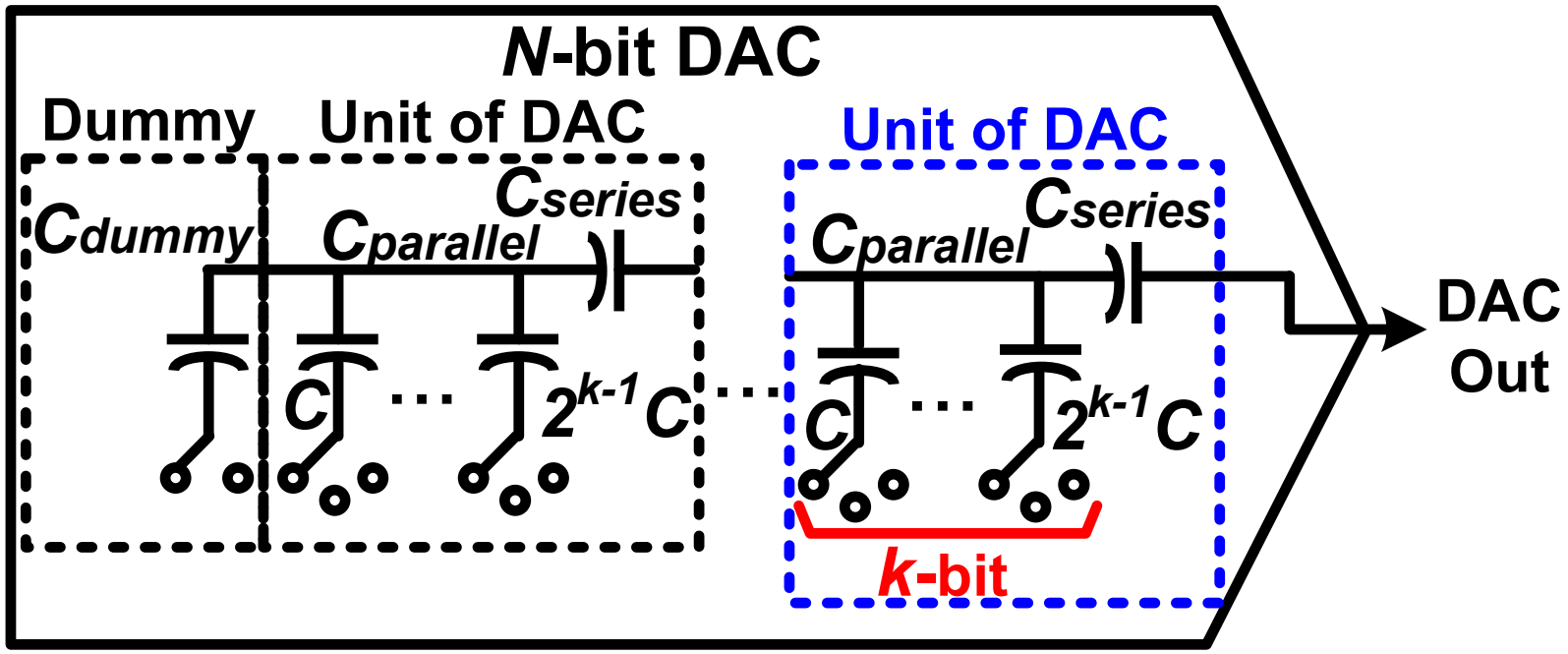
- SNR is limited by total capacitance at DAC Out node
- To increase total capacitance, the upper bit DAC is composed of binary capacitor DAC

Limitation of SNR



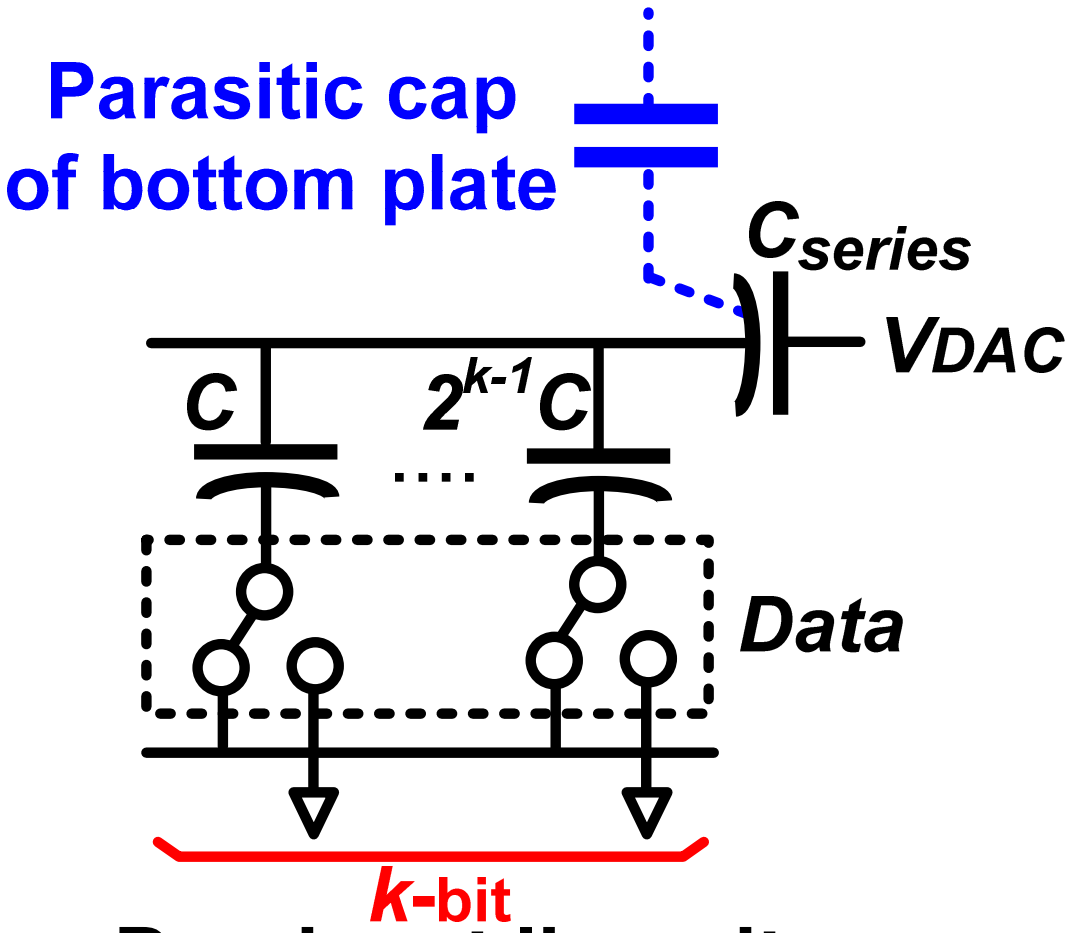
- Realizing small upper bit DAC, small capacitors close to noise limitation are chosen
- 4-bit binary(8C, 4C, 2C, C) upper bit DAC

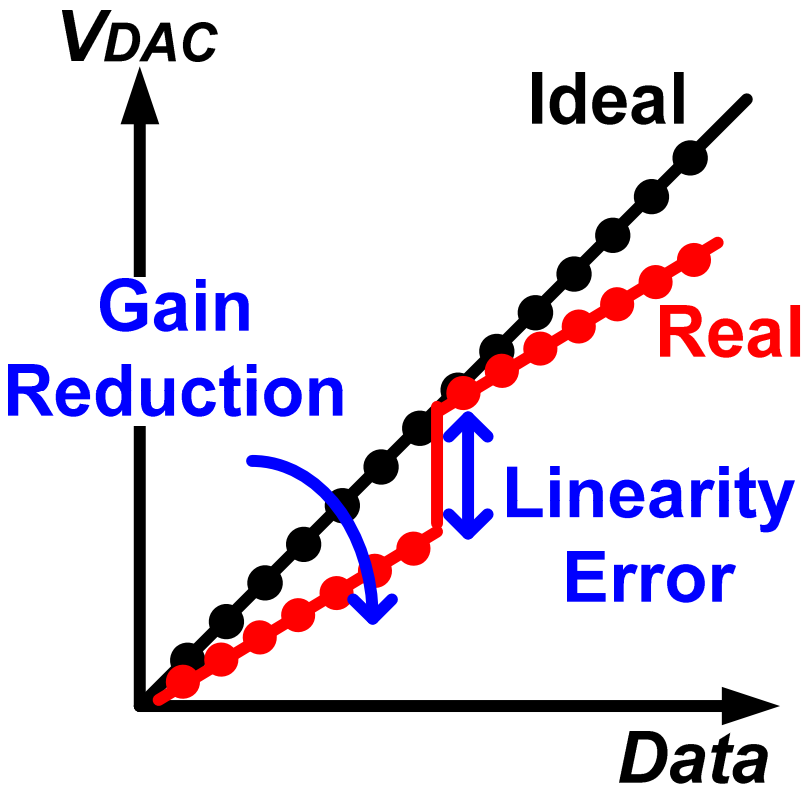
Lower Bit DAC Architecture



- Charge redistribution DAC is divided into unit DAC blocks using unit capacitors
- N bits DAC can be realized by series connection of *k*-bit unit DAC

Linearity Error of Unit DAC

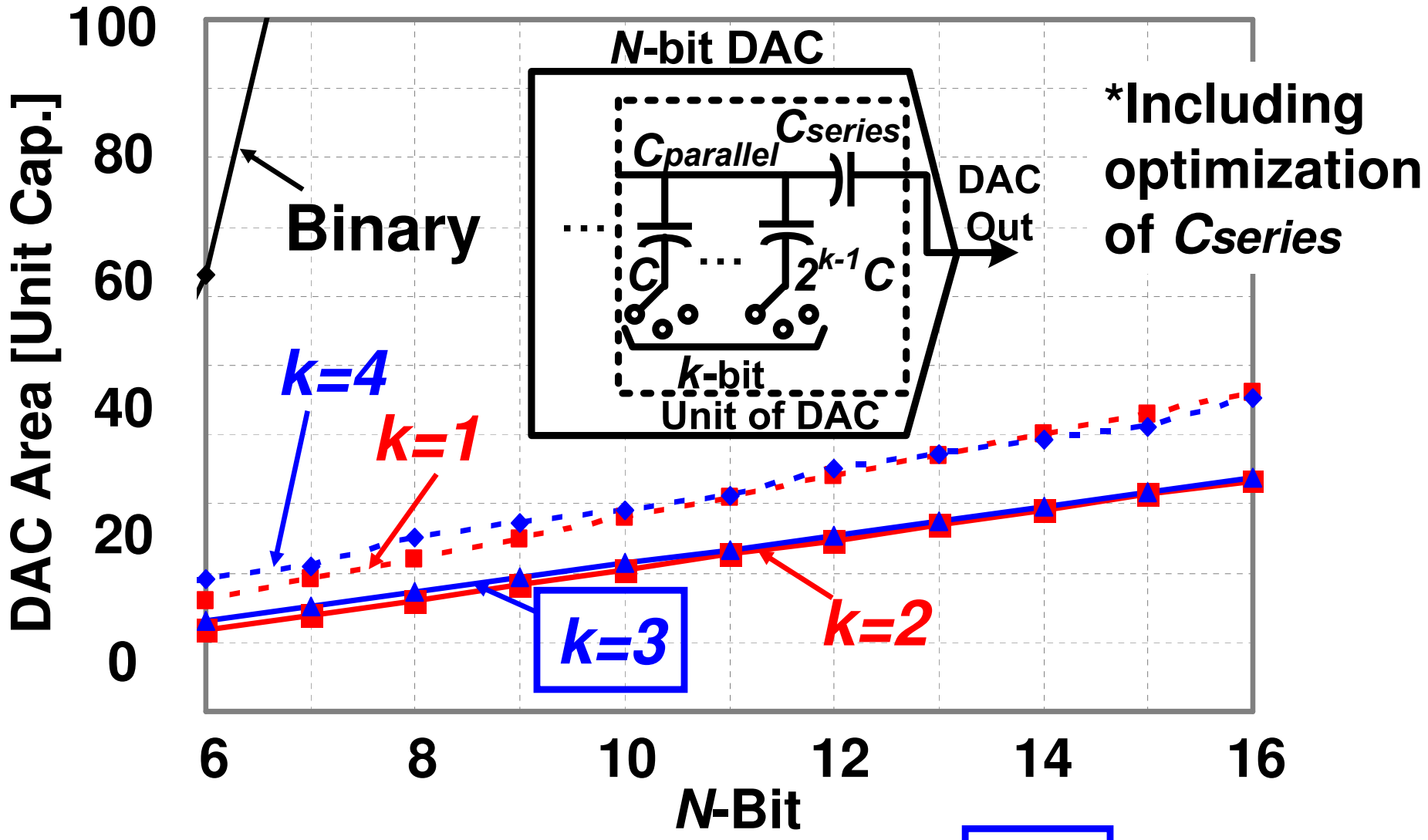




- Dominant linearity error is caused by parasitic bottom capacitor

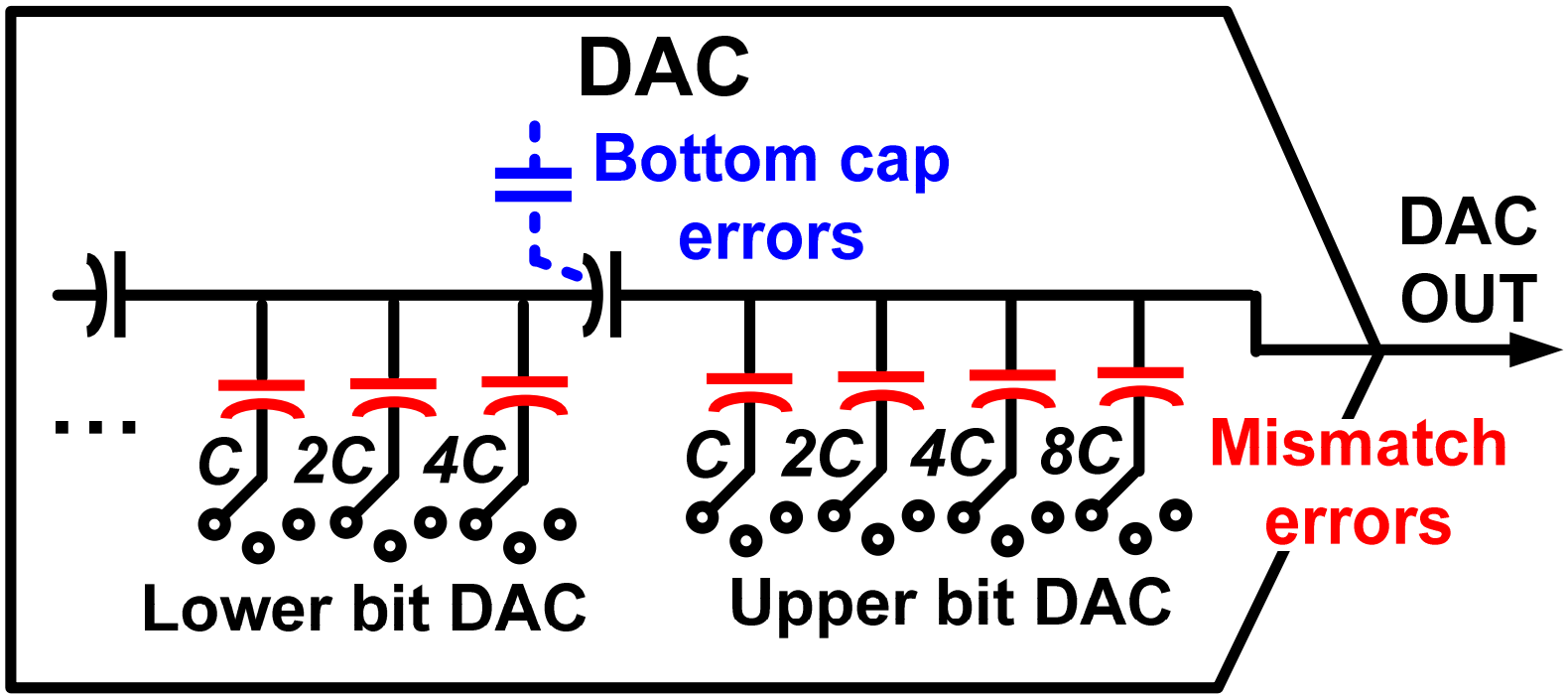
  => Large "*k*" is better for linearity

Size Comparison



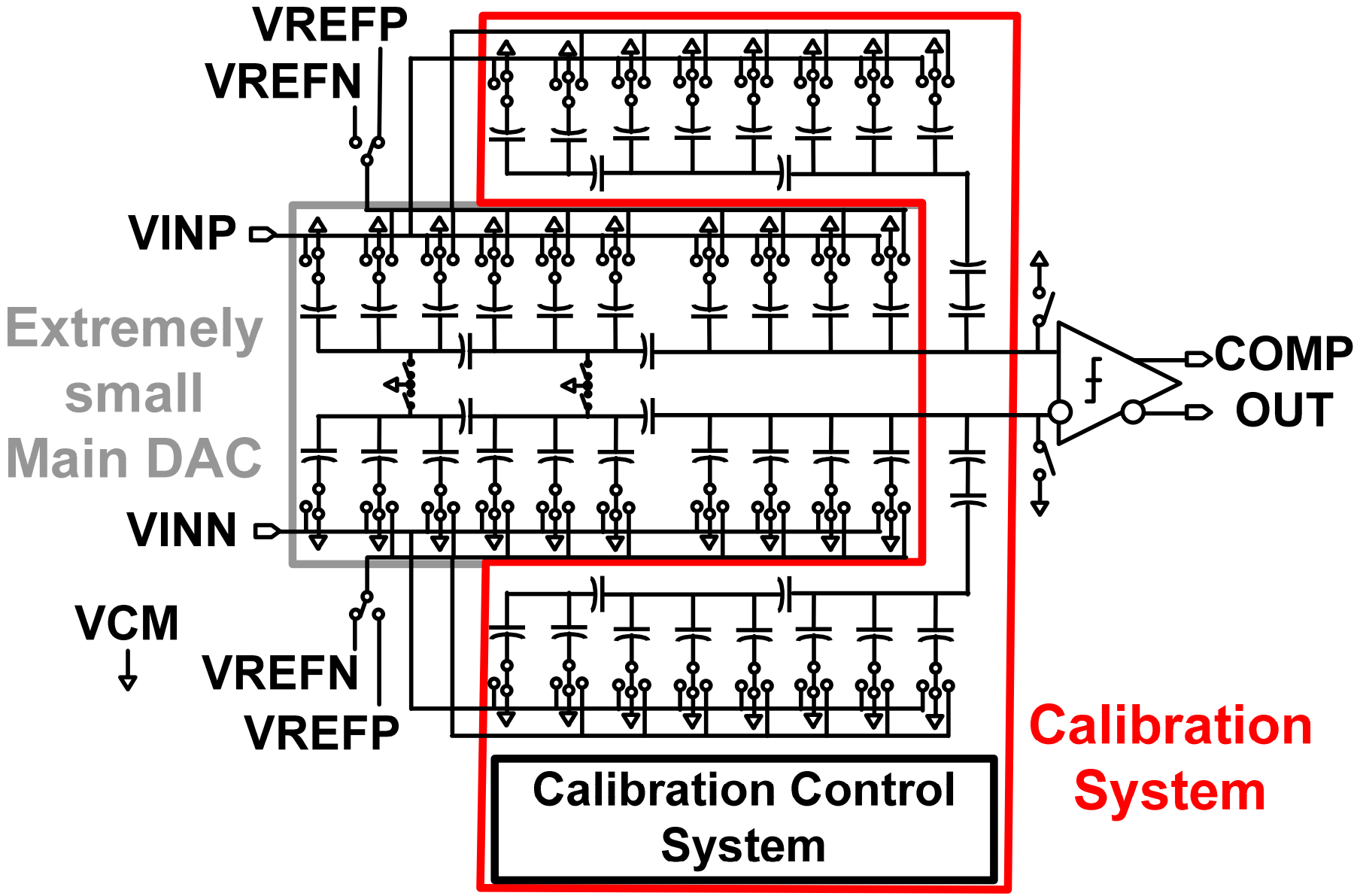
- Small size and good linearity => **k=3** (C, 2C, 4C)

Linearity Error

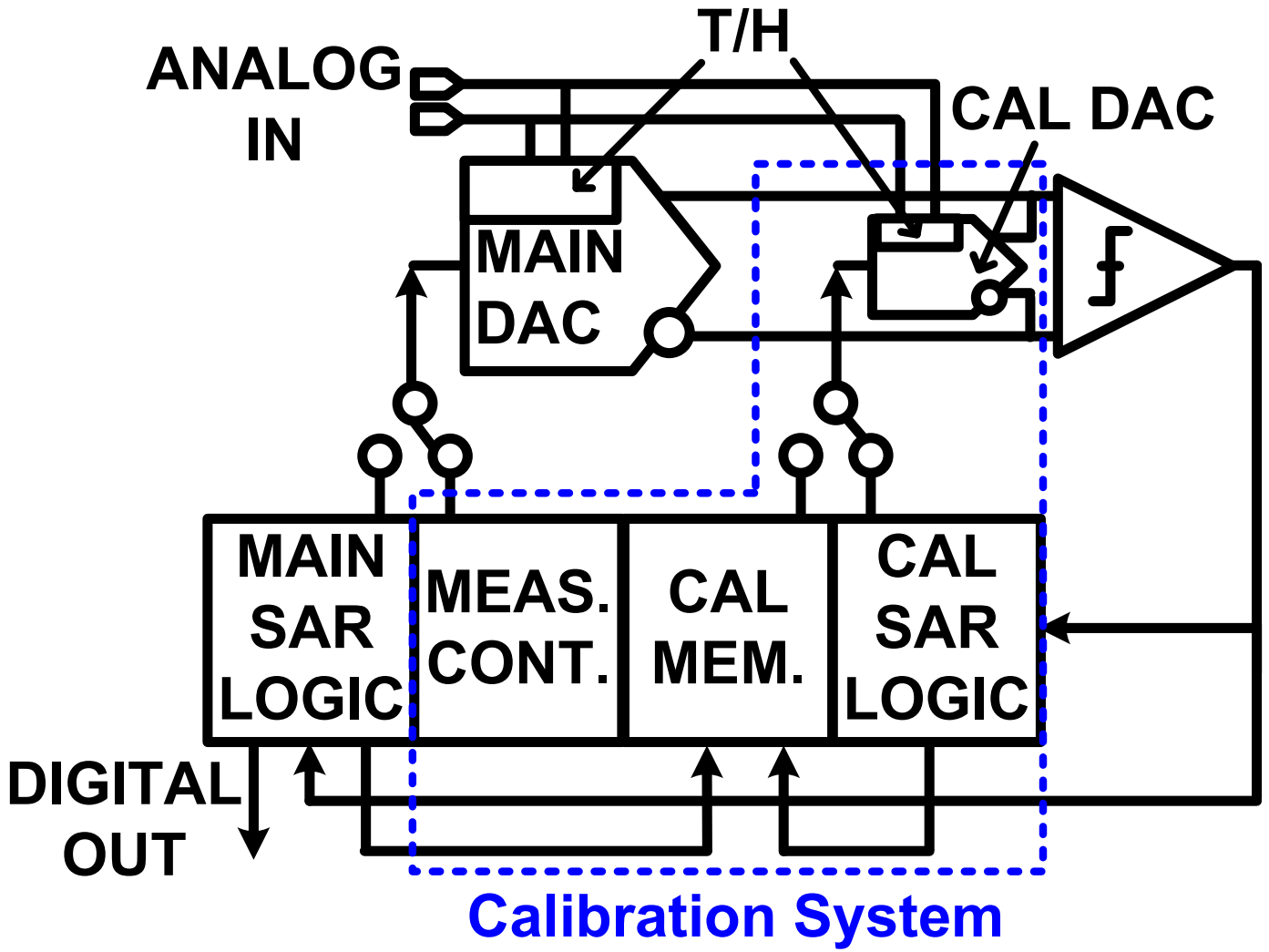


- **Dominant linearity errors are caused by a parasitic bottom capacitor and mismatch errors of parallel capacitors**

ADC Core Circuitry

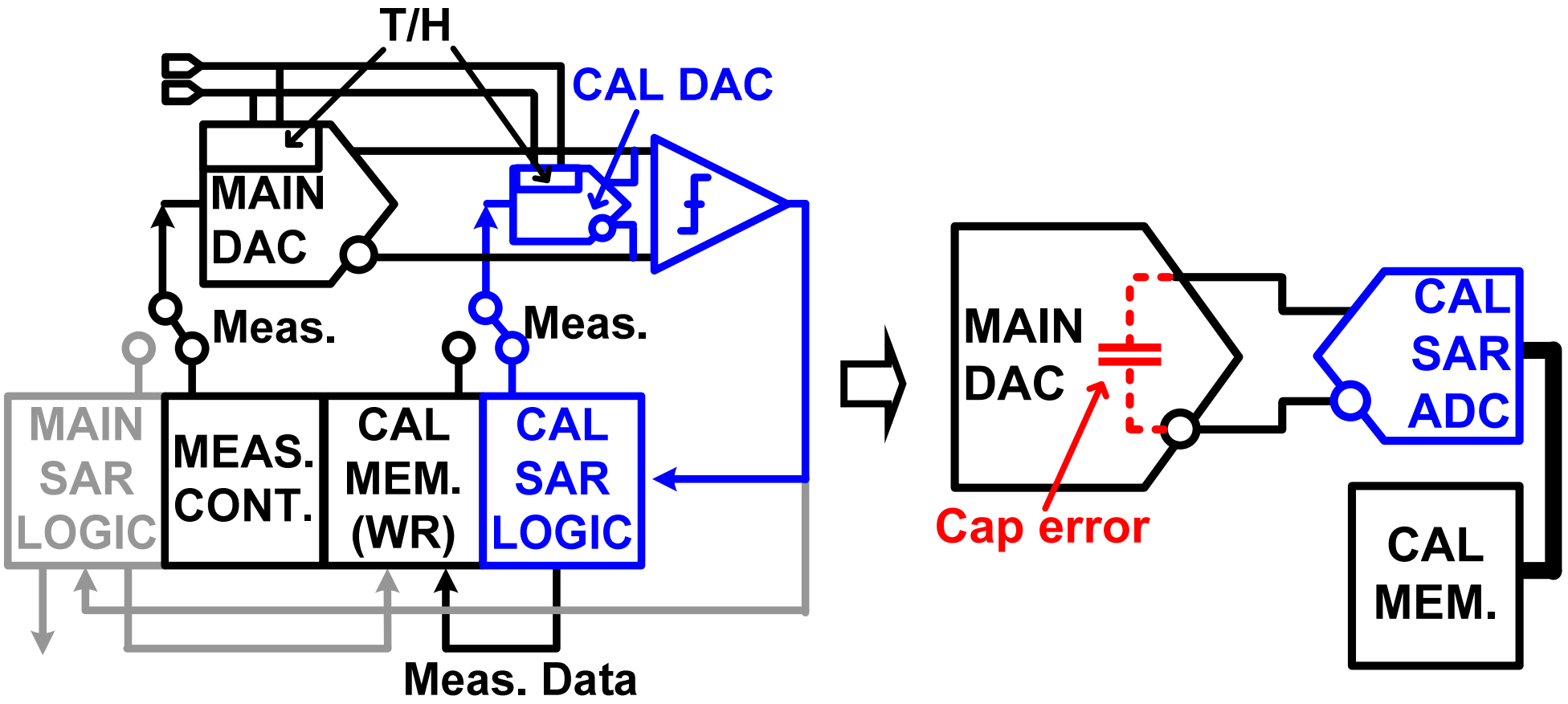


Calibration System



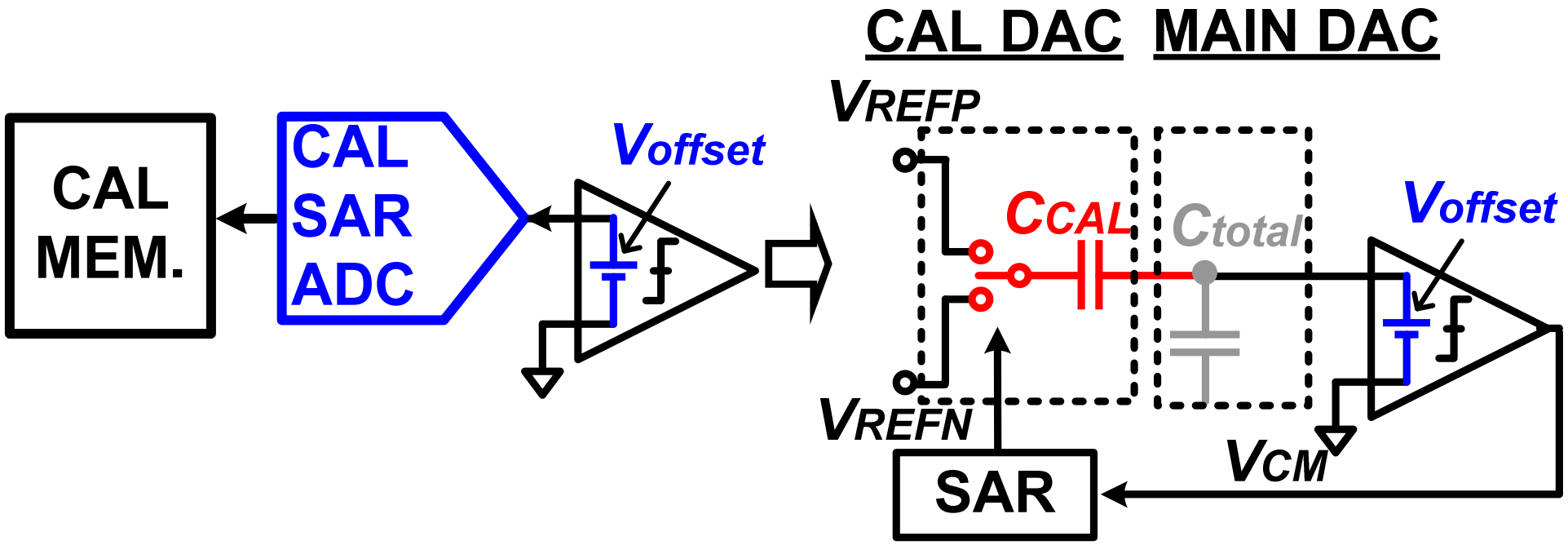
- CAL range: from -16LSB to 16LSB
  with 1/4LSB step

Self-measurement System



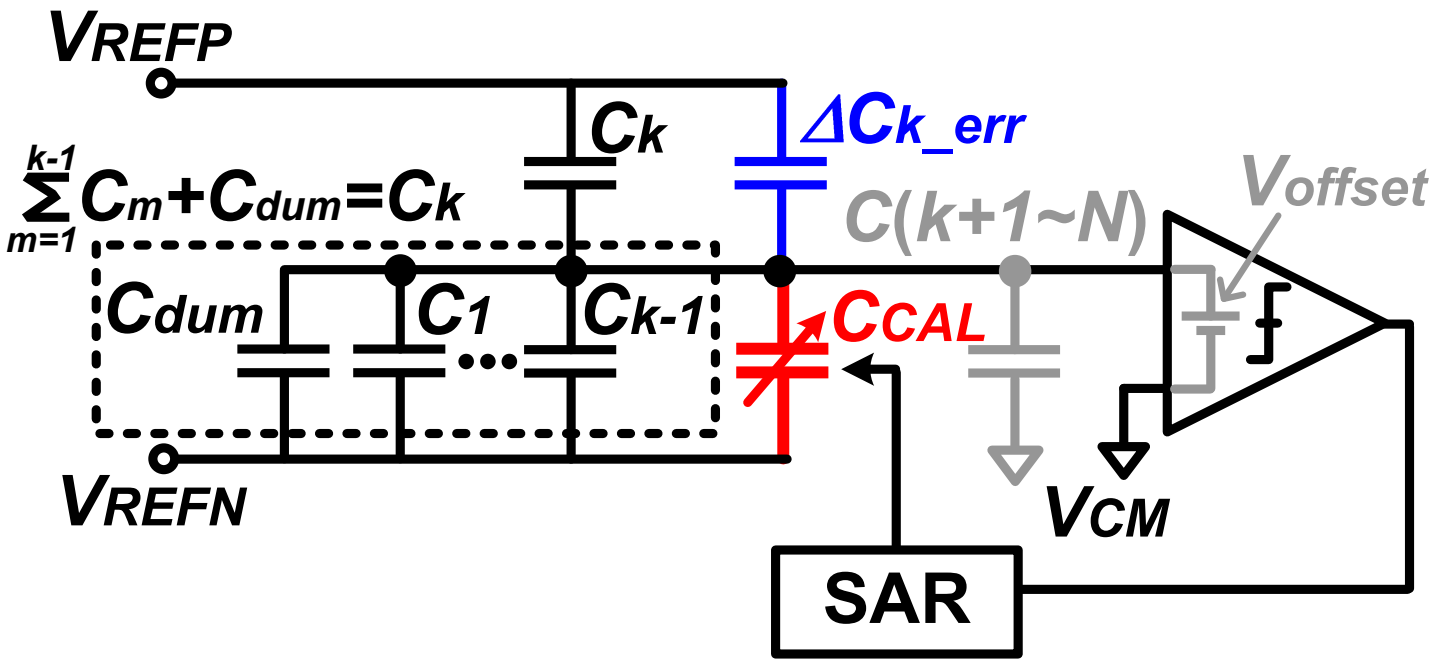
- The CAL DAC and comparator operates as error measurement ADC with a SAR algorithm

Measurement of Offset



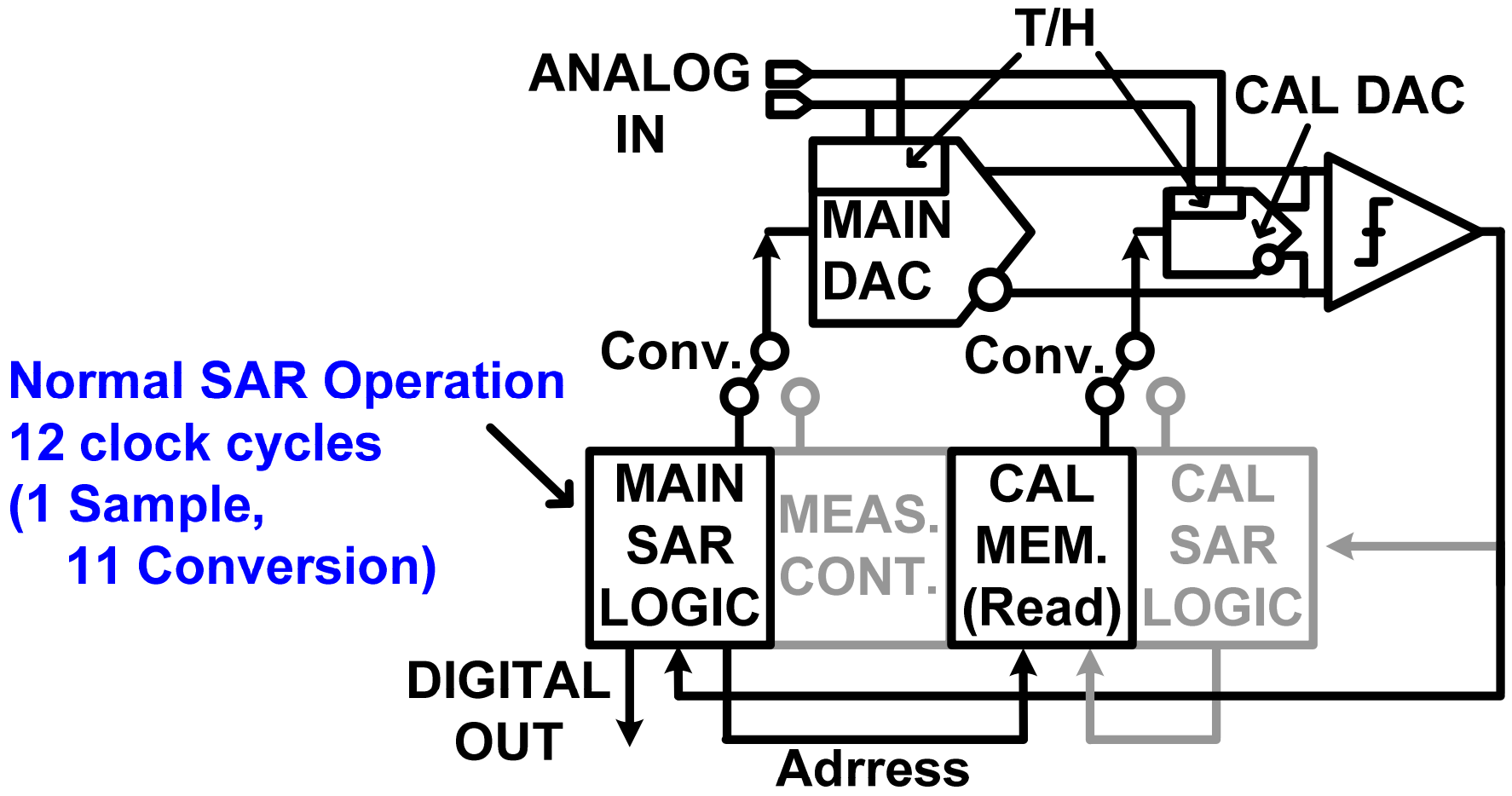
- **Measurement sequence :**
  1. Measurement of the offset
  2. Measurement of the upper 5-bit
- **CAL SAR search for *Voffset***

Measurements of Cap. Errors



- **Measurement sequence :**
  1. **Measurement of the offset**
  2. **Measurement of the upper 5-bit**
- **CAL SAR search for ΔC_{k_err} – $C_{CAL}=0$**

Conversion Sequence



- **Conversion Sequence :**

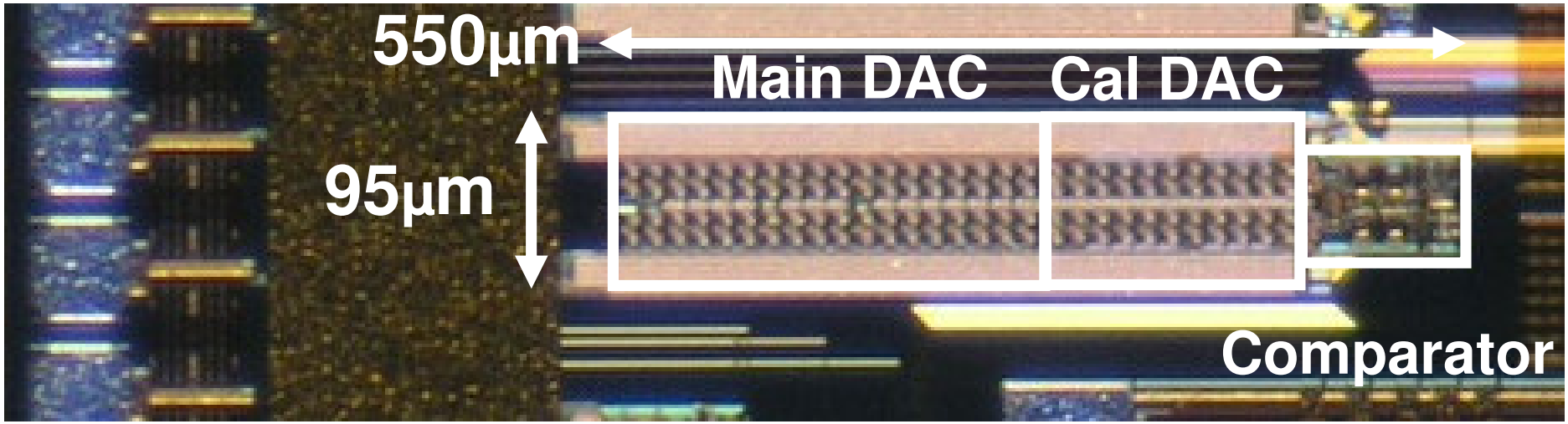
  Main DAC output is calibrated with CAL DAC based on measurement data

Outline

- Background
- ADC core architecture
- Calibration system
- **Measurement results**
- Conclusions

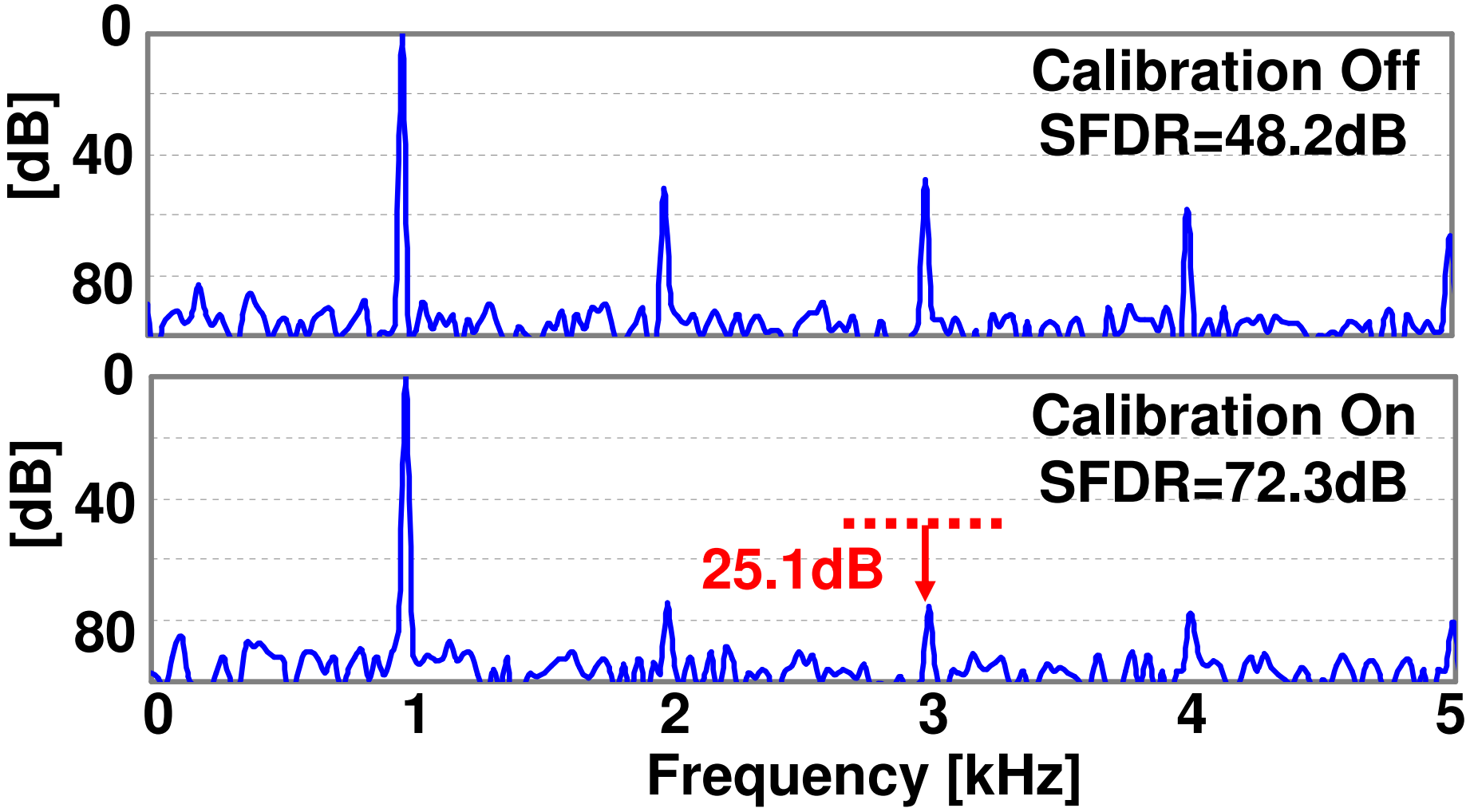
Chip Micrograph

- 0.18µm CMOS, 1-poly, 6-metal Layers, MIM Capacitor
- Control logics are composed of an off chip FPGA



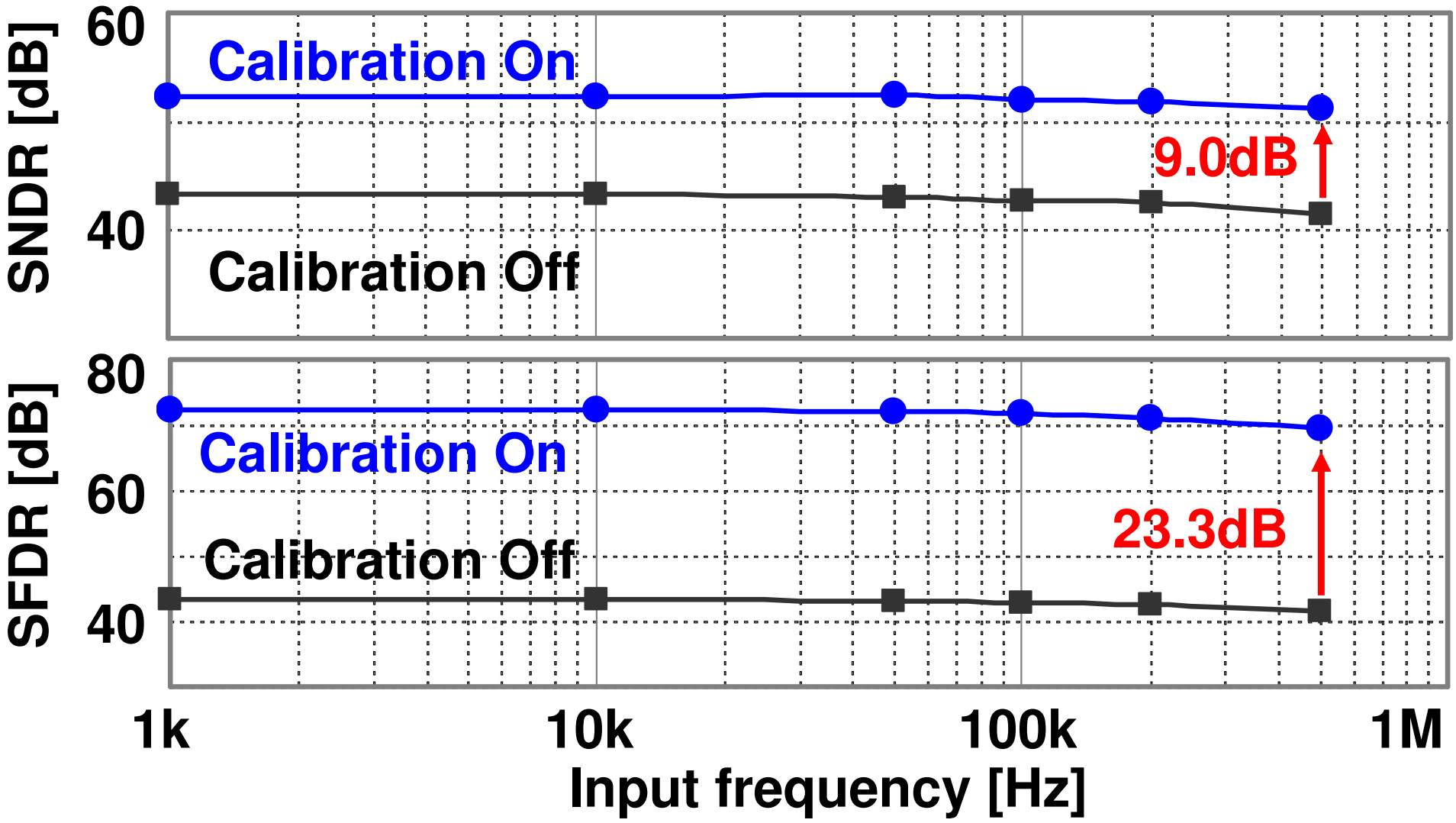
Measured Spectrum

- Fsample 1MS/s, Fin 1kHz, 1.8V Supply



Dynamic Performance

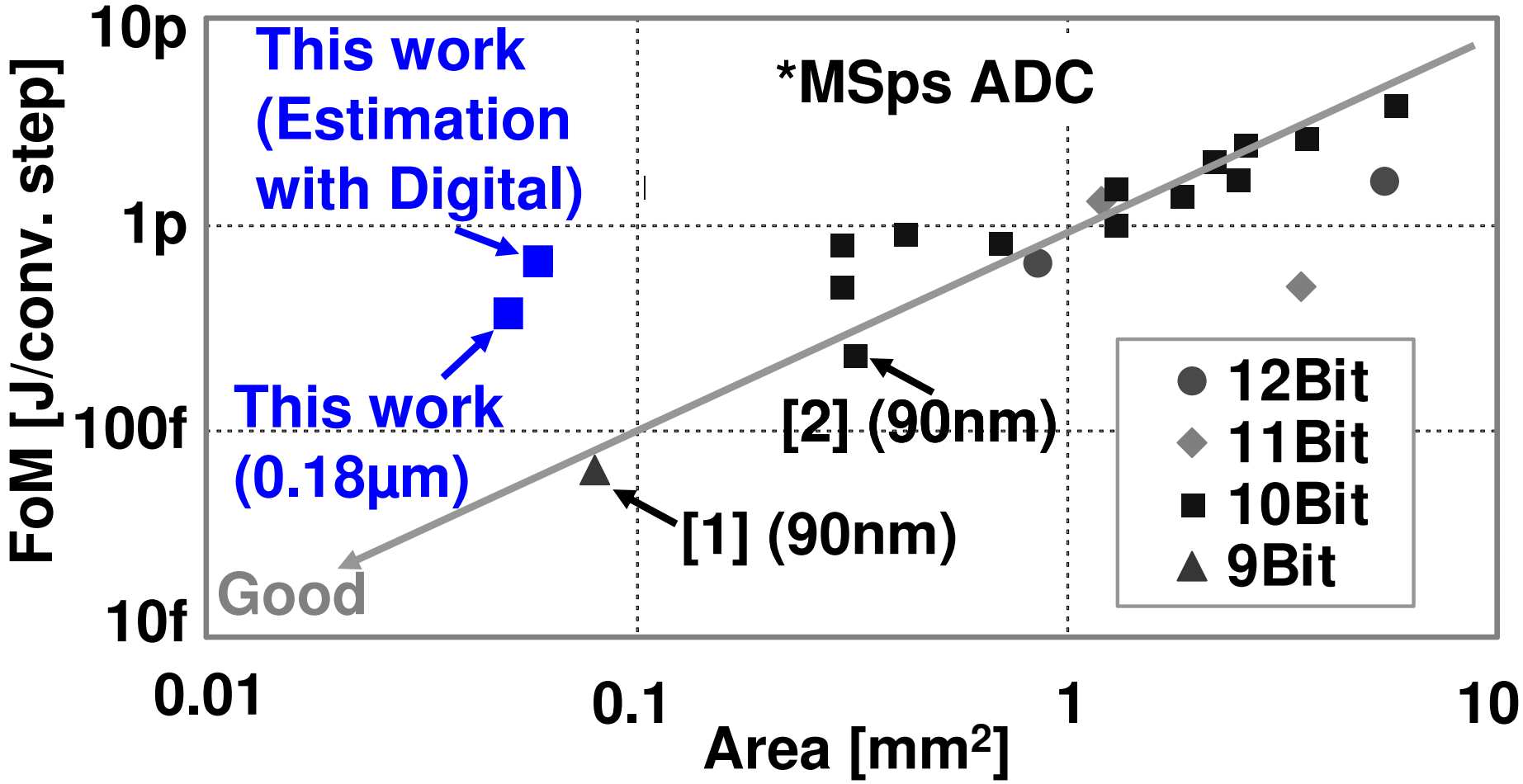
- Fsample 1MS/s, 1.8V Supply



ADC Performance Summary 1

Technology	0.18μm, 1poly, 6metal CMOS
Resolution	10bit
Active Area	95μm x 550μm=0.05mm^2
Sampling Rate	1MSps (12MHz clock)
SNDR@nyquist	51.1dB
SFDR@nyquist	69.8dB
Full Scale Voltage	2.2Vppd
Power Supply	1.8V
Power Consumption	110μW(Analog)

ADC Performance Summary 2



[1] J. Craninckx, et. al., "A 65fJ/Conversion-Step, 0-to-50MS/s 0-to-0.7mW 9bit Charge-Sharing SAR ADC in 90nm Digital CMOS", *ISSCC 2007*

[2] Y. Jeon, et. al., "A 4.7mW 0.32mm2 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS", *ISSCC 2007*

Conclusions

- **A 0.05-mm^2 110-µW 10-b SAR ADC core:**

- 0.18µm CMOS

- Minimizing total capacitance based on SNR

- Minimizing the area of lower bit DAC with series connection of binary DAC

- Main DAC with low accuracy small capacitors calibrated by CAL DAC, SNDR:9.0dB, SFDR:23.3dB improvement