Fine and Wide Frequency Tuning Digital Controlled Oscillators Utilizing Capacitance Position Sensitivity in Distributed Resonators

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Outline

- **Background**
- **Proposed Circuit**
- **Design Method**
- **Prototype DCO and Measurements**
- **Conclusion**

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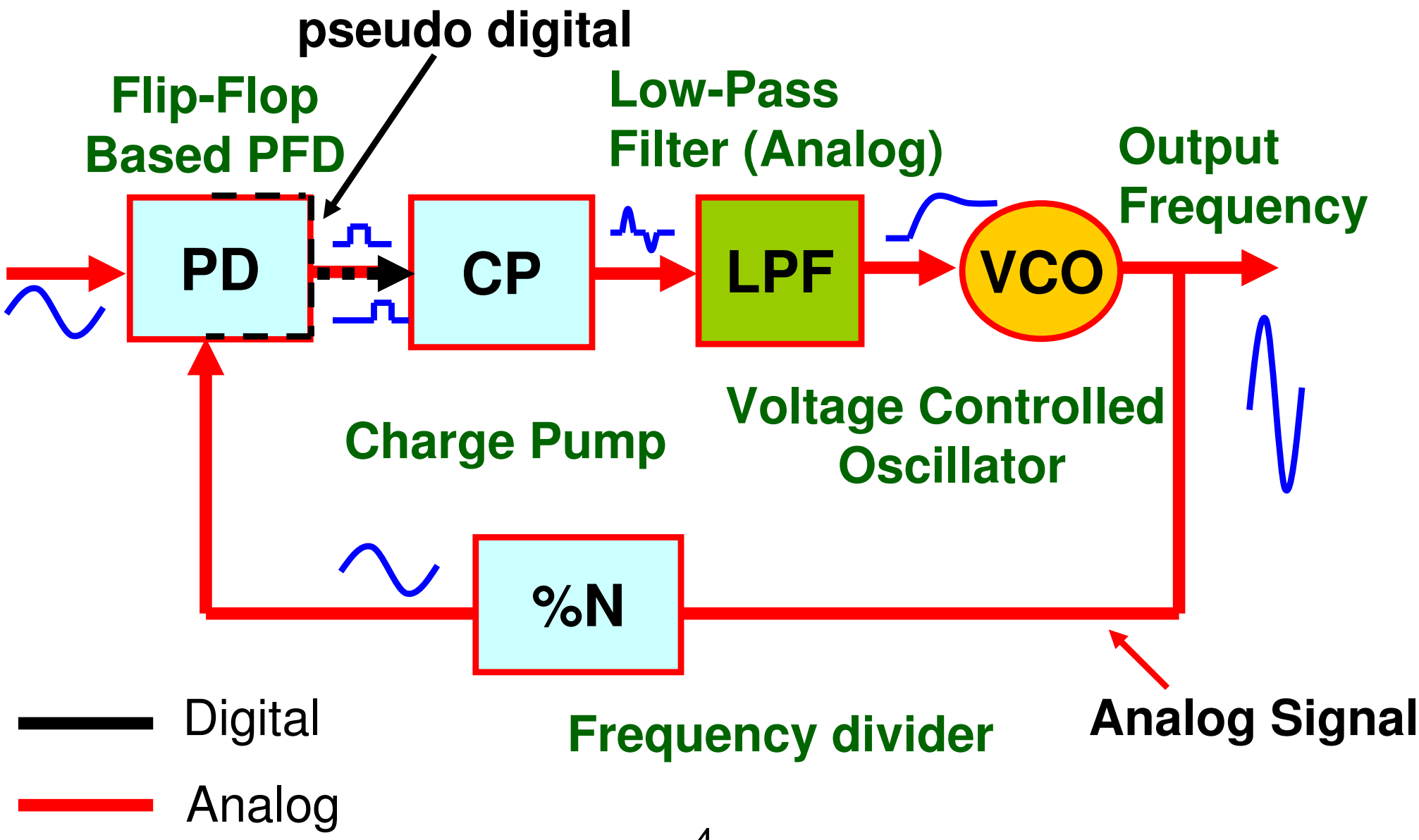
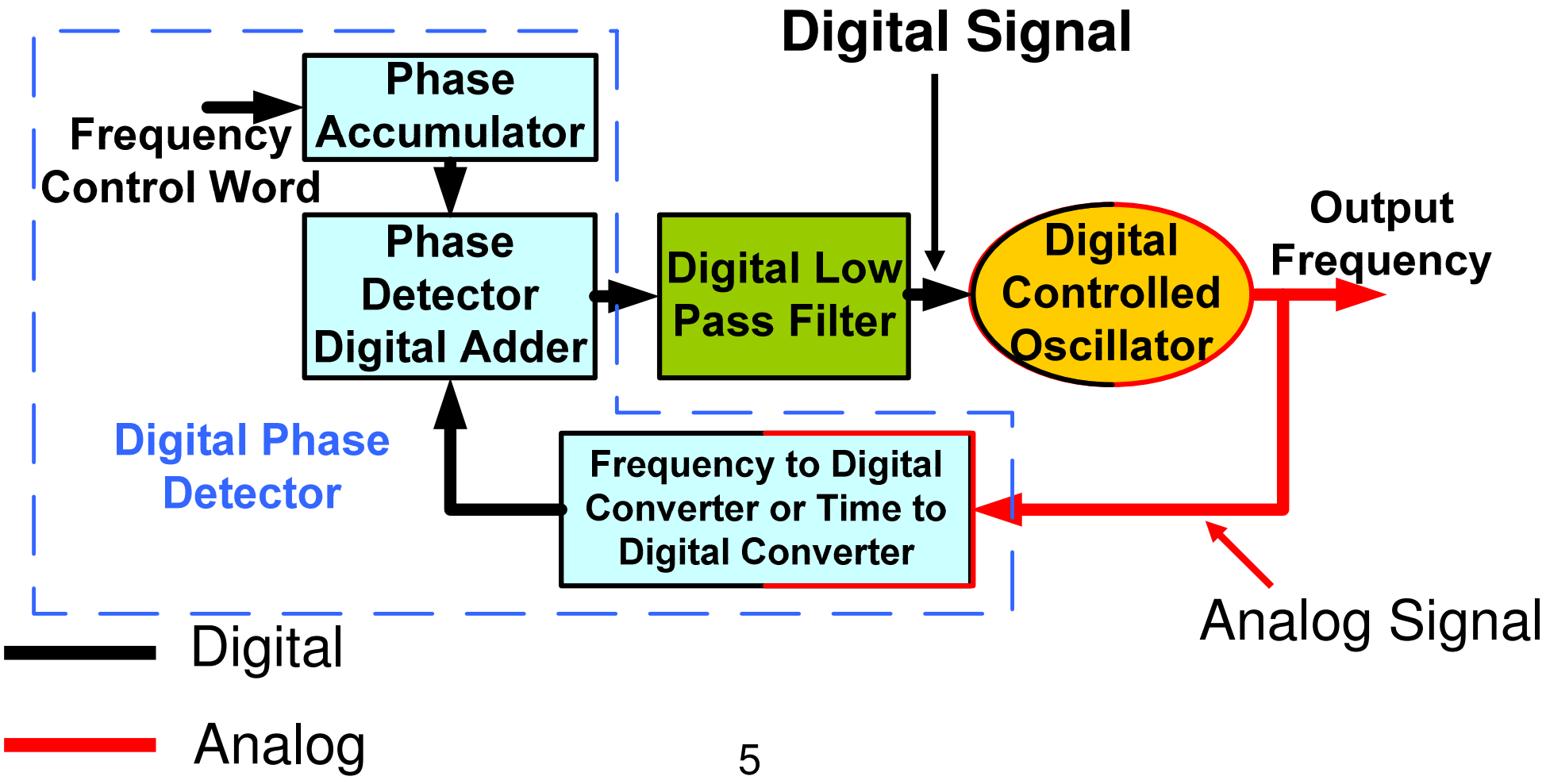
Phase Locked Loop



ADPLL Overview

Recently GHz freq. all-digital phase locked loop (ADPLL) shown practical



Advantages of ADPLL

- **Robust to variation**
  - **process, voltage, temperature (PVT)**
- **Technology Scaling**
  - **better with low voltage, sharper signal edges**
- **DSP Enhancement**
  - **Dynamic parameter control, calibration**
- **Promising multi-band**
  - **inherent adaptability**

Challenges of ADPLL

- **Critical Interface Elements**
  - **TDC limits loop feedback resolution**
  - **DCO limits synthesized frequency resolution**
- **Complexity**
  - **compared to traditional PLL, $\Delta\Sigma$, DEM, overhead calculation**
- **Excess Power Consumption**
  - **from $\Delta\Sigma$, DEM, overhead calculation**

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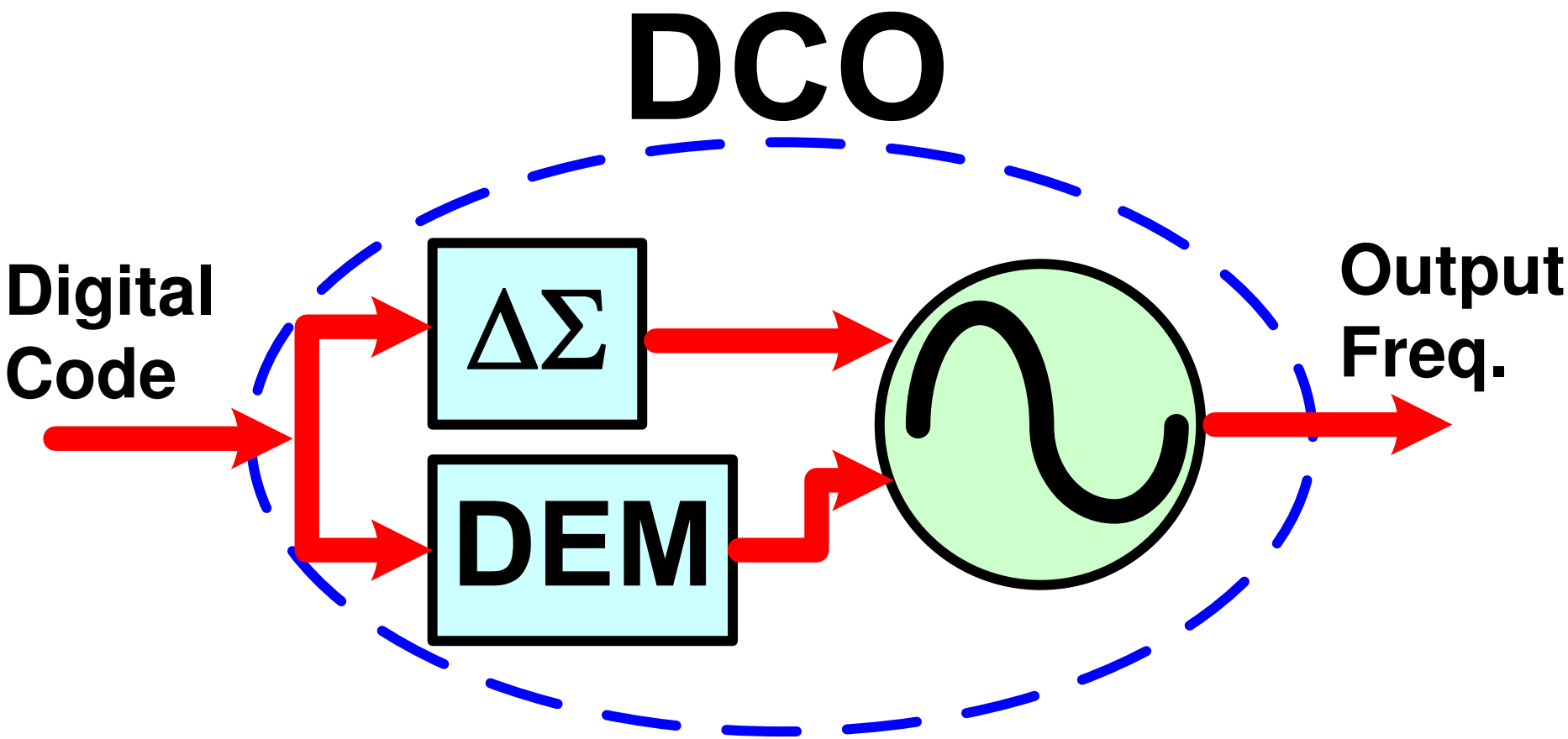
Inside the DCO



DCO Challenges 1

DCO freq. step $\propto$ ADPLL's freq. resolution

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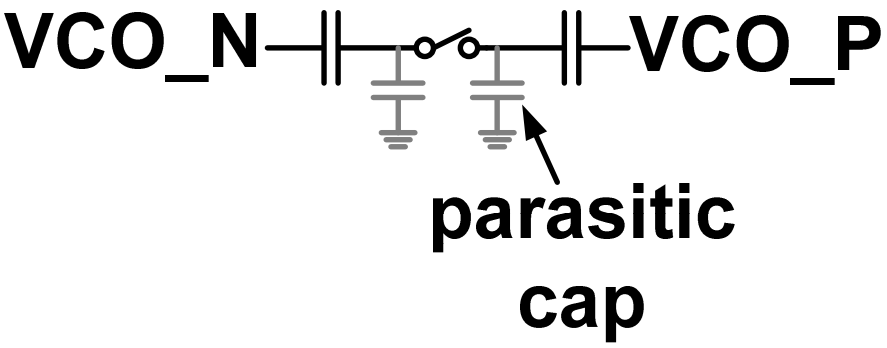
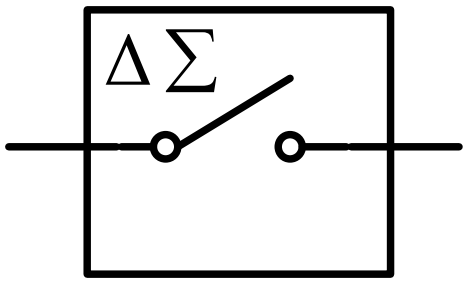
DCO freq. step ∝ ADPLL's freq. resolution

1. **Small cap. (50aF) used for fine freq. step DCO**
   [1] Staszewski,2005, JSSC



2. **High freq. dithering increase freq. resolution**



DCO Challenges 1

DCO freq. step ∝ ADPLL's freq. resolution

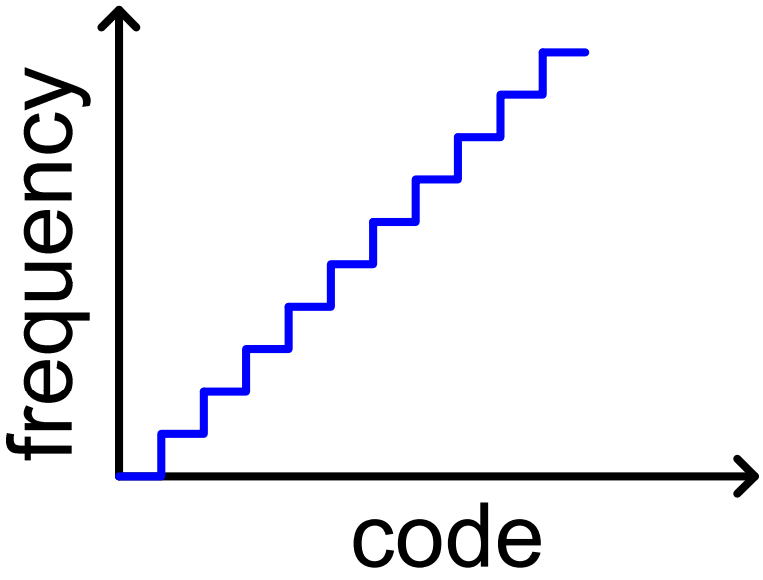
1. **Small cap. (50aF) used for fine freq. step DCO**
   [1] Staszewski,2005, JSSC

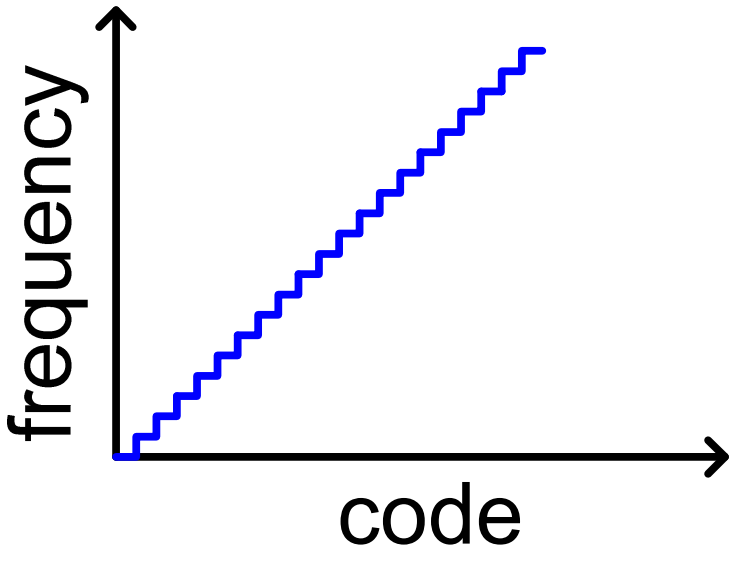
Difficult to control the small cap., mis-match, parasitic are problematic

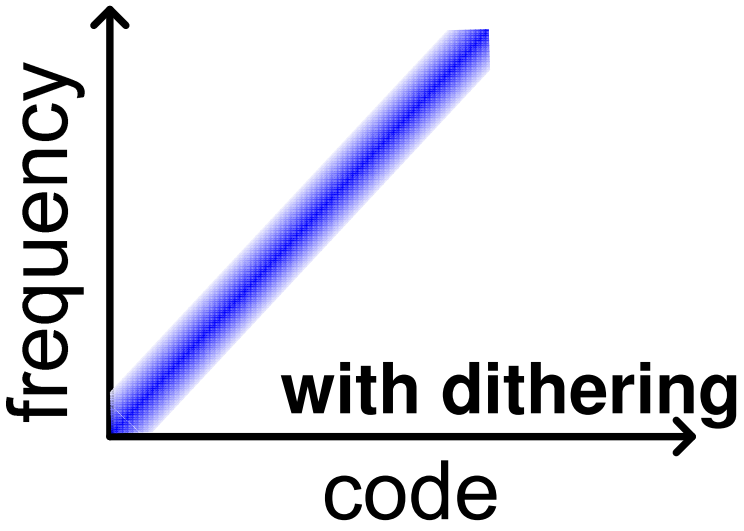
2. **High freq. dithering increase freq. resolution**

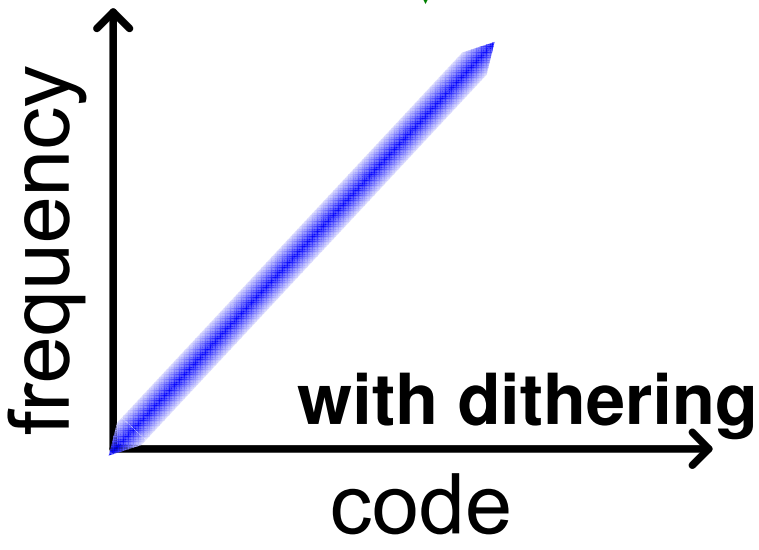
High Freq. dithering Increase Power consumption, add noise into system

Dithering Noise

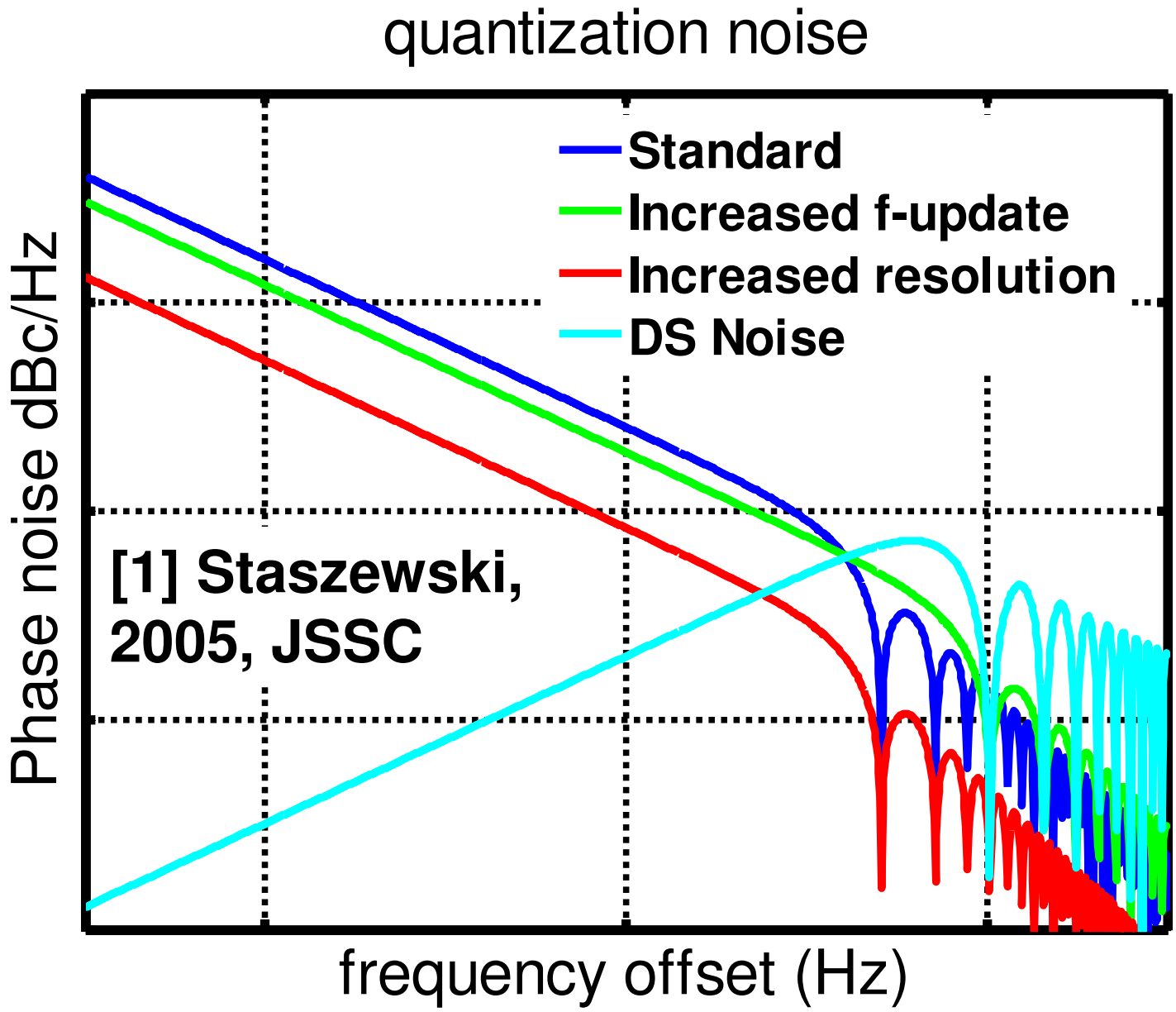






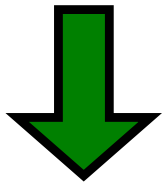


Phase Noise Due to Quantization



DCO Challenges 2

Challenges faced in DCO now (2GHz)



Problem will increase in future for higher freq. (5GHz and beyond) DCO when

1. **Parasitic cap. becomes more significant**
2. **Mismatch leads to greater freq. deviation**
3. **Dithering methods must be run at higher freq.**

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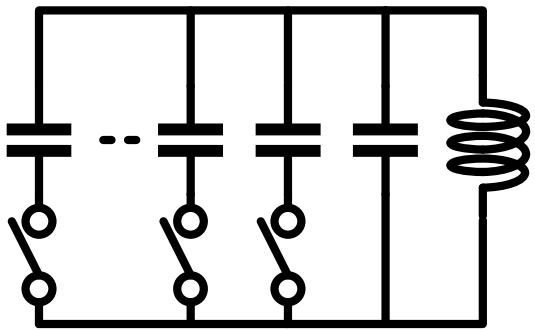
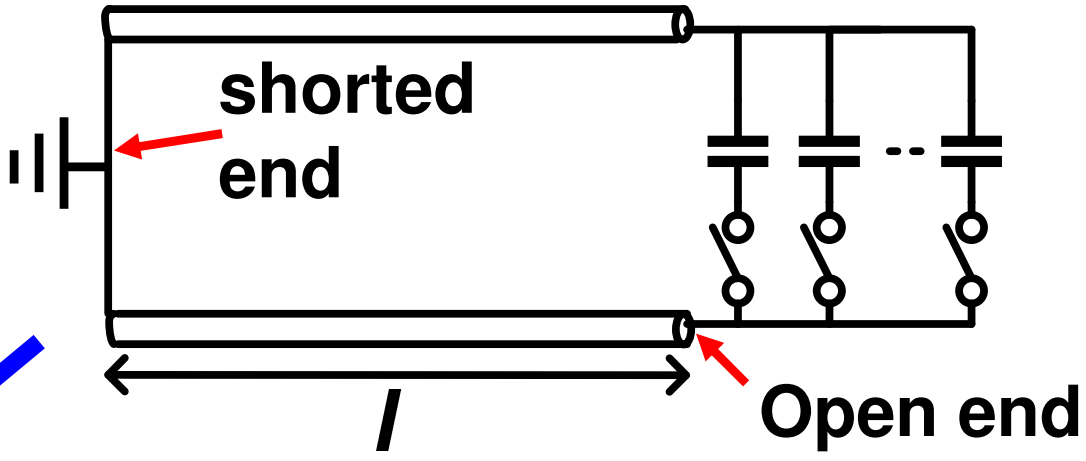
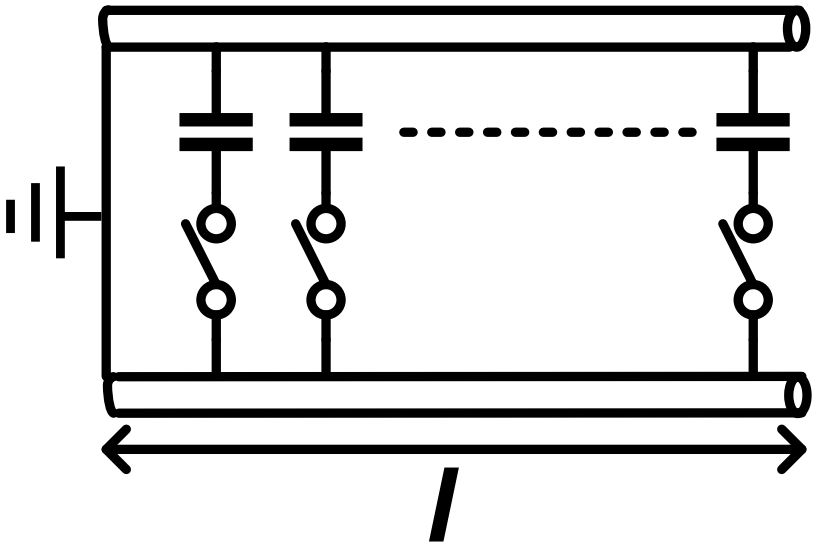
Proposed Circuit



Present DCO resonators

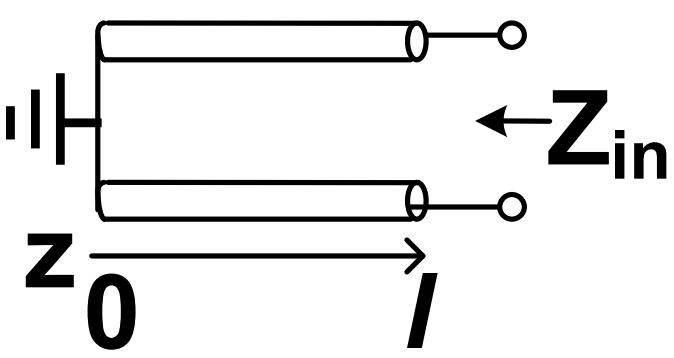


Distributed DCO resonator using present tuning techniques

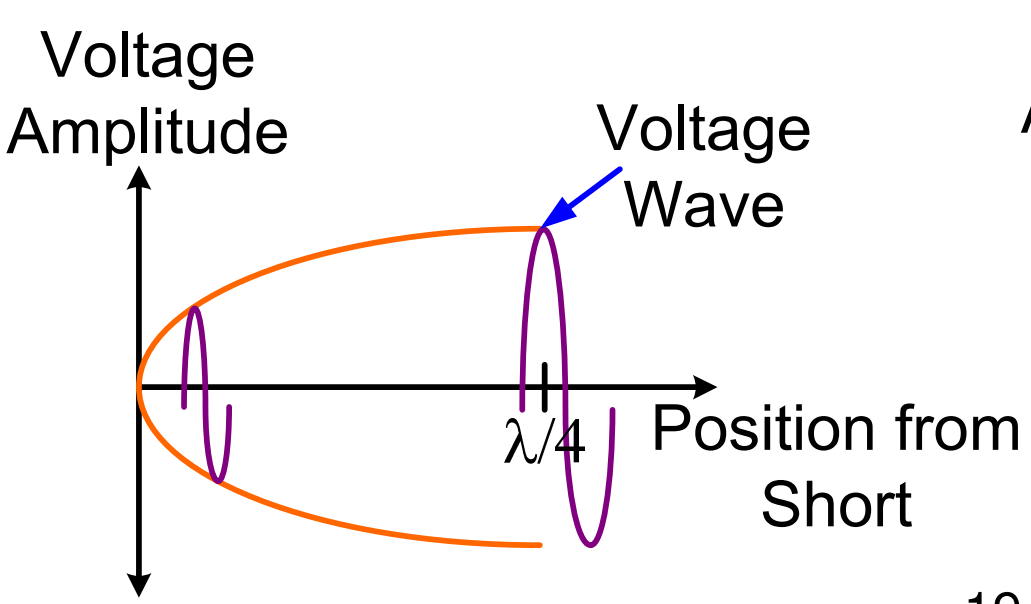


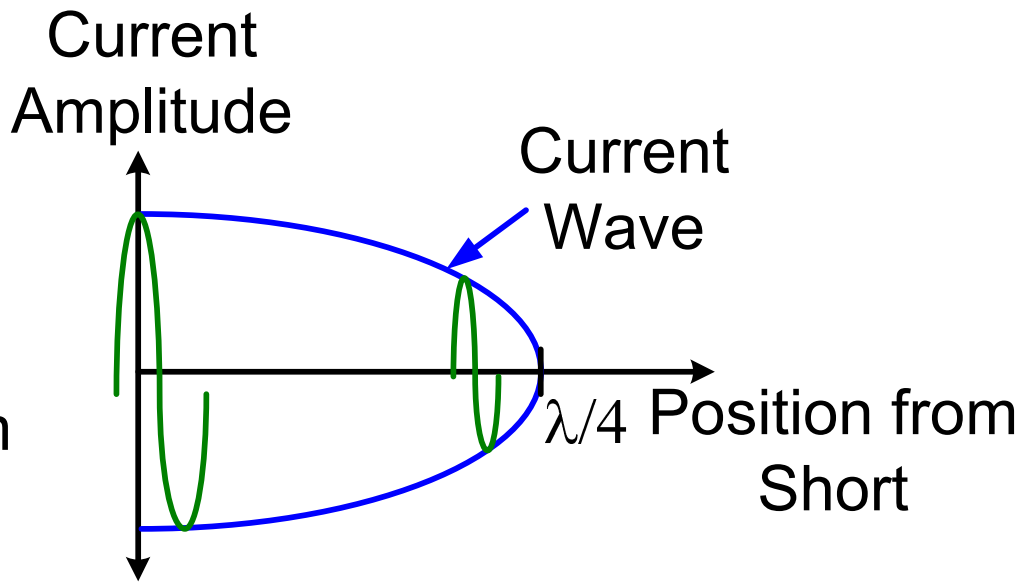
Proposed DCO resonator

Distributed Resonators

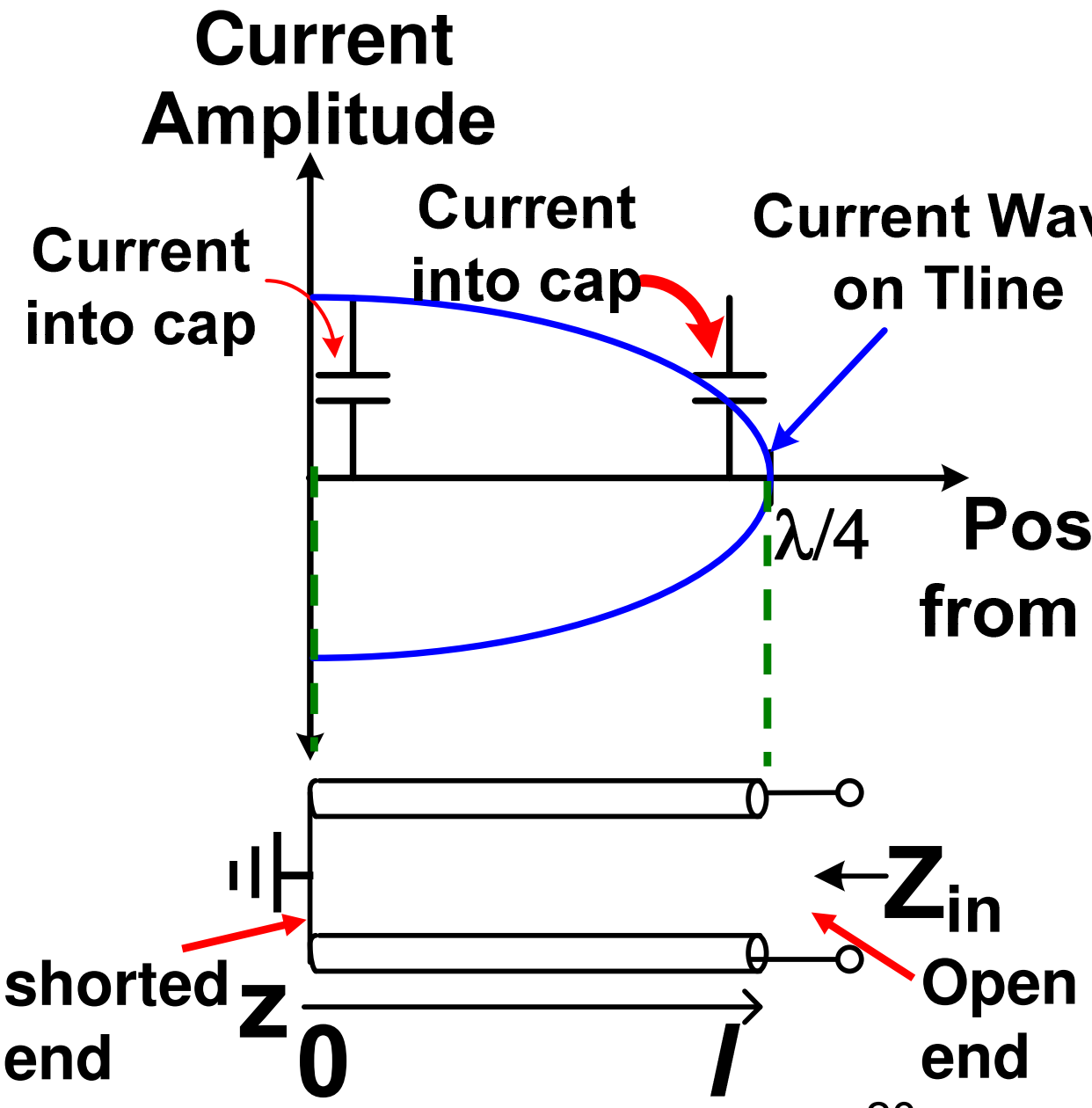


Current and voltage varies with position, should the cap.'s freq. contribution vary with position too?





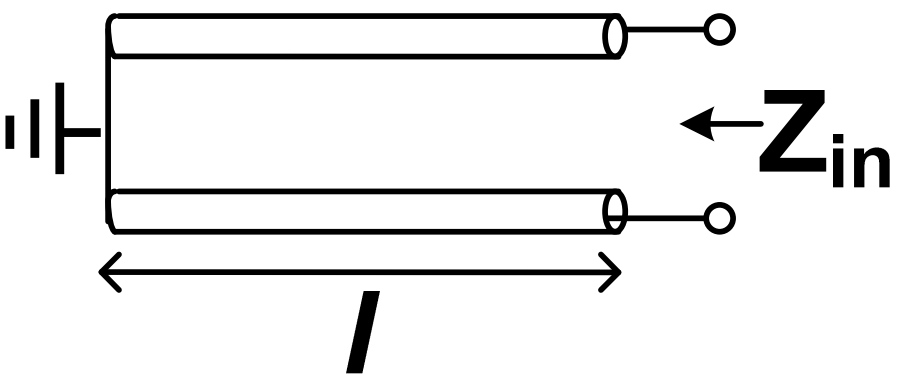
Current Into Cap. VS Position

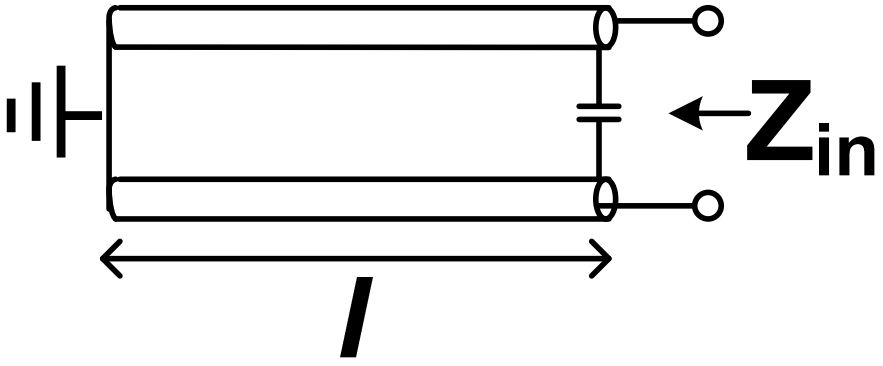


Effect of cap. decreases as it nears short end

How to find the resonance freq. of the T-line with cap in middle?

Resonance Frequency





resonance freq. is

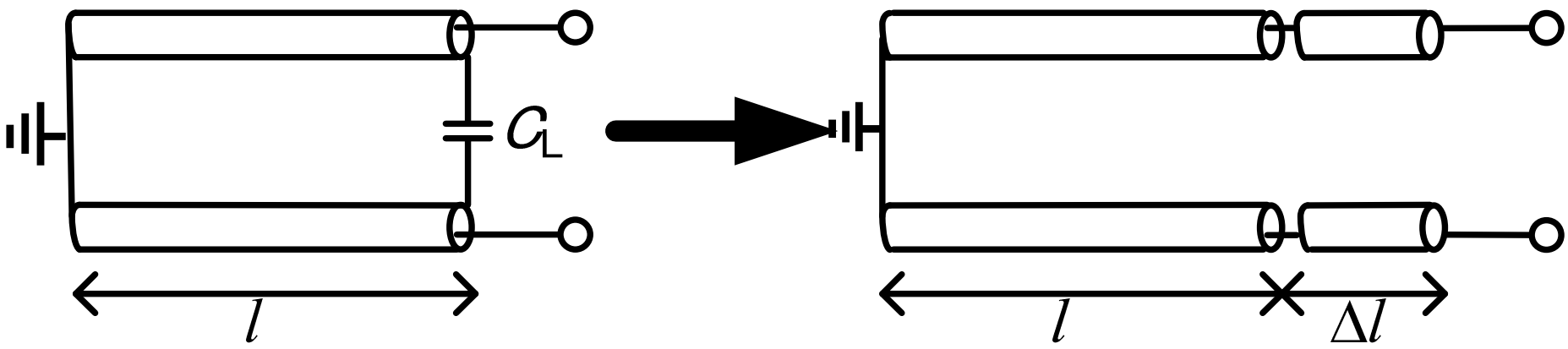
$$f_0 = \frac{v_p}{4 \cdot l} = \frac{1}{4 \cdot l \cdot \sqrt{\mu_0 \cdot \varepsilon_0 \cdot \varepsilon_{reff}}}$$

resonance freq. is

$$f_0 \approx \frac{1}{4 \cdot (l \cdot \sqrt{\mu_0 \cdot \varepsilon_0 \cdot \varepsilon_{reff}} + C_L \cdot Z_0)}$$

Extra factor proportional to load and characteristic impedance of T-line

Capacitance Equivalent Length

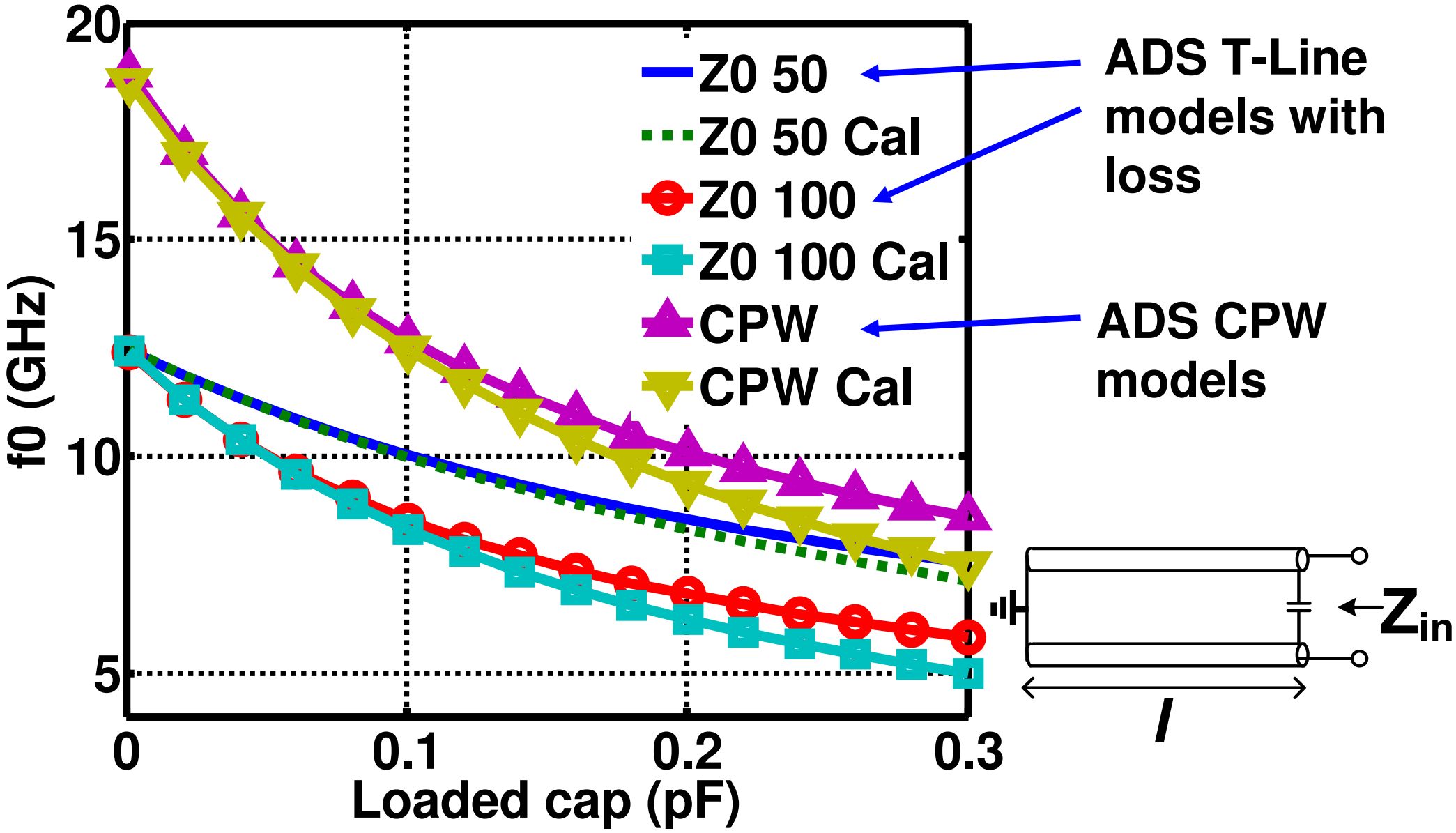


$$f_0 \approx \frac{1}{4 \cdot (l \cdot \sqrt{\mu_0 \cdot \varepsilon_0 \cdot \varepsilon_{reff}} + C_L \cdot Z_0)}$$

$$f_0 \approx \frac{1}{4 \cdot ((l + C_L / C') \cdot \sqrt{\mu_0 \cdot \varepsilon_0 \cdot \varepsilon_{reff}})}$$

extended length
$\Delta l = C_L / C'$
C' = T-line cap. per unit length

Calculated and Simulated Values



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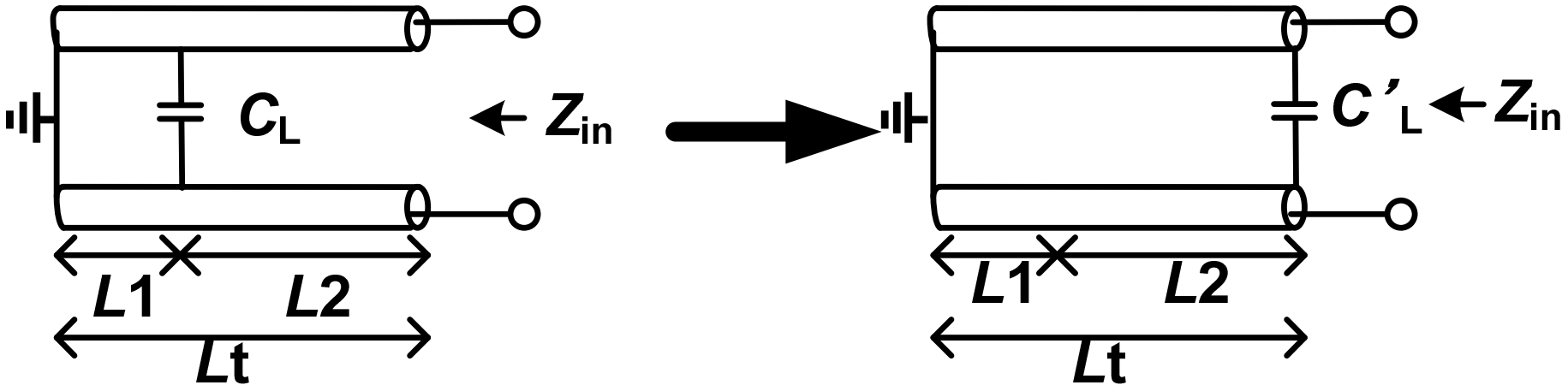
Equivalent Capacitance



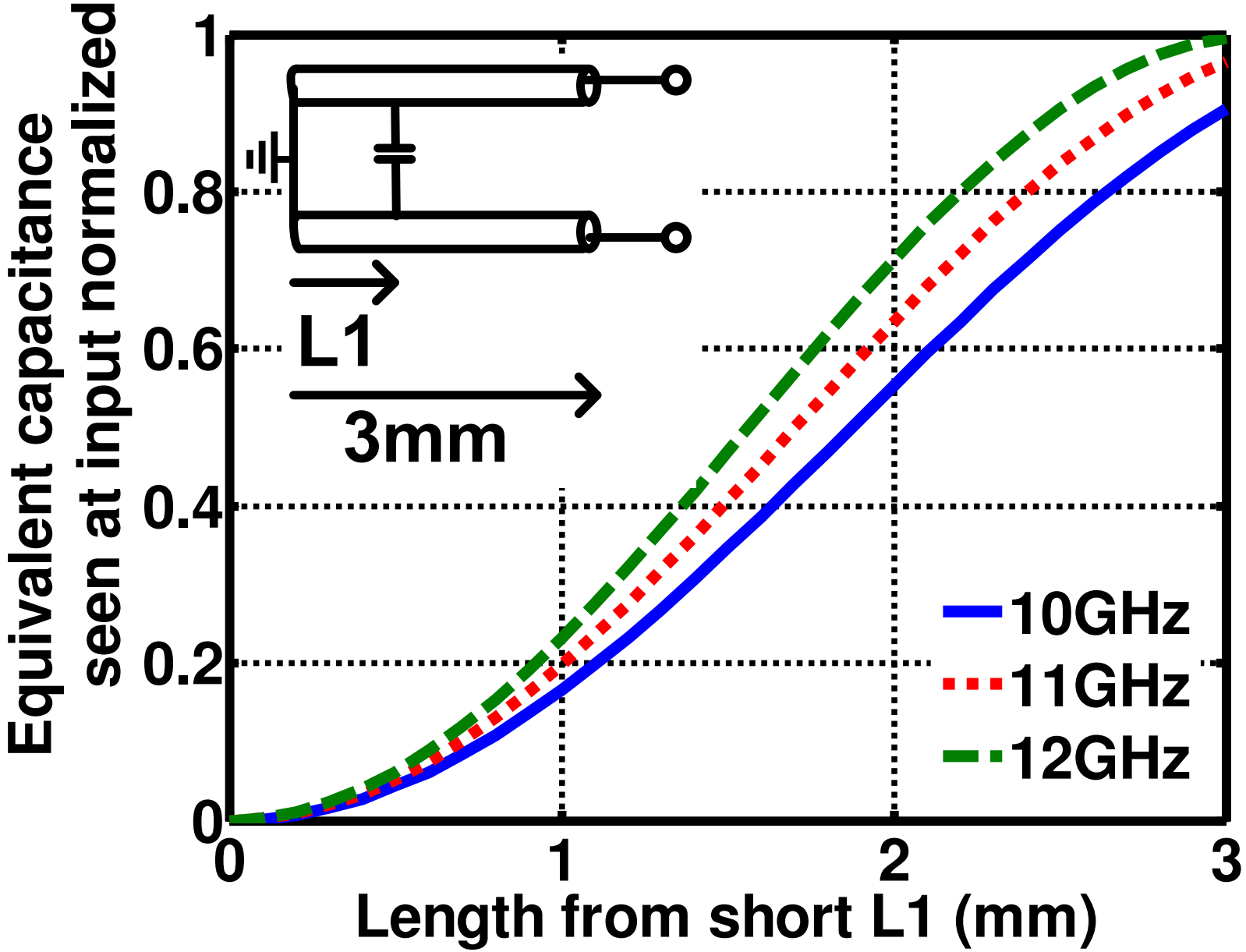
$$C_L' = \frac{C_L}{2} + \left(\frac{C_L}{2}\right) \cdot \sin\left(\frac{\omega}{v_p} \cdot (2 \cdot L1)\right) \cdot \cot\left(\frac{\omega}{v_p} \cdot Lt\right) - \left(\frac{C_L}{2}\right) \cdot \cos\left(\frac{\omega}{v_p} \cdot (2 \cdot L_1)\right)$$

For L=Lt/2 at resonance

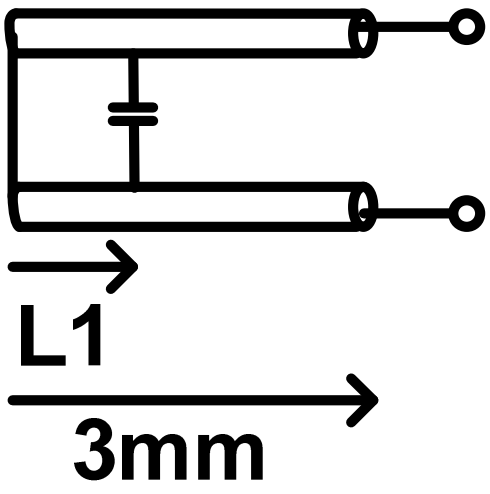
$$C_L' = \frac{C_L}{2}$$

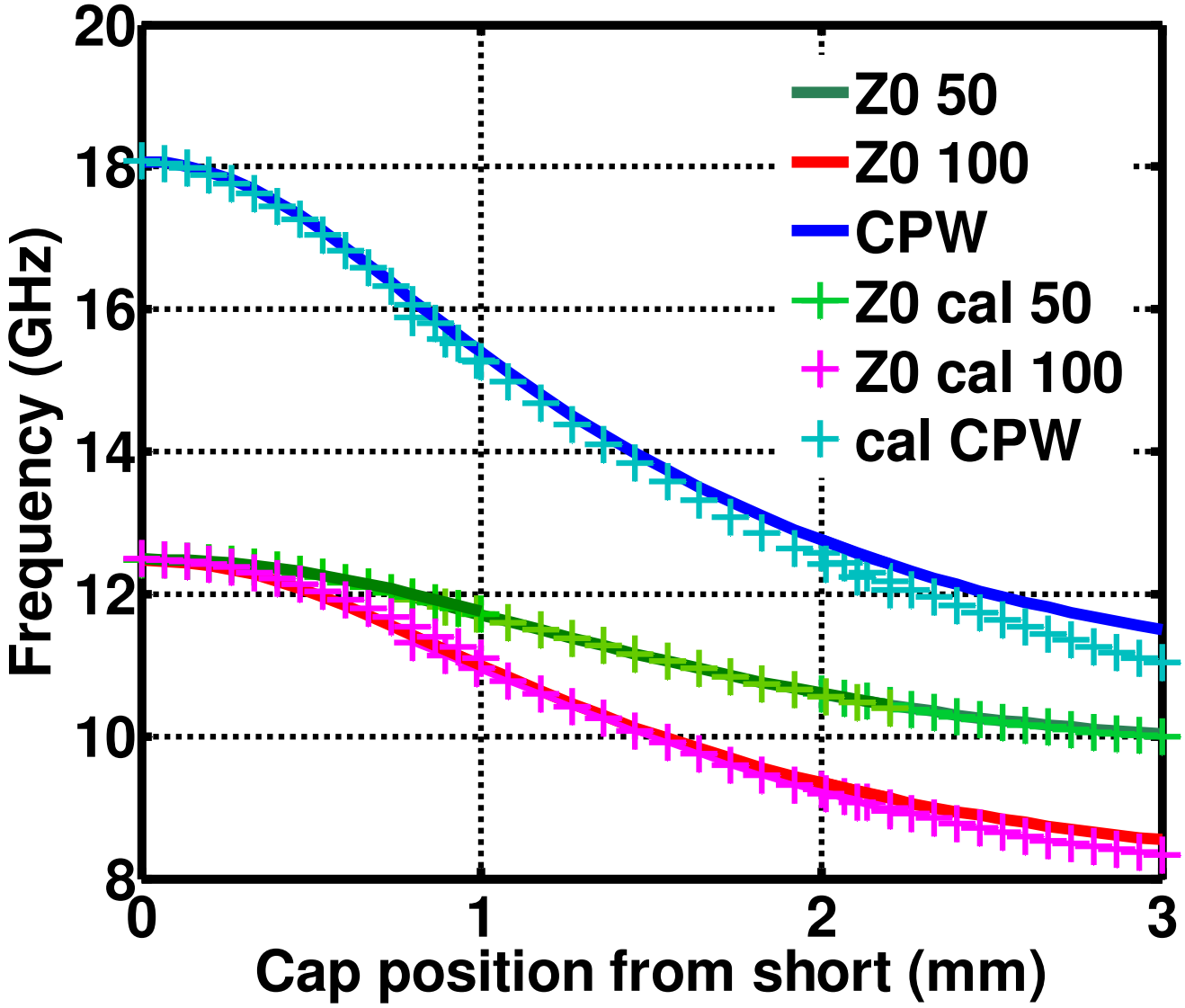
C_L = loading cap
C_L' = equivalent loading cap

Equivalent Capacitance Plot



Simulation VS Calculation





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Design Method

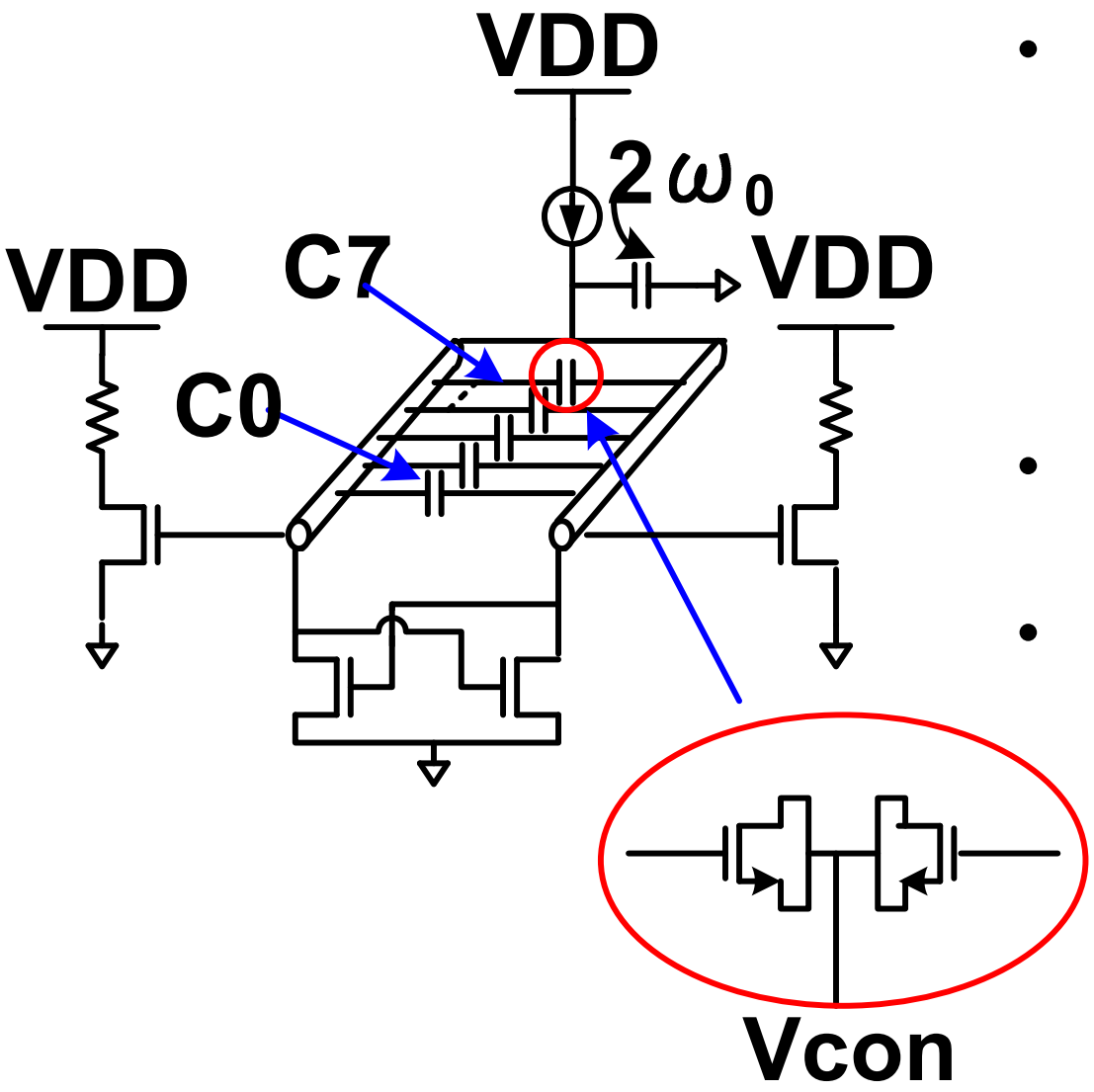
1. **Characterize T-line of arbitrary size**
2. **Estimate needed T-line size and input cap. size for a freq. step using**

$$f_0 \approx \frac{1}{4 \cdot (l \cdot \sqrt{\mu_0 \cdot \varepsilon_0 \cdot \varepsilon_{reff}} + C_L \cdot Z_0)} \qquad (1)$$

3. **Estimate actual cap. size and cap. position using the equiv. cap. equation and (1)**

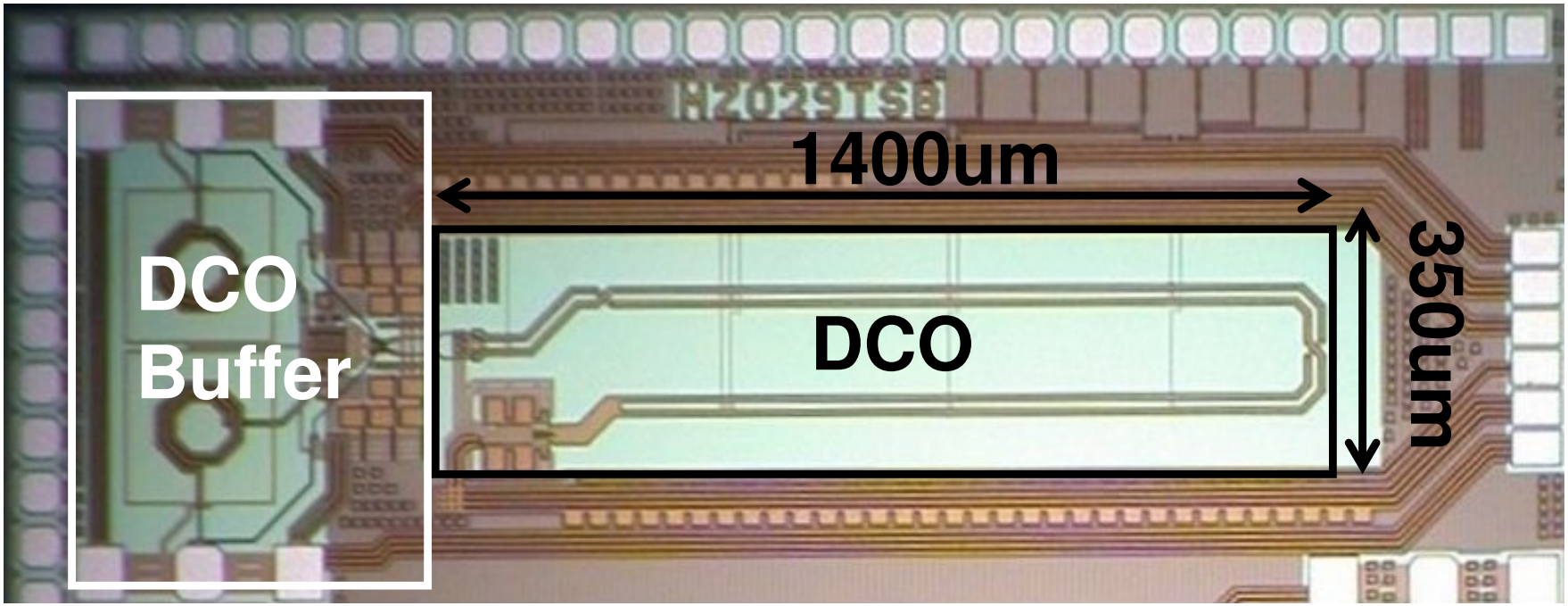
4. **Create actual T-line with estimated tap positions for cap.**
5. **Simulate whole system, and iterate until correct**

Prototype DCO

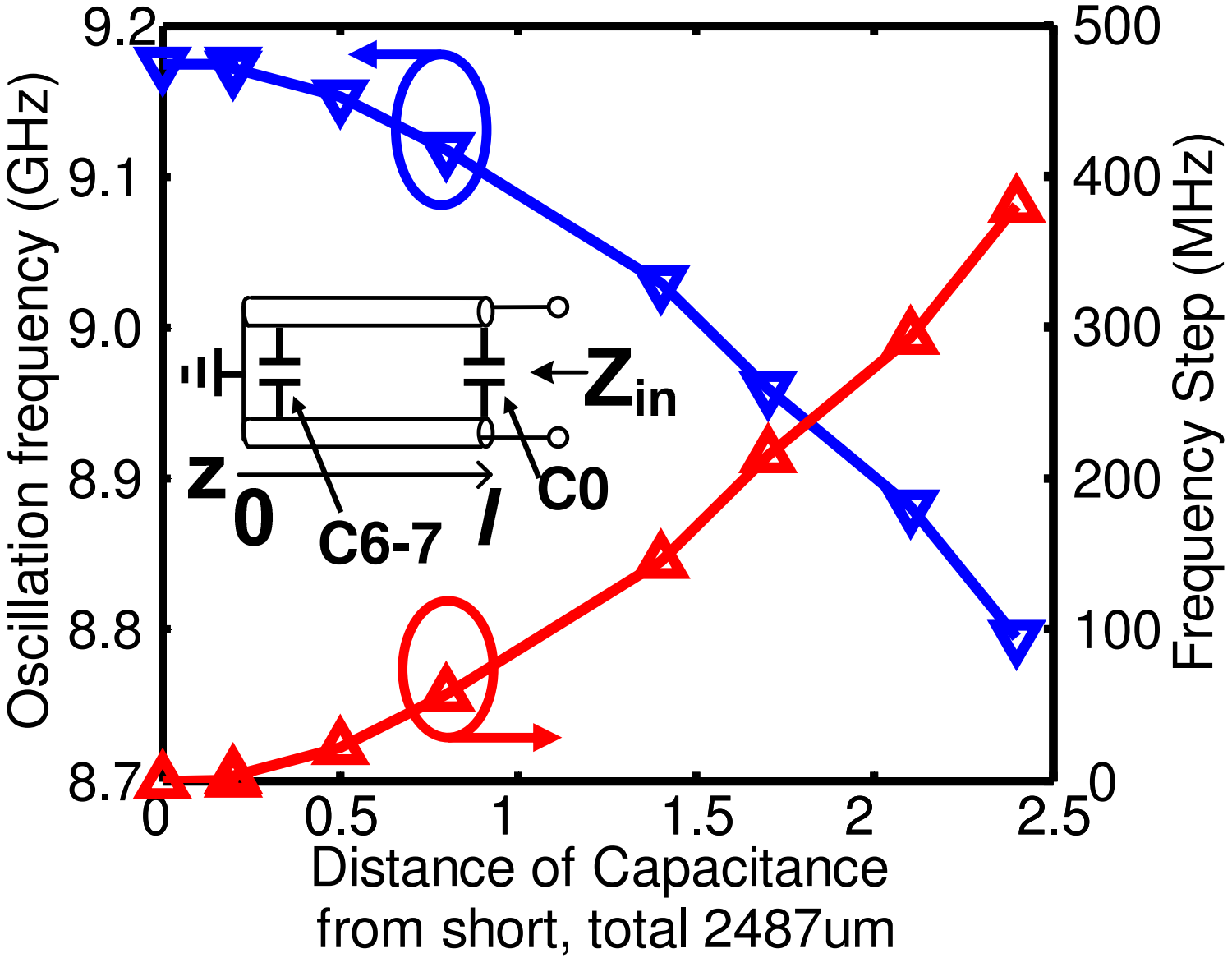


- 8 steps total
  Steps 1-7 mid size MOS cap (C0-C6)
  Step 8 min size MOS cap (C7)
- Coplanar Strip Line
  9GHz center frequency
- 0.18 um CMOS, 6 metal process

Chip Photo



Measurement Frequency Step



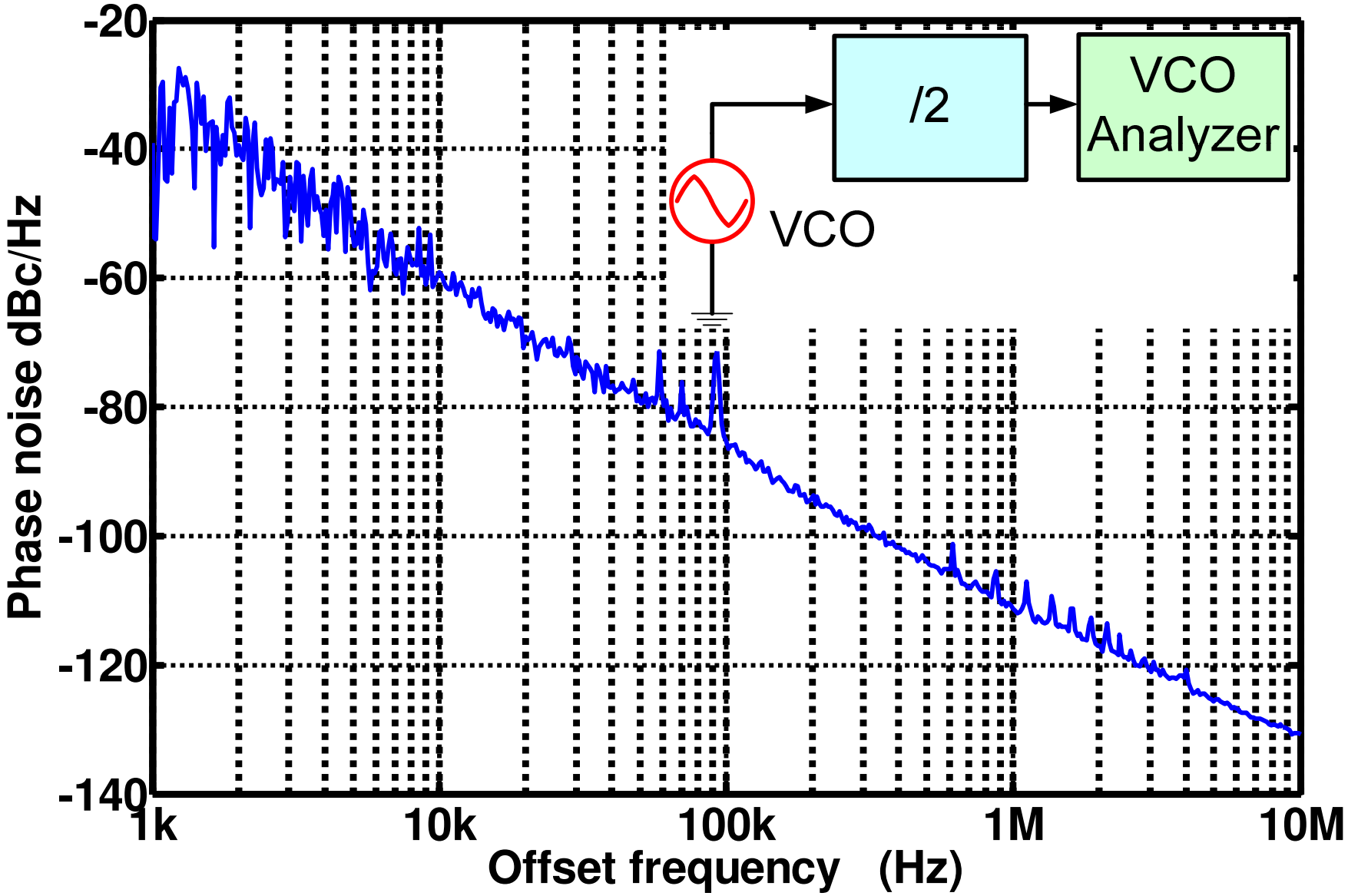
Outer Step C0
376 MHz

Inner Step C6
3.45 MHz

Min Step C7
<100kHz

100X Step Frequency Difference

Phase Noise Measurement



Performance Summary

Process	0.18um CMOS
Resonance Frequency	9.2 GHz
Power supply	1.8V
Bias Current	5mA
Frequency Step outer	376MHz
Frequency Step inner	3.45MHz
Min step	< 100Khz
Phase Noise	-105dBc/Hz @1MHz
Q at 9GHz (sim)	6.8

Possible Impact, Challenges

Process	cap	Center Freq	freq step	
130nm	38aF	2.4GHz	23KHz (cal.)	[2]
90nm	50aF	3.6GHz/2=1.8GHz	20KHz (cal.)	[3]
90nm	50aF	11.15GHz/5=2.23GHz	160Hz (sim.)	This*

***Predicted using, 3000um TL, cap 50um from short**

- **Slight more difficult to predict resonance freq. than LC case**

- **Making real linear DCO slightly more difficult**
- **Calibration necessary (same as LC)**

[2] Staszewski, JSSC Dec.04
[3] Staszewski, JSSC May 06

Conclusion

- **Spatial Cap. Sensitivity Exists in Distributed Resonators**
- **Spatial Sensitivity shown in design of oscillators w/ very fine freq. step and large calibration range**
- **Better freq. step resolution is possible, practically limited by accuracy of short on distributed resonator**

Reference

[1] R. B. Staszewski, C. Hung, N. Barton, M Lee and D. Leipold, “A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones”, IEEE J. Solid-State Circuits, Vol. 40, pp. 2203-2211, November 2005.

[2] R.B. Staszewski, “All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130nm CMOS”, J. Solid-State Circuits, Dec. 2004

[3] R.B. Staszewski, “A Digitally Controlled Oscillator System for SAW-Less Transmitters in Cellular Handsets”, J. Solid-State Circuits, May 2006

Thank you
for your Attention!

Questions?

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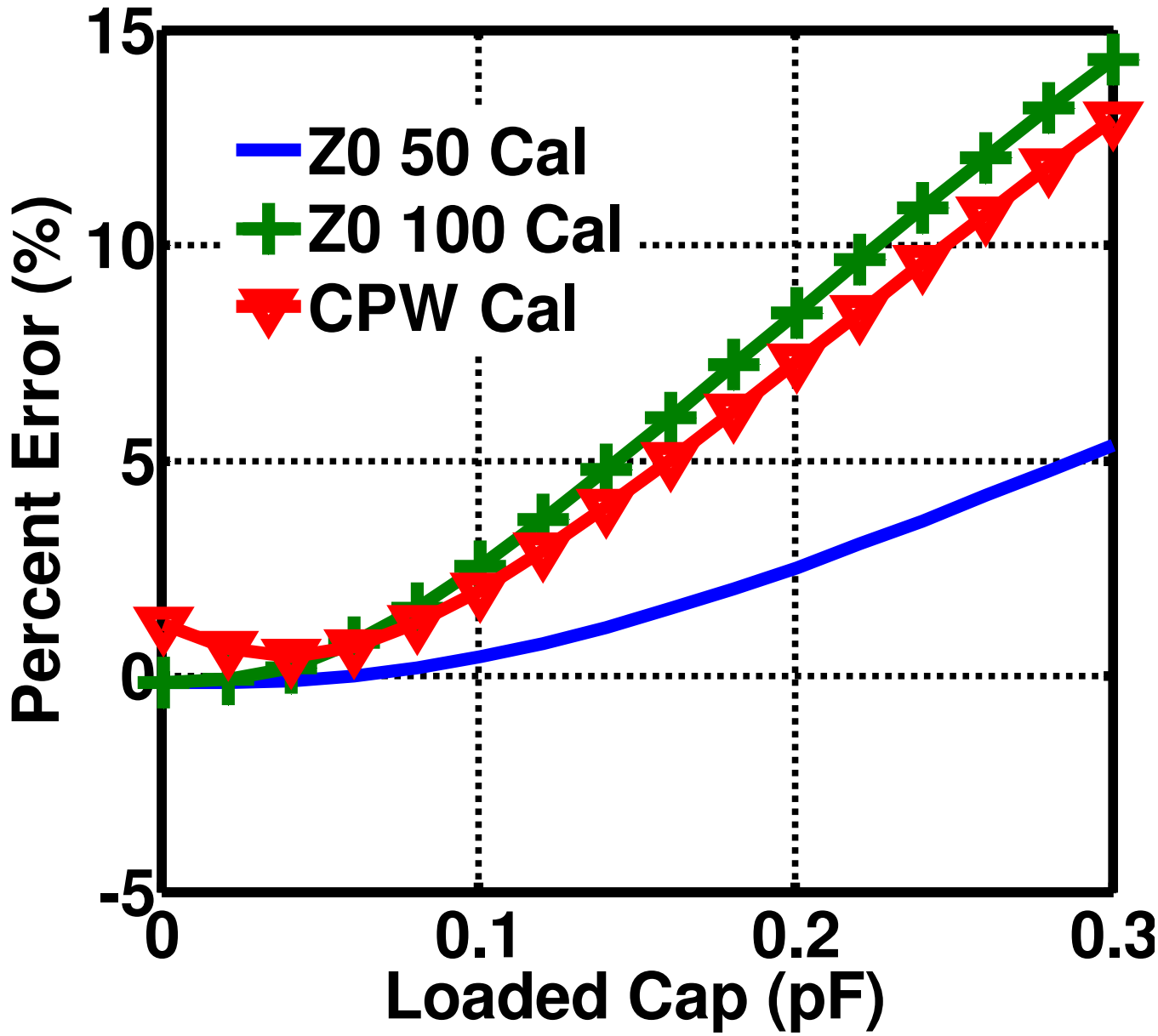
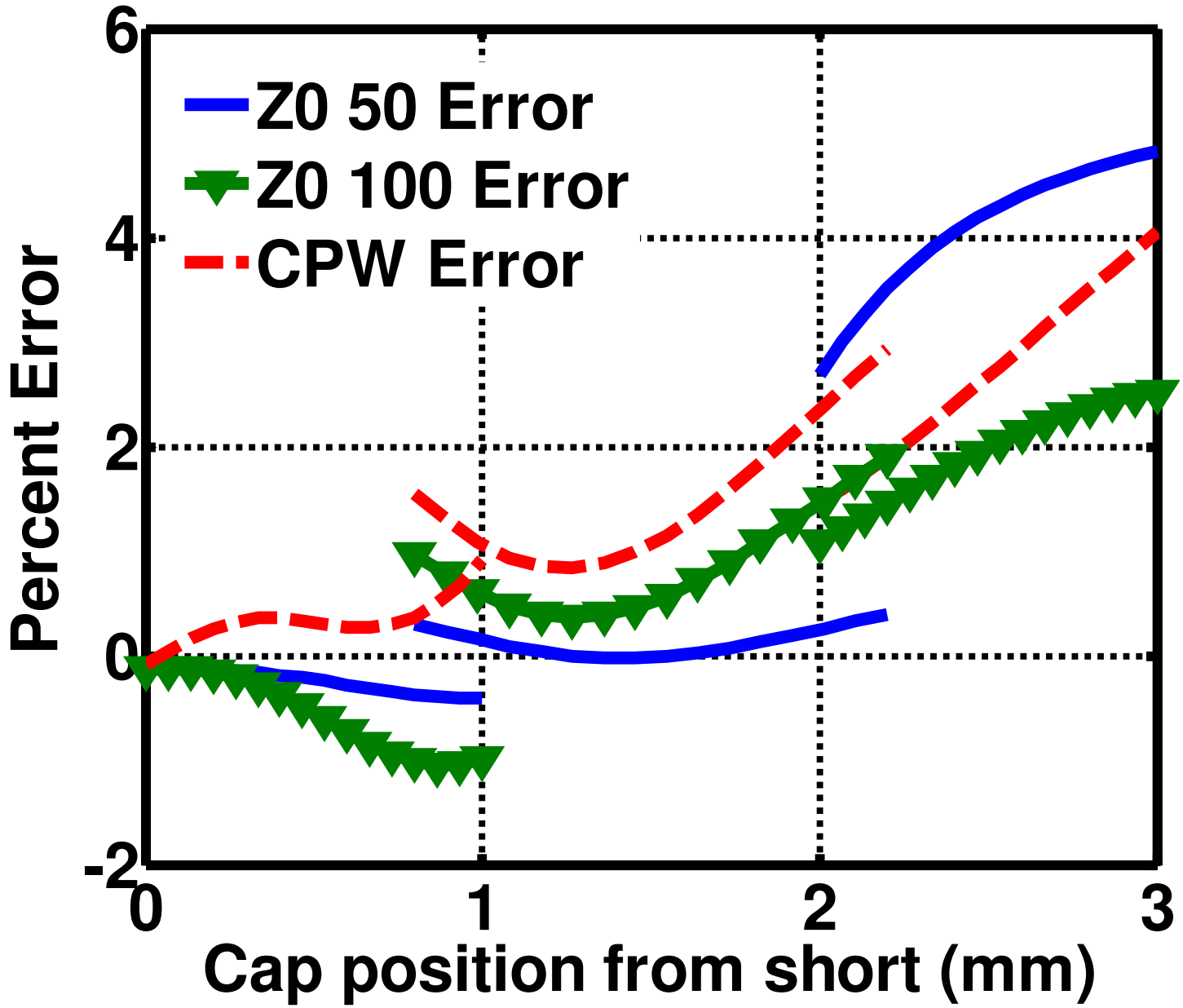
Extra

Cal. Error Resonance Calculation



Calculation Error Equ. Cap Method



Taylor Approximation Error